

**25A, 180V and 200V, 0.150 Ohm,
N-Channel Power MOSFETs**

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

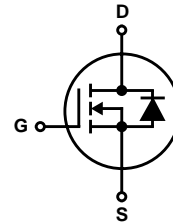
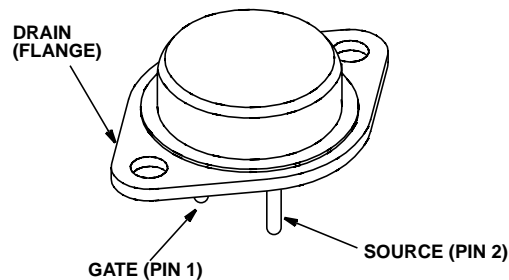
Ordering Information

PART NUMBER	PACKAGE	BRAND
RFK25N18	TO-204AE	RFK25N18
RFK25N20	TO-204AE	RFK25N20

NOTE: When ordering, use the entire part number.

Features

- 25A, 180V and 200V
- $r_{DS(ON)} = 0.150\Omega$

Symbol

Packaging
JEDEC TO-204AE


RFK25N18, RFK25N20

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFK25N18	RFK25N20	UNITS	
Drain to Source Voltage (Note 1)	V_{DS}	180	200	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	25	25	A
Pulsed Drain Current (Note 3)	I_{DM}	60	60	A
Gate to Source Voltage	V_{GS}	± 20	± 20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFK25N18	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0$	180	-	-	V
			RFK25N20	200	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 25\text{A}, V_{GS} = 10\text{V}$ (Figures 6, 7)	-	-	0.150	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 25\text{A}, V_{GS} = 10\text{V}$	-	-	3.75	V
Turn On Delay Time	$t_{d(ON)}$	$I_D \approx 12.5\text{A}, V_{DD} = 100\text{V}, R_G = 50, V_{GS} = 10\text{V}$ $R_L = 8,$ (Figures 10, 11, 12)	-	40	80	ns
Rise Time	t_r		-	150	225	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	300	400	ns
Fall Time	t_f		-	120	200	ns
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$ $f = 1\text{MHz}$ (Figure 9)	-	-	3500	pF
Output Capacitance	C_{OSS}		-	-	900	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	400	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.83	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 12.5\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	300	-	ns

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$ Duty Cycle $\leq 2\%$.
- Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

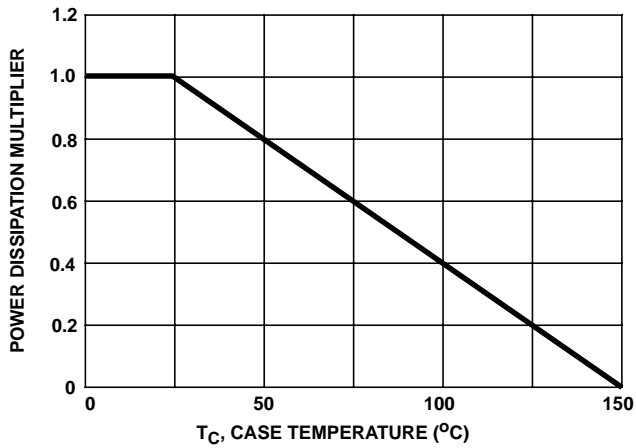


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

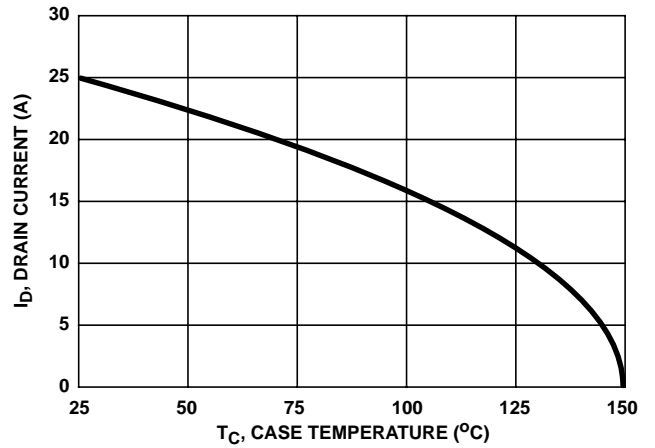


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

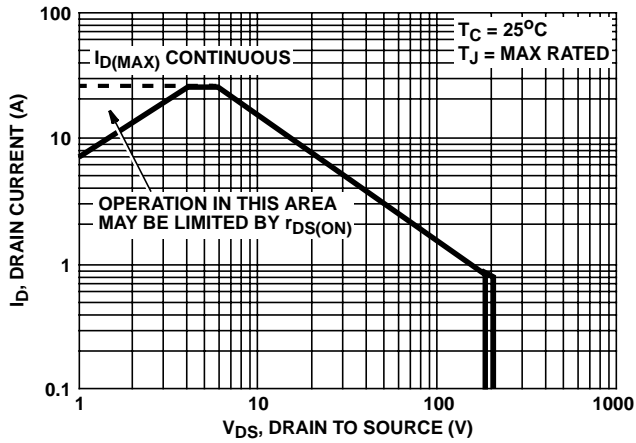


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

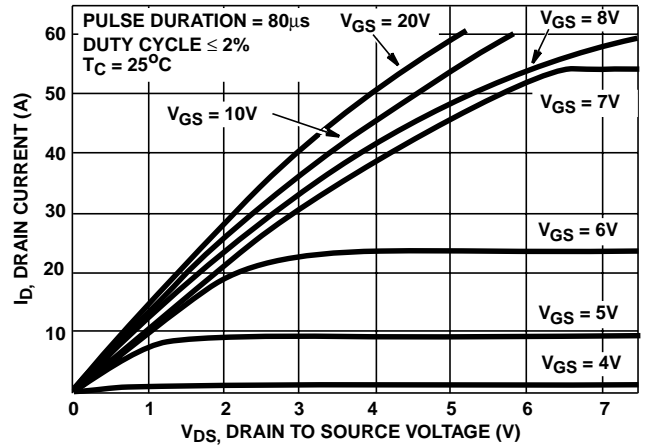


FIGURE 4. SATURATION CHARACTERISTICS

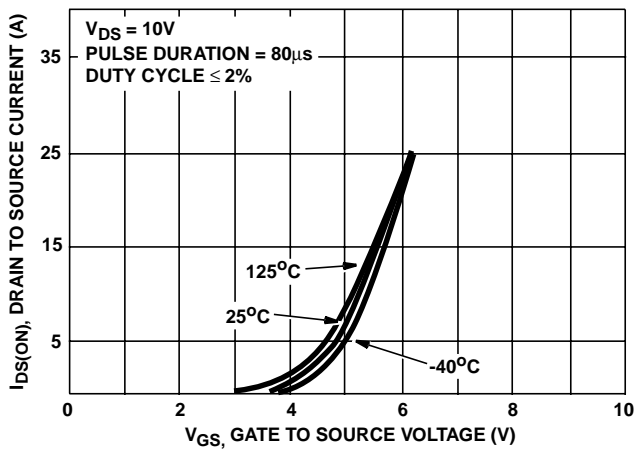


FIGURE 5. TRANSFER CHARACTERISTICS

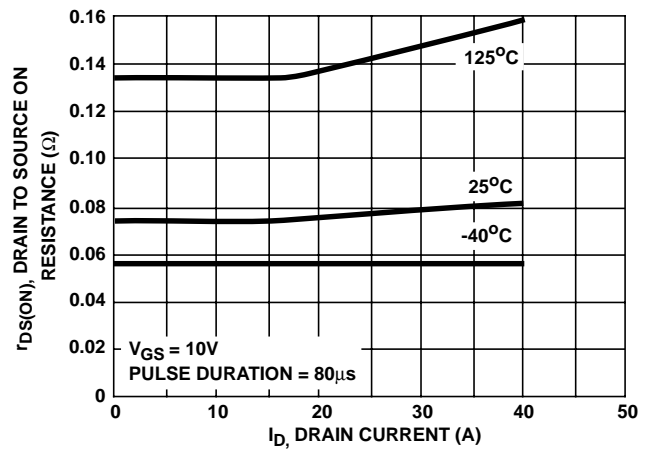


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

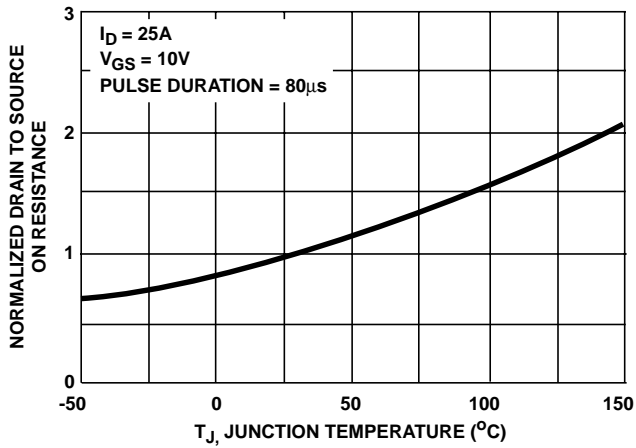


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

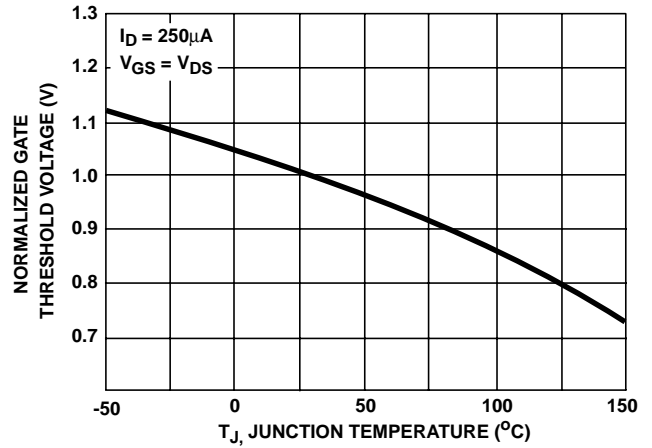


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

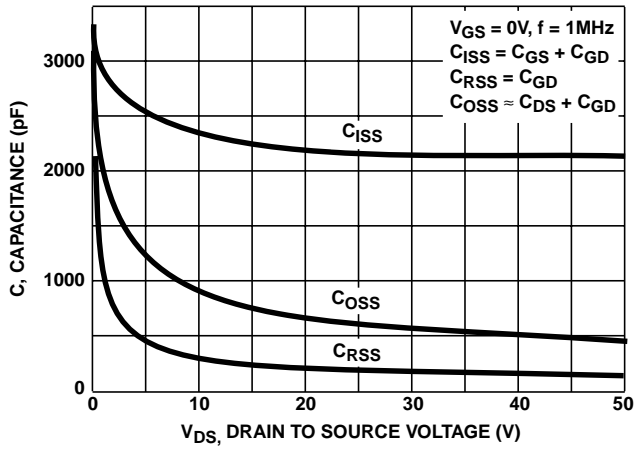
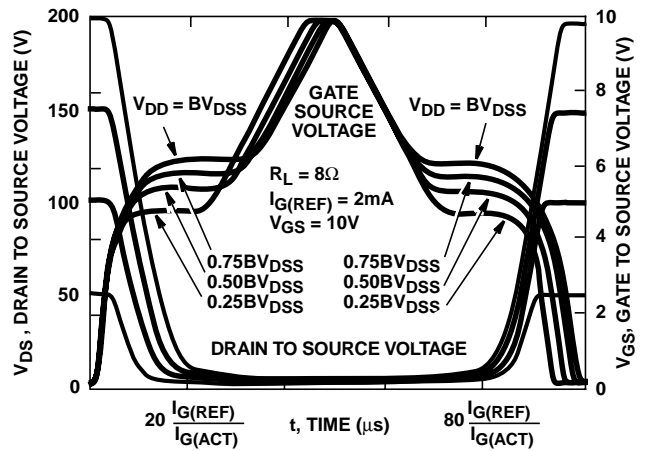


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

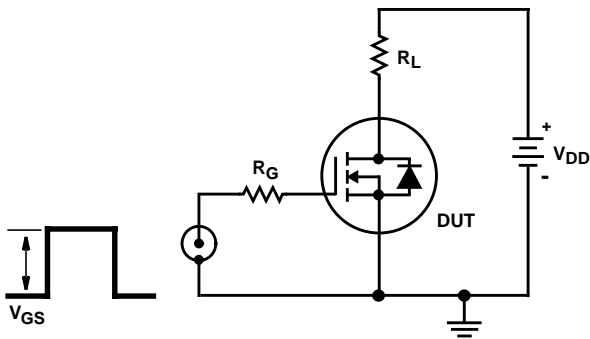


FIGURE 11. RESISTIVE SWITCHING TEST CIRCUIT

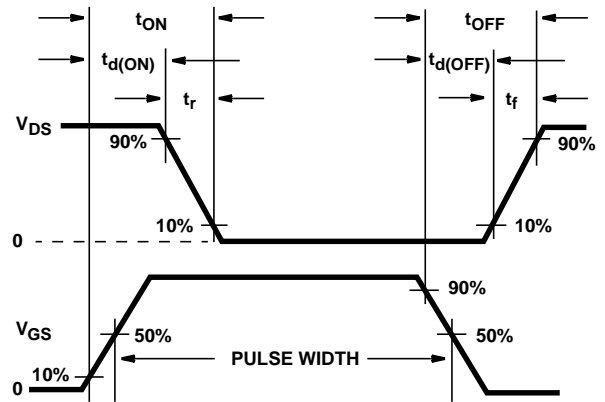


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

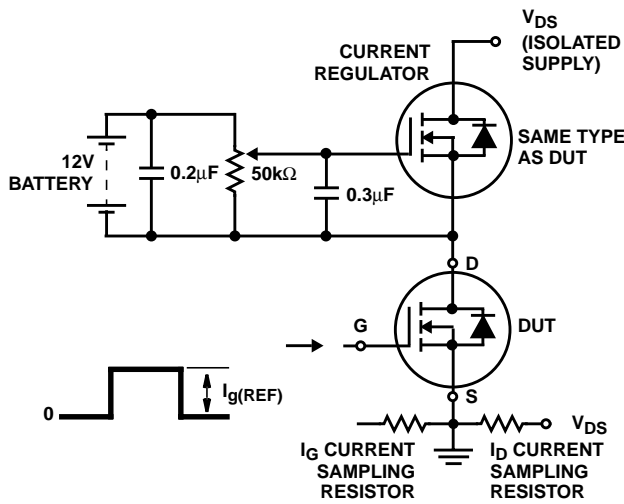


FIGURE 13. GATE CHARGE TEST CIRCUIT

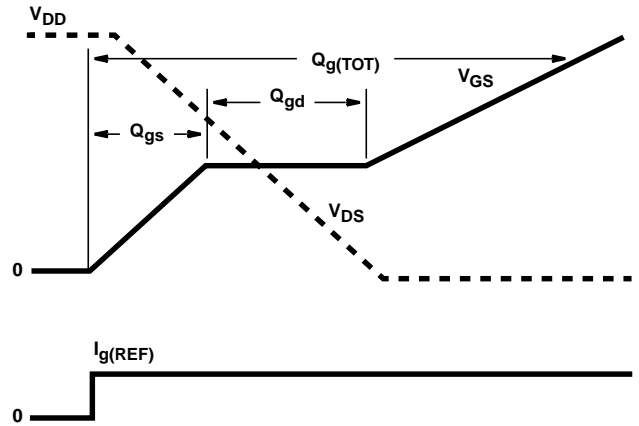


FIGURE 14. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029