

Data Sheet July 1999 File Number 2214.4

3.0A, 100V, 1.200 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17541.

Ordering Information

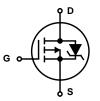
PART NUMBER	PACKAGE	BRAND
IRF9510	TO-220AB	IRF9510

NOTE: When ordering, include the entire part number.

Features

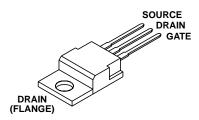
- 3.0A, 100V
- $r_{DS(ON)} = 1.200\Omega$
- Single Pulse Avalanche Energy Rated
- · SOA is Power Dissipation Limited
- · Nanosecond Switching Speeds
- · Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	IRF9510	UNITS
Drain to Source Voltage (Note 1)	-100	V
Drain to Gate Voltage (R _{GS} = 20kΩ) (Note 1)	-100	V
Continuous Drain Current	-3.0	Α
$T_C = 100^{\circ}C$	-2.0	Α
Pulsed Drain Current (Note 3)	-12	Α
Gate to Source Voltage	±20	V
Maximum Power Dissipation	20	W
Linear Derating Factor	0.16	W/oC
Single Pulse Avalanche Energy Rating (Note 4)	190	mJ
Operating and Storage Temperature Range	-55 to 150	οС
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	οС
Package Body for 10s, See Techbrief 334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}C$ to $125^{\circ}C$.

$\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{C} = 25^{o}\text{C, Unless Otherwise Specified}$

PARAMETER	SYMBOL	TEST COI	NDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0V, I_D = -250\mu A, (Figure 10)$		-100	-	-	V
Gate to Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	$V_{GS} = V_{DS}, I_{D} = -250\mu A$		-	-4.0	V
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Zero-Gate Voltage Drain Current	I _{DSS}	V_{DS} = Rated BV _{DSS} , V_{GS} = 0V V_{DS} = 0.8 x Rated BV _{DSS} , V_{GS} = 0V, T_C = 125°C		-	-	-25	μА
				-	-	-250	μА
On-State Drain Current (Note 2)	I _{D(ON)}	$V_{DS} > I_{D(ON) \times r_{DS(ON)MAX}}, V_{GS} = -10V,$ (Figure 7)		-3.0	-	-	А
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	$V_{GS} = -10V, I_D = -1.5A,$	(Figures 8, 9)	-	1.000	1.200	Ω
Forward Transconductance (Note 2)	9fs	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} Max$, $I_D = -1.5A$, (Figure 12)		0.8	1.1	-	S
Turn-On Delay Time	t _d (ON)	$\begin{array}{l} V_{DD} = 0.5 \text{ x Rated BV}_{DSS}, I_D \approx -3.0\text{A}, \\ R_G = 50\Omega, V_{GS} = 10\text{V}, \text{ (Figures 17, 18)} \\ R_L = 15.7\Omega \text{ for V}_{DSS} = 50\text{V} \\ R_L = 12.3\Omega \text{ for V}_{DSS} = 40\text{V} \\ \text{MOSFET Switching Times are} \\ \text{Essentially Independent of Operating} \\ \text{Temperature} \end{array}$		-	15	30	ns
Rise Time	t _r			-	30	60	ns
Turn-Off Delay Time	t _d (OFF)			-	20	40	ns
Fall Time	t _f			-	20	40	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{g(TOT)}	V _{GS} = -10V, I _D = -3A, V _{DS} = 0.8 x Rated BV _{DSS} , (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature		-	8.5	11	nC
Gate to Source Charge	Q _{gs}			-	3.8	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	4.7	-	nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz, (Figure 11)		-	180	-	pF
Output Capacitance	Coss			-	85	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	30	-	pF
Internal Drain Inductance	L _D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die	Inductances G C Ls	-	4.5	-	nH
Internal Source Inductance	L _S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Junction to Case	$R_{\theta JC}$			-	-	6.4	°C/W
Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount		-	-	62.5	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I _{SD}	Modified MOSFET	♀ D	-	-	-3.0	Α
Pulse Source to Drain Current (Note 3)	I _{SDM}	Symbol Showing the Integral Reverse P-N Junction Diode	G o s	-	-	-12	A
Source to Drain Diode Voltage(Note 2)	V _{SD}	$T_C = 25^{\circ}C$, $I_{SD} = -3.0A$, $V_{GS} = 0V$, (Figure 13)		-	-	-1.5	V
Reverse Recovery Time	t _{rr}	$T_J = 150^{\circ}C$, $I_{SD} = -3.0A$, $dI_{SD}/dt = 100A/\mu s$		-	120	-	ns
Reverse Recovered Charge	Q _{RR}	$T_J = 150^{\circ}C$, $I_{SD} = -3.0A$, $dI_{SD}/dt = 100A/\mu s$		-	6.0	-	μС

NOTES:

- 2. Pulse test: pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
- 3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- 4. $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, L = 31.7mH, $R_G = 25\Omega$, peak $I_{AS} = 3.0$ A. See Figures 15, 16.

Typical Performance Curves Unless Otherwise Specified

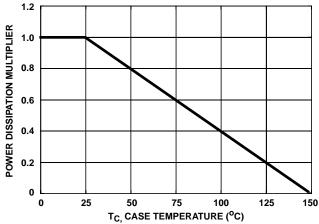


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE
TEMPERATURE

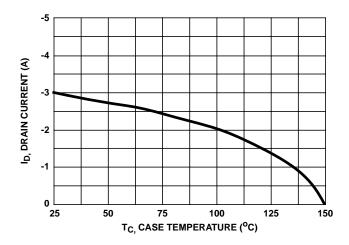


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

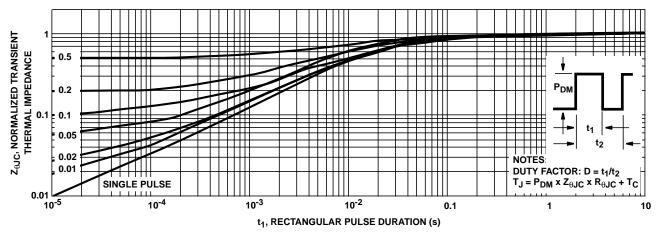


FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

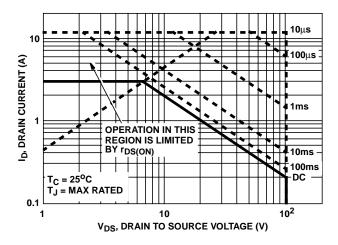


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

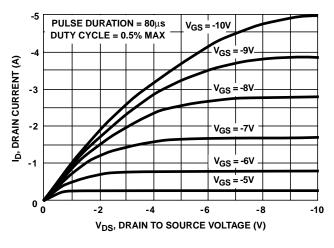


FIGURE 6. SATURATION CHARACTERISTICS

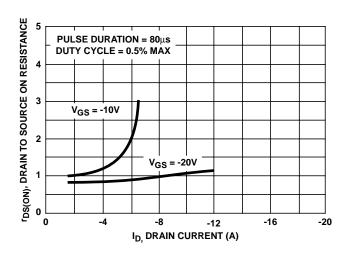


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

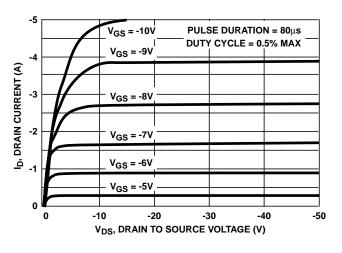


FIGURE 5. OUTPUT CHARACTERISTICS

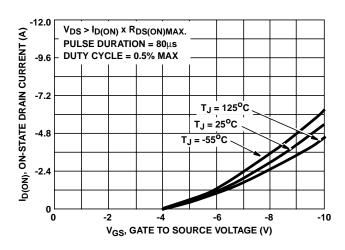


FIGURE 7. TRANSFER CHARACTERISTICS

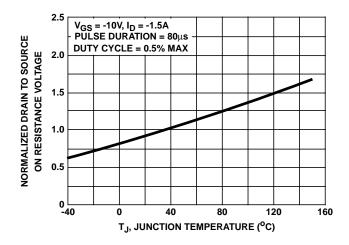


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

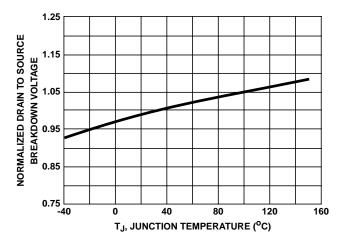


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

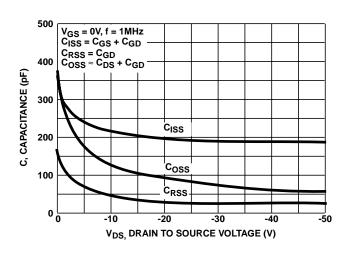


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

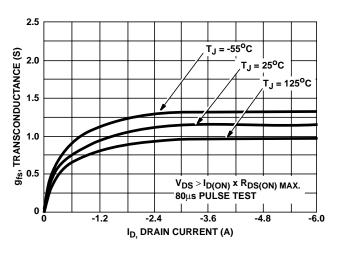


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

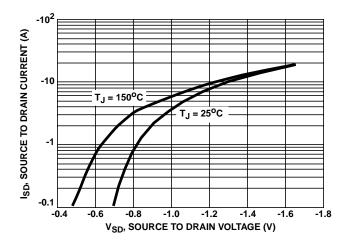


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

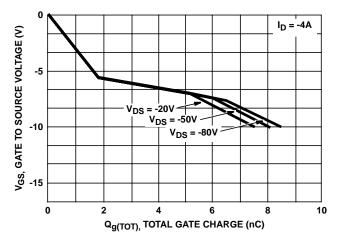


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

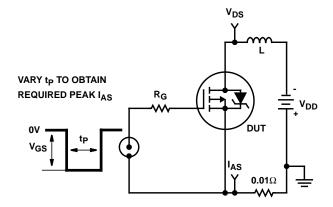


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

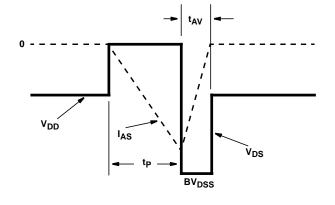


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

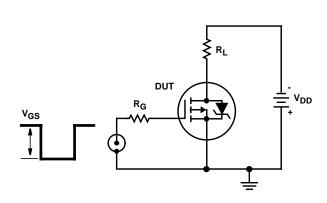


FIGURE 17. SWITCHING TIME TEST CIRCUIT

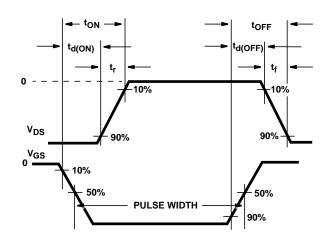


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

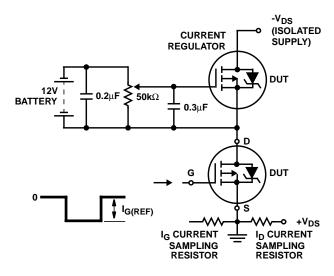


FIGURE 19. GATE CHARGE TEST CIRCUIT

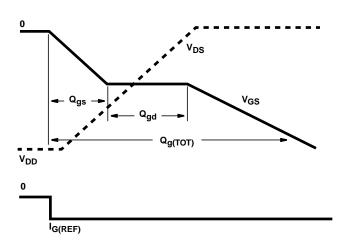


FIGURE 20. GATE CHARGE WAVEFORMS

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