HCS190MS

Radiation Hardened Synchronous 4-Bit Up/Down Counter

September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii $\leq$ 5μA at VOL, VOH

Description

The Intersil HCS190MS is an asynchronously presettable BCD Decade synchronous counter. Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the parallel load input ($\overline{PL}$). Counting occurs when ($\overline{PL}$) is high, Count Enable ($\overline{CE}$) is low and the Up/Down ($\overline{U}$/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high speed cascading. The TC output also initiates the Ripple Clock output ($\overline{RC}$) which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counter can be cascaded using the Ripple Carry output.

If the decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts.

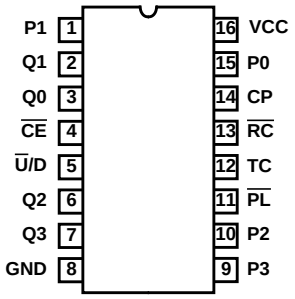
The HCS190MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCS190MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

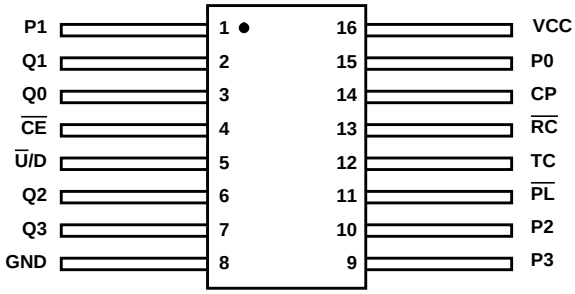
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T16

TOP VIEW



16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F16

TOP VIEW



TRUTH TABLE

INPUTS				OUTPUT FUNCTION
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset
H	H	X	X	No Change

H = High Voltage Level X = Immaterial
L = Low Voltage Level ⎍ =Positive Transistion

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS190DMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead SBDIP
HCS190KMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead Ceramic Flatpack
HCS190D/Sample	+25^{o}C	Sample	16 Lead SBDIP
HCS190K/Sample	+25^{o}C	Sample	16 Lead Ceramic Flatpack
HCS190HMSR	+25^{o}C	Die	Die

Spec Number **518836**
File Number **2251.2**

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10sec) . . . . . $+265^oC$
Junction Temperature (TJ) . . . . . $+175^oC$
ESD Classification . . . . . Class 1
(All Voltage Reference to the VSS Terminal)

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$73^oC/W$	$24^oC/W$
Ceramic Flatpack Package	$114^oC/W$	$29^oC/W$

Maximum Package Power Dissipation at $+125^oC$ Ambient
SBDIP Package. 0.68W
Ceramic Flatpack Package 0.44W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package. . . . . $13.7mW/^oC$
Ceramic Flatpack Package . . . . . $8.8mW/^oC$
Gate Count . . . . . 13 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Input Rise and Fall Time at 4.5V VCC (tr, tf) . . . . . 100ns/V Max.
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input High Voltage. . . . . VCC to 70% of VCC
Input Low Voltage . . . . . .0V to 30% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	40	µA
			2, 3	$+125^oC$, -55^oC	-	750	µA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	$+25^oC$	-4.8	-	mA
			2, 3	$+125^oC$, -55^oC	-4.0	-	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	$+25^oC$	4.8	-	mA
			2, 3	$+125^oC$, -55^oC	4.0	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 3)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	V

NOTES:

1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	30	ns
$\overline{PL}$ to Qn			10, 11	+125°C, -55°C	2	35	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	41	ns
Pn to Qn	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	38	ns
CP to Qn	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
CP to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	28	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	26	ns
CP to TC	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	41	ns
			10, 11	+125°C, -55°C	2	49	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	47	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	37	ns
			10, 11	+125°C, -55°C	2	40	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	40	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	43	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	36	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	36	pF
			1	+125°C, -55°C	-	62	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	12	-	ns
Pn to $\overline{PL}$			1	+125°C, -55°C	18	-	ns
	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	12	-	ns
$\overline{CE}$ to CP			1	+125°C, -55°C	18	-	ns
	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	18	-	ns
$\overline{U}$/D to CP			1	+125°C, -55°C	27	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	2	-	ns
Pn to $\overline{PL}$			1	+125°C, -55°C	2	-	ns
	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	2	-	ns
$\overline{CE}$ to CP			1	+125°C, -55°C	2	-	ns
	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	0	-	ns
$\overline{U}$/D to CP			1	+125°C, -55°C	0	-	ns
Pulse Width Time	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	16	-	ns
CP			1	+125°C, -55°C	24	-	ns
	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	20	-	ns
$\overline{PL}$			1	+125°C, -55°C	30	-	ns
Recovery Time	TREC	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Maximum Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	30	-	ns
			1	+125°C, -55°C	20	-	ns
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	1	15	ns
			1	+125°C, -55°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0	+25°C	-4.0	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4.0	-	mA

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 2)	+25°C	-	-	V
Propagation Delay	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	35	ns
$\overline{PL}$ to Qn	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	41	ns
Pn to Qn	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	33	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	38	ns
CP to Qn	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	37	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	34	ns
CP to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	28	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	26	ns
CP to TC	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	49	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	47	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	40	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	40	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	43	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	36	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	25	ns
	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
2, 3, 6, 7, 12, 13	1, 4, 5, 8, 9, 10, 11, 14, 15	-	16	-	-
STATIC II BURN-IN (Note 1)					
2, 3, 6, 7, 12, 13	8	-	1, 4, 5, 9, 10, 11, 14, 15, 16	-	-
DYNAMIC BURN-IN (Note 2)					
-	1, 4, 5, 8, 9, 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTES:

1. Each pin except VCC and GND will have a series resistor of 10K ± 5%.
2. Each pin except VCC and GND will have a series resistor of 1K ± 5%.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9, 10, 11, 14, 15, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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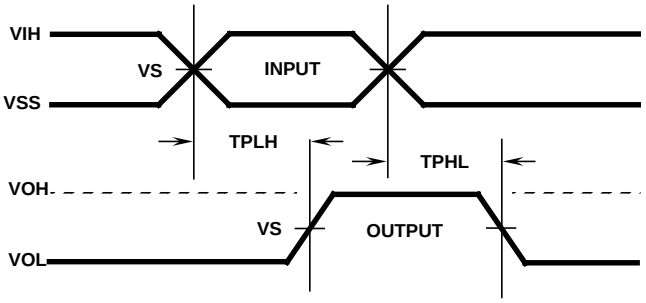
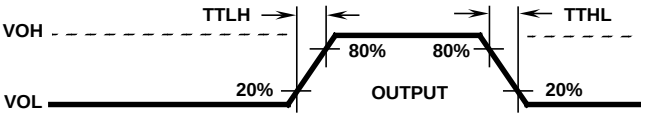
Propagation Delay Timing Diagram



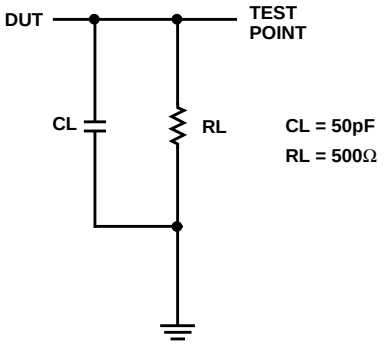
Transition Timing Diagram



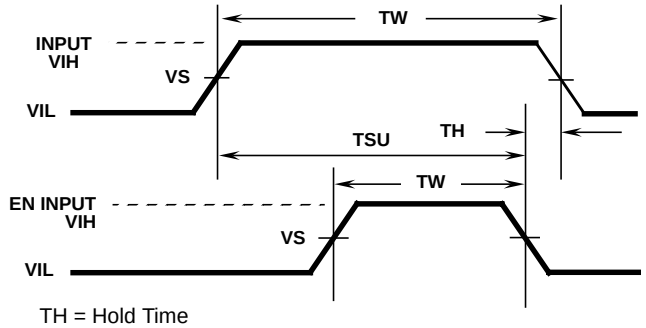
VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

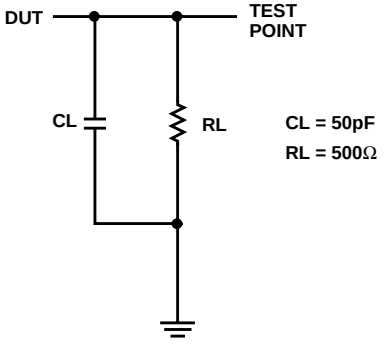


TH = Hold Time
TSU = Setup Time
TW = Pulse Width

AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 (mils)
2.65 x 2.19 (mm)

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

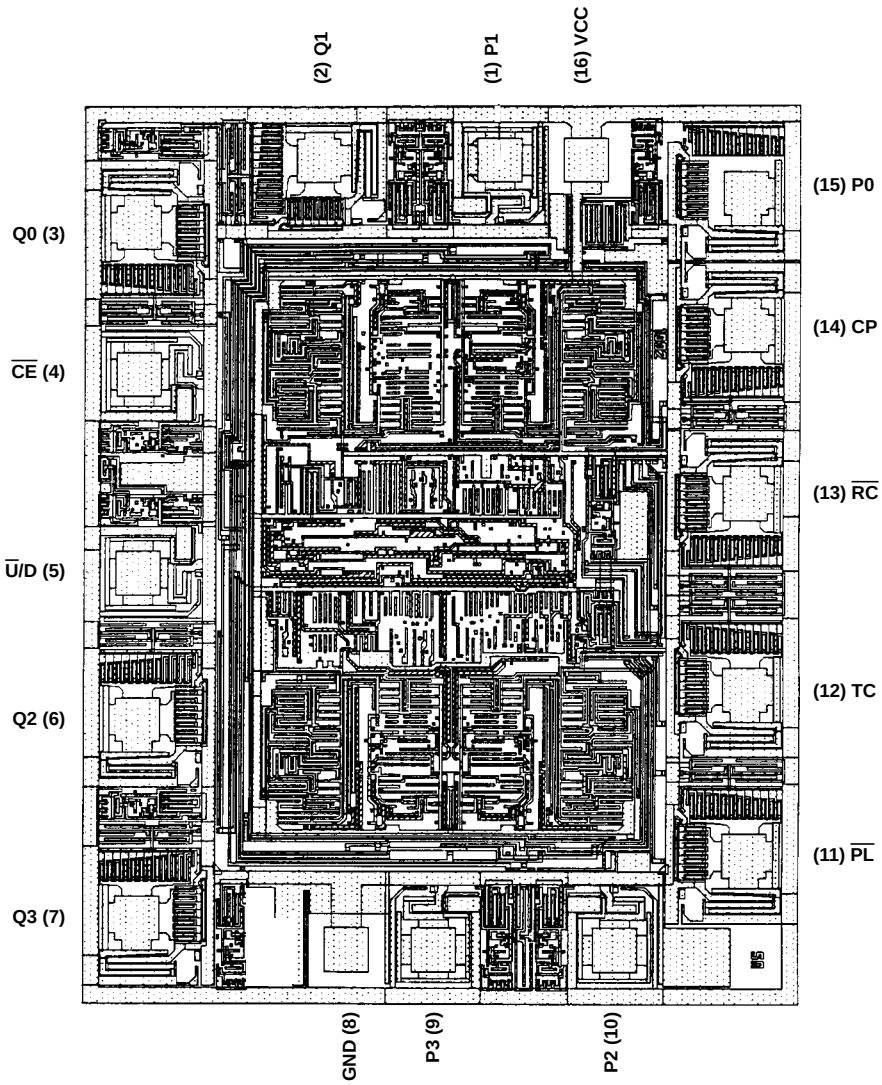
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5$ A/cm^2

BOND PAD SIZE:
4 x 4 (mils)
100 x 100µm

Metallization Mask Layout

HCS190MS



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS190 is TA14344A.