Data Sheet June 1999 File Number 2419.2

## 13A, 50V, 0.120 Ohm, N-Channel Power MOSFET

This is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Formerly developmental type TA9770.

## Ordering Information

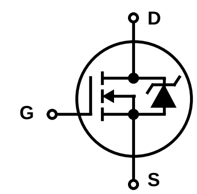
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| BUZ71A | TO-220AB | BUZ71A |

NOTE: When ordering, use the entire part number.

## Features

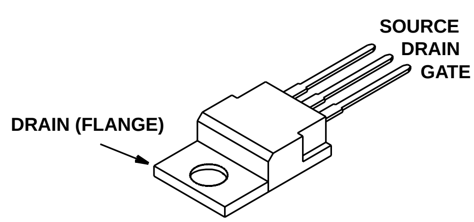
- 13A, 50V
- $r_{DS(ON)} = 0.120\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Symbol




## Packaging

JEDEC TO-220AB



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | BUZ71A | UNITS |
|---|---|---|---|
| Drain to Source Breakdown Voltage (Note 1) | $V_{DS}$ | 50 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 50 | V |
| Continuous Drain Current, $T_C = 55^oC$ | $I_D$ | 13 | A |
| Pulsed Drain Current (Note 3) | $I_{DM}$ | 48 | A |
| Gate to Source Voltage | $V_{GS}$ | ±20 | V |
| Maximum Power Dissipation | $P_D$ | 40 | W |
| Single Pulse Avalanche Energy Rating (Note 4) | $E_{AS}$ | 100 | mJ |
| Linear Derating Factor | | 0.32 | W/$^o$C |
| Operating and Storage Temperature | $T_{STG}$, $T_J$ | -55 to 150 | $^o$C |
| DIN Humidity Category - DIN 40040 | | E | |
| IEC Climatic Category - DIN IEC 68-1 | | 55/150/56 | |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^o$C |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^o$C |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $125^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250μA, $V_{GS}$ = 0V | 50 | - | - | V |
| Gate to Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = 1mA (Figure 9) | 2.1 | 3 | 4 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $T_J = 25^oC$, $V_{DS}$ = 50V, $V_{GS}$ = 0V | - | 20 | 250 | μA |
| | | $T_J = 125^oC$, $V_{DS}$ = 50V, $V_{GS}$ = 0V | - | 100 | 1000 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = 20V, $V_{DS}$ = 0V | - | 10 | 100 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $I_D$ = 9A, $V_{GS}$ = 10V (Figure 8) | - | 0.11 | 0.12 | Ω |
| Forward Transconductance (Note 2) | $g_{fs}$ | $V_{DS}$ = 25V, $I_D$ = 9A (Figure 11) | 3.0 | 5.2 | - | S |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{CC}$ = 30V, $I_D$ ≈ 3A, $V_{GS}$ = 10V, $R_{GS}$ = 50Ω, $R_L$ = 10Ω | - | 20 | 30 | ns |
| Rise Time | $t_r$ | | - | 55 | 85 | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 70 | 90 | ns |
| Fall Time | $t_f$ | | - | 80 | 110 | ns |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz (Figure 10) | - | 480 | 650 | pF |
| Output Capacitance | $C_{OSS}$ | | - | 280 | 450 | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | - | 160 | 280 | pF |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | ≤ 3.1 | | | $^o$C/W |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | ≤ 75 | | | $^o$C/W |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Continuous Source to Drain Current | $I_{SD}$ | $T_C = 25^oC$ | - | - | 13 | A |
| Pulsed Source to Drain Current | $I_{SDM}$ | $T_C = 25^oC$ | - | - | 52 | A |
| Source to Drain Diode Voltage | $V_{SD}$ | $T_J = 25^oC$, $I_{SD}$ = 26A, $V_{GS}$ = 0V, (Figure 12) | - | 1.6 | 2.2 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J = 25^oC$, $I_{SD}$ = 13, $dI_{SD}/dt$ = 100A/μs, $V_R$ = 30V | - | 120 | - | ns |
| Reverse Recovery Charge | $Q_{RR}$ | | - | 0.15 | - | μC |

NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD}$ = 10V, $T_J = 25^oC$, L = 820μH, $I_{PEAK}$ = 14A. (See Figures 14 and 15).

## *Typical Performance Curves* Unless Otherwise Specified

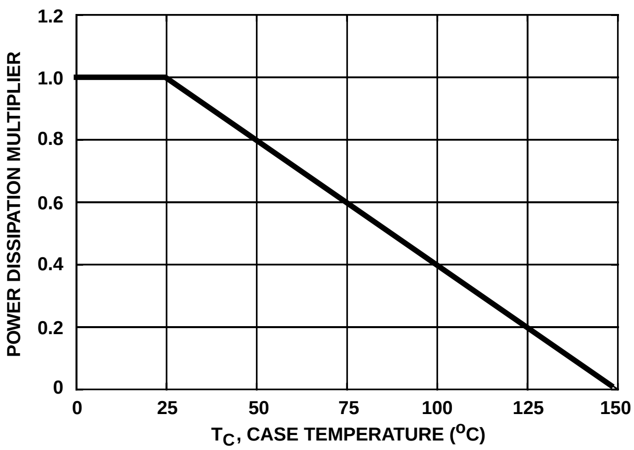



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

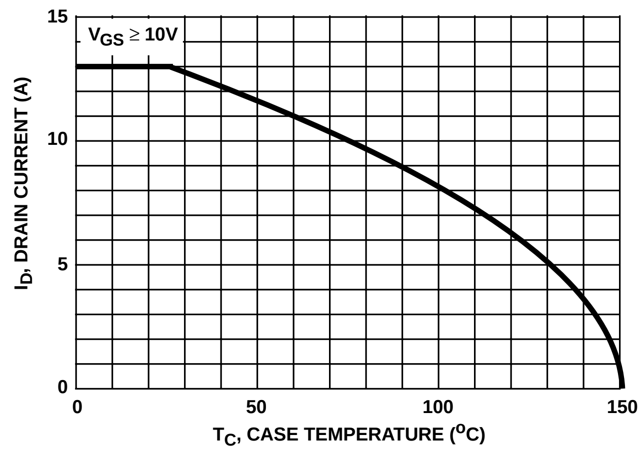



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

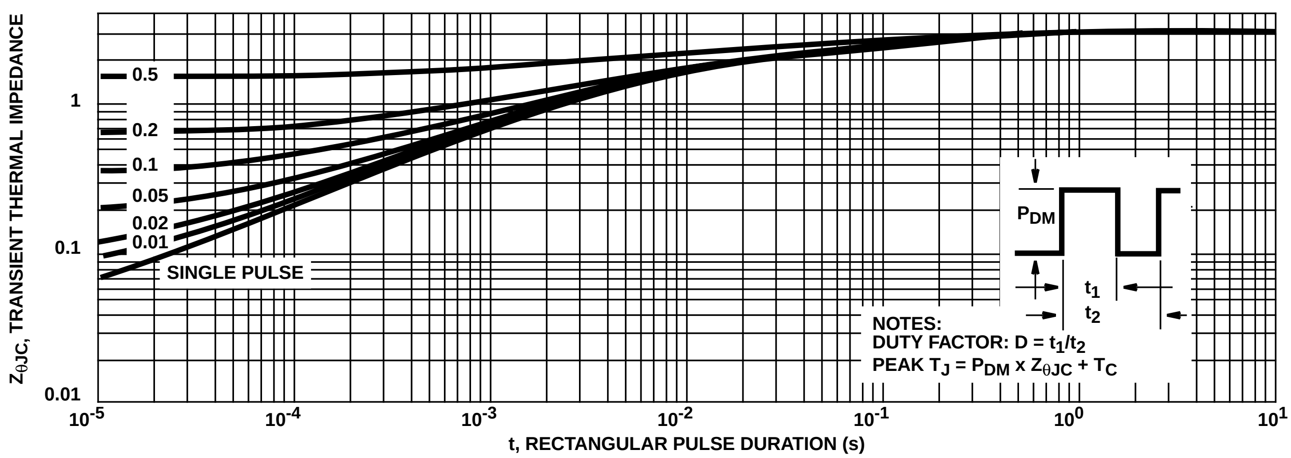



FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

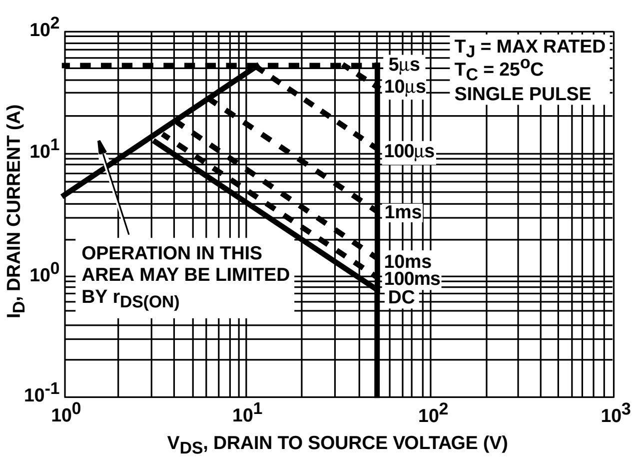



FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

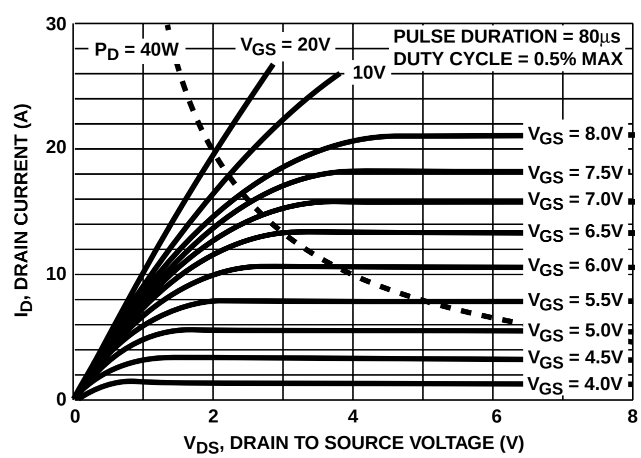



FIGURE 5. OUTPUT CHARACTERISTICS

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

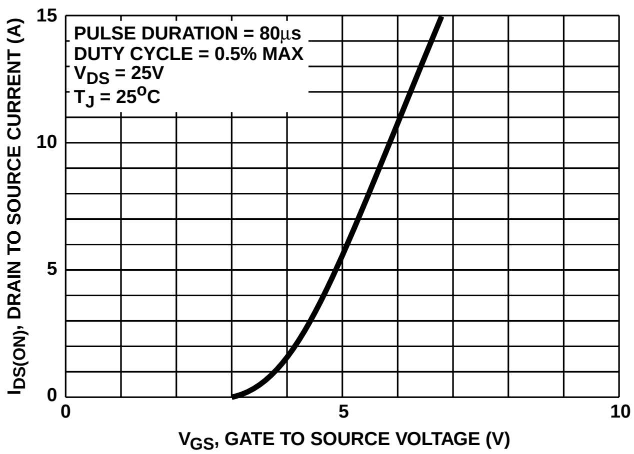



**FIGURE 6. TRANSFER CHARACTERISTICS**

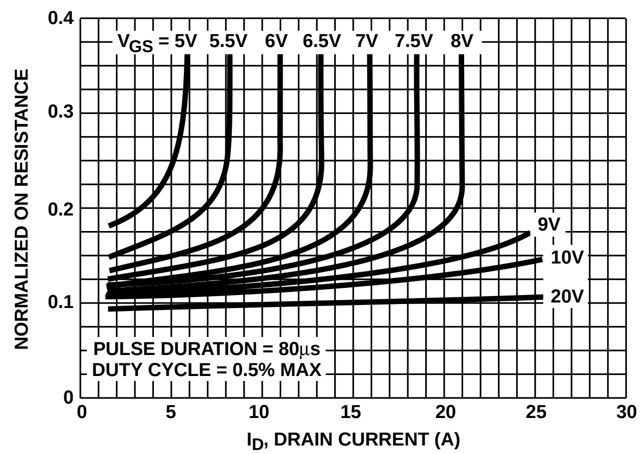



**FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT**

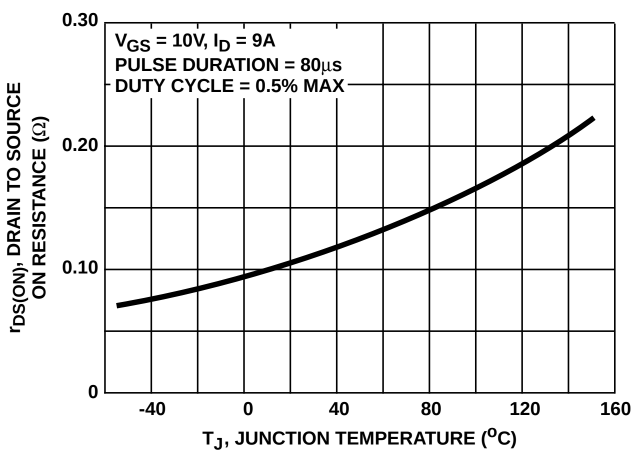



**FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**

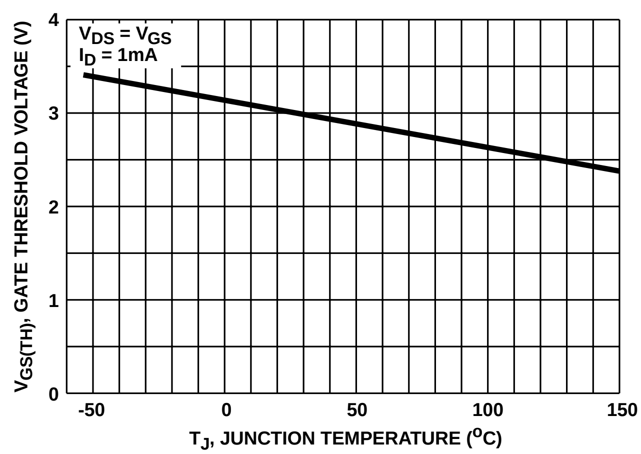



**FIGURE 9. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE**

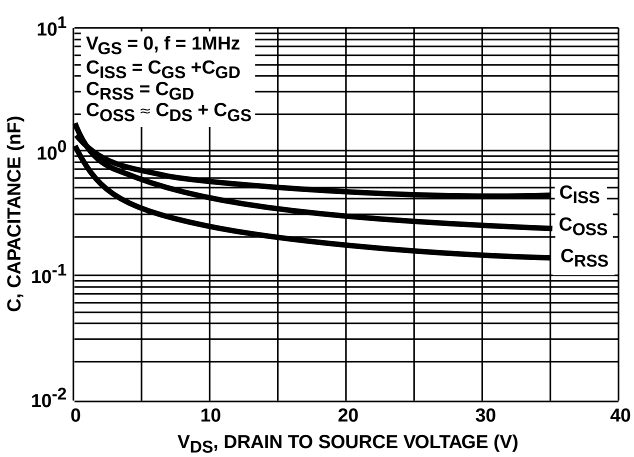



**FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE**

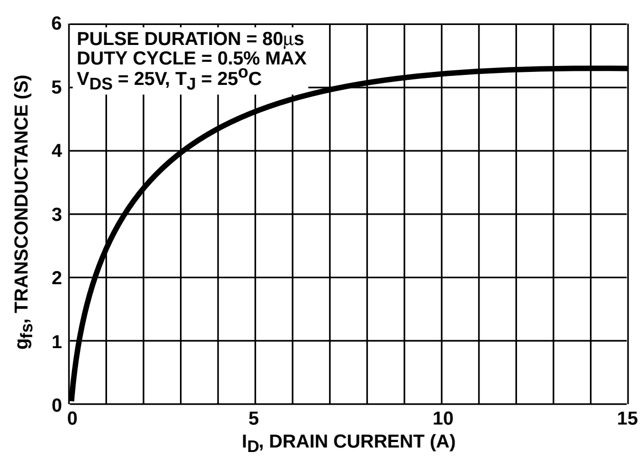



**FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT**

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

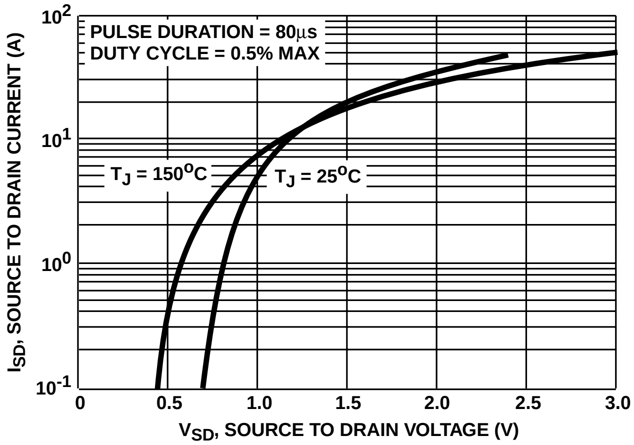



**FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE**

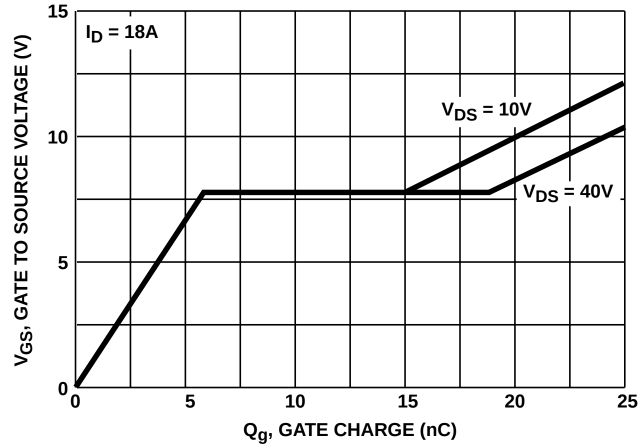



**FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE**

## *Test Circuits and Waveforms*

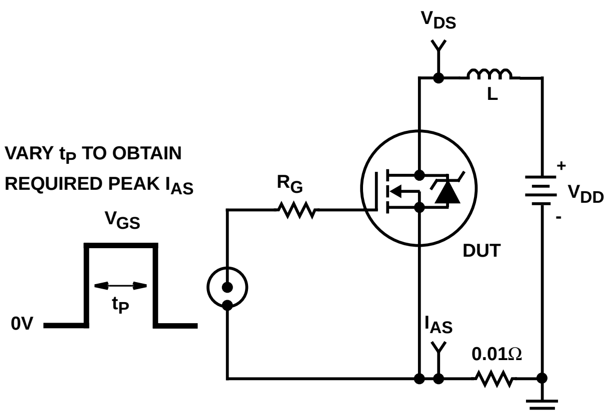



**FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT**

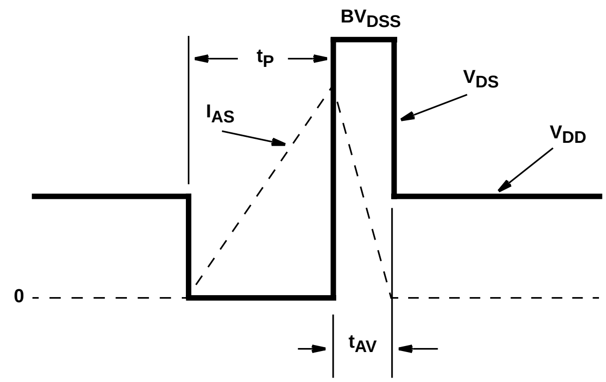



**FIGURE 15. UNCLAMPED ENERGY WAVEFORMS**

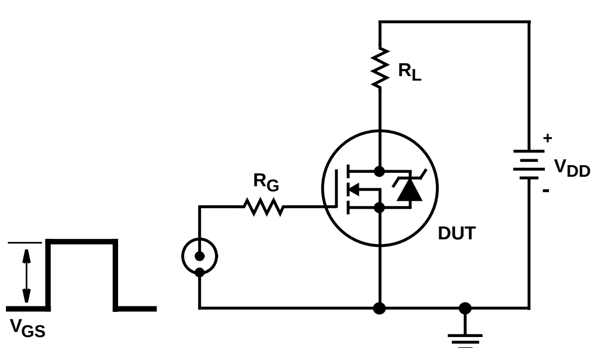



**FIGURE 16. SWITCHING TIME TEST CIRCUIT**

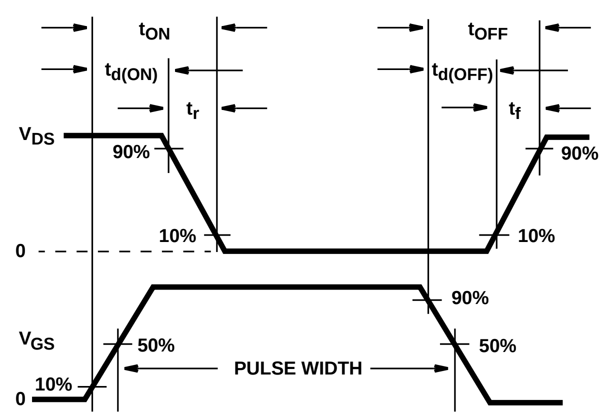



**FIGURE 17. RESISTIVE SWITCHING WAVEFORMS**

## Test Circuits and Waveforms (Continued)

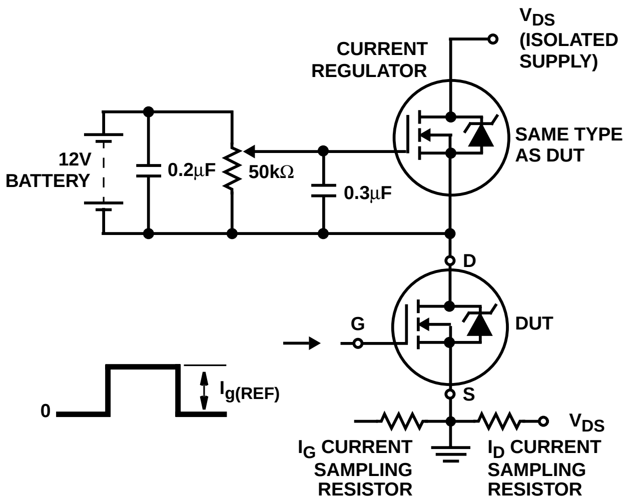



FIGURE 18. GATE CHARGE TEST CIRCUIT

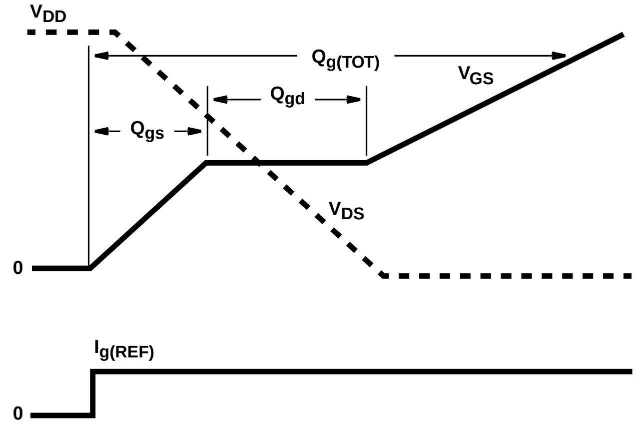



FIGURE 19. GATE CHARGE WAVEFORMS



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