Data Sheet November 1999 File Number 2808.8

Dual FIR Filter

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the Decimation Registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16 x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Features

- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10-Bit Data and Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 19-Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Standard Microprocessor Interface

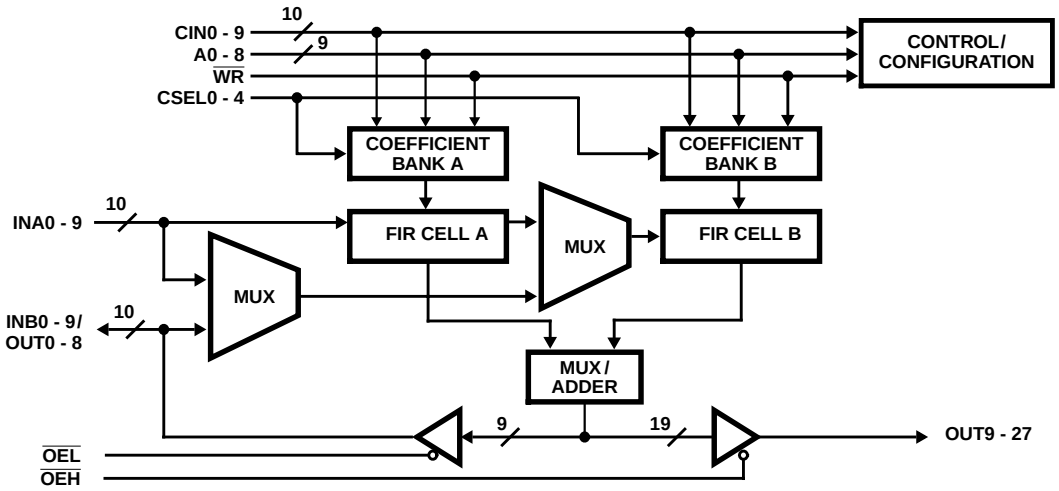
Applications

- Quadrature, Complex Filtering
- Image Processing
- Polyphase Filtering
- Adaptive Filtering

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HSP43168VC-33	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-40	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-45	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-40	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-45	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JI-40	-40 to 85	84 Ld PLCC	N84.1.15
HSP43168GC-45	0 to 70	84 Ld CPGA	G84.A

Block Diagram



Pinouts

84 LEAD CPGA
BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1	
A	$\overline{RVRS}$	$\overline{WR}$	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A
B	$\overline{SHFTEN}$	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
C	$\overline{TXFR}$	$\overline{FWRD}$			A5	A6	CSEL0			CIN6	CIN4	C
D	V_{CC}	ACCEN								GND	CIN3	D
E	$\overline{OEH}$	GND	CLK						CIN2	CIN1	CIN0	E
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	$\overline{OEL}$	INB3			INA0	INA2	J
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	PIN 'A1' ID

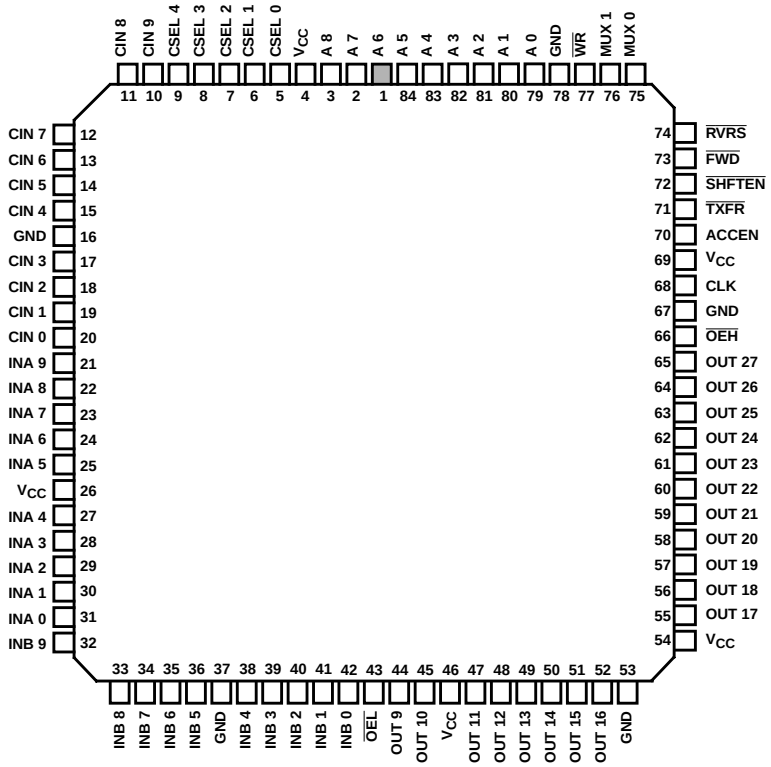
HSP43168
BOTTOM VIEW

84 LEAD CPGA
TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1	
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
J	OUT19	OUT17			OUT9	$\overline{OEL}$	INB3			INA0	INA2	J
H	OUT21	OUT20								INA3	INA4	H
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
E	$\overline{OEH}$	GND	CLK						CIN2	CIN1	CIN0	E
D	V_{CC}	ACCEN								GND	CIN3	D
C	$\overline{TXFR}$	$\overline{FWRD}$			A5	A6	CSEL0			CIN6	CIN4	C
B	$\overline{SHFTEN}$	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
A	$\overline{RVRS}$	$\overline{WR}$	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A
	11	10	9	8	7	6	5	4	3	2	1	PIN 'A1' ID

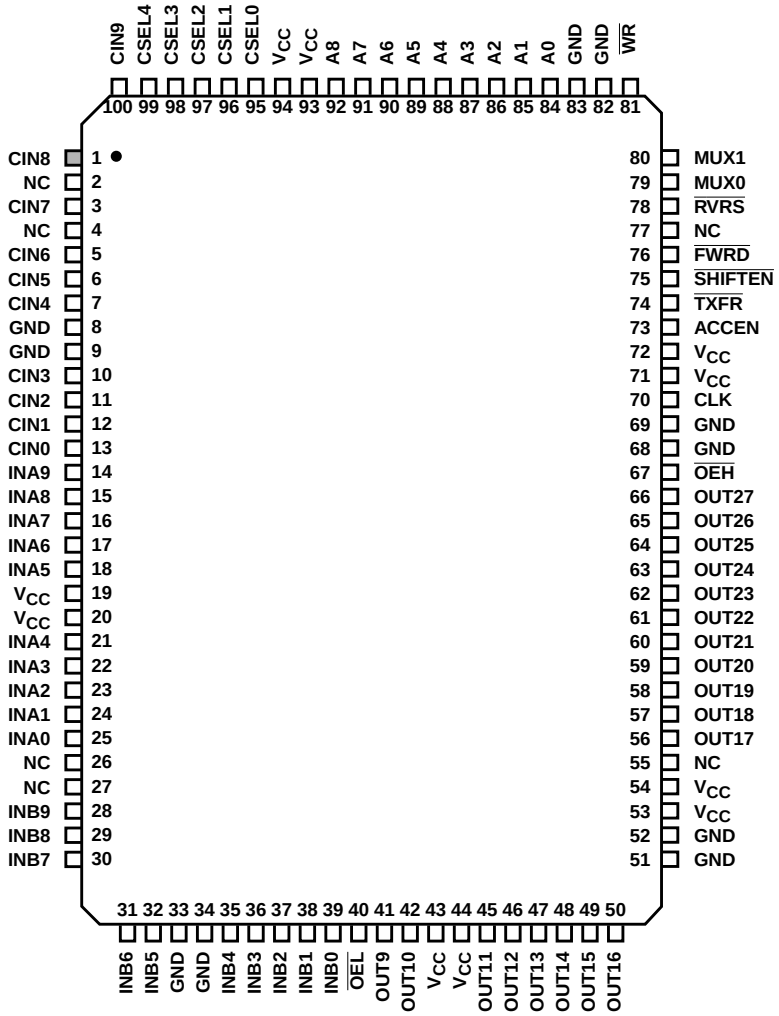
HSP43168
TOP VIEW

84 LEAD PLCC
TOP VIEW



Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



Pin Description

SYMBOL	TYPE	DESCRIPTION
V_{CC}		V_{CC}: +5V power supply pin.
GND		Ground.
CIN0-9	I	Control/Coefficient Data Bus. Processor interface for loading control data and coefficients. CIN0 is the LSB.
A0-8	I	Control/Coefficient Address Bus. Processor interface for addressing Control and Coefficient Registers. A0 is the LSB.
$\overline{WR}$	I	Control/Coefficient Write Clock. Data is latched into the Control and Coefficient Registers on the rising edge of $\overline{WR}$.
CSEL0-4	I	Coefficient Select. This input determines which of the 32 coefficient sets are to be used by FIR A and B. This input is registered and CSEL0 is the LSB.
INA0-9	I	Input to FIR A. INA0 is the LSB.
INB0-9	I/O	Bidirectional Input for FIR B. INB0 is the LSB and is input only. When used as output, INB1-9 are the LSBs of the output bus, and INB9 is the MSB of these bits.
OUT9-27	O	19 MSBs of Output Bus. Data format is either unsigned or two's complement depending on configuration. OUT27 is the MSB.
$\overline{SHFTEN}$	I	Shift Enable. This active low input enables clocking of data into the part and shifting of data through the Decimation Registers.
$\overline{FWRD}$	I	Forward ALU Input Enable. When active low, data from the forward decimation path is input to the ALUs through the “a” input. When high, the “a” inputs to the ALUs are zeroed.
$\overline{RVRS}$	I	Reverse ALU Input Enable. When active low, data from the reverse decimation path is input to the ALUs through the “b” input. When high, the “b” inputs to the ALUs are zeroed.
$\overline{TXFR}$	I	Data Transfer Control. This active low input switches the LIFO being read into the reverse decimation path with the LIFO being written from the forward decimation path (see Figure 1).
MUX0-1	I	Adder/Mux Control. This input controls data flow through the output Adder/Mux. Table 5 lists the various configurations.
CLK	I	Clock. All inputs except those associated with the processor interface (CIN0-9, A0-8, $\overline{WR}$) and the output enables ($\overline{OEL}$, $\overline{OEH}$) are registered by the rising edge of CLK.
$\overline{OEL}$	I	Output Enable Low. This three-state control enables the LSBs of the output bus to INB1-9 when $\overline{OEL}$ is low.
$\overline{OEH}$	I	Output Enable High. This three-state control enables OUT9-27 when $\overline{OEH}$ is low.
ACCEN	I	Accumulate Enable. This active high input allows accumulation in the FIR Cell Accumulator. A low on this input latches the FIR Accumulator contents into the Output Holding Registers while zeroing the feedback pass in the Accumulator.

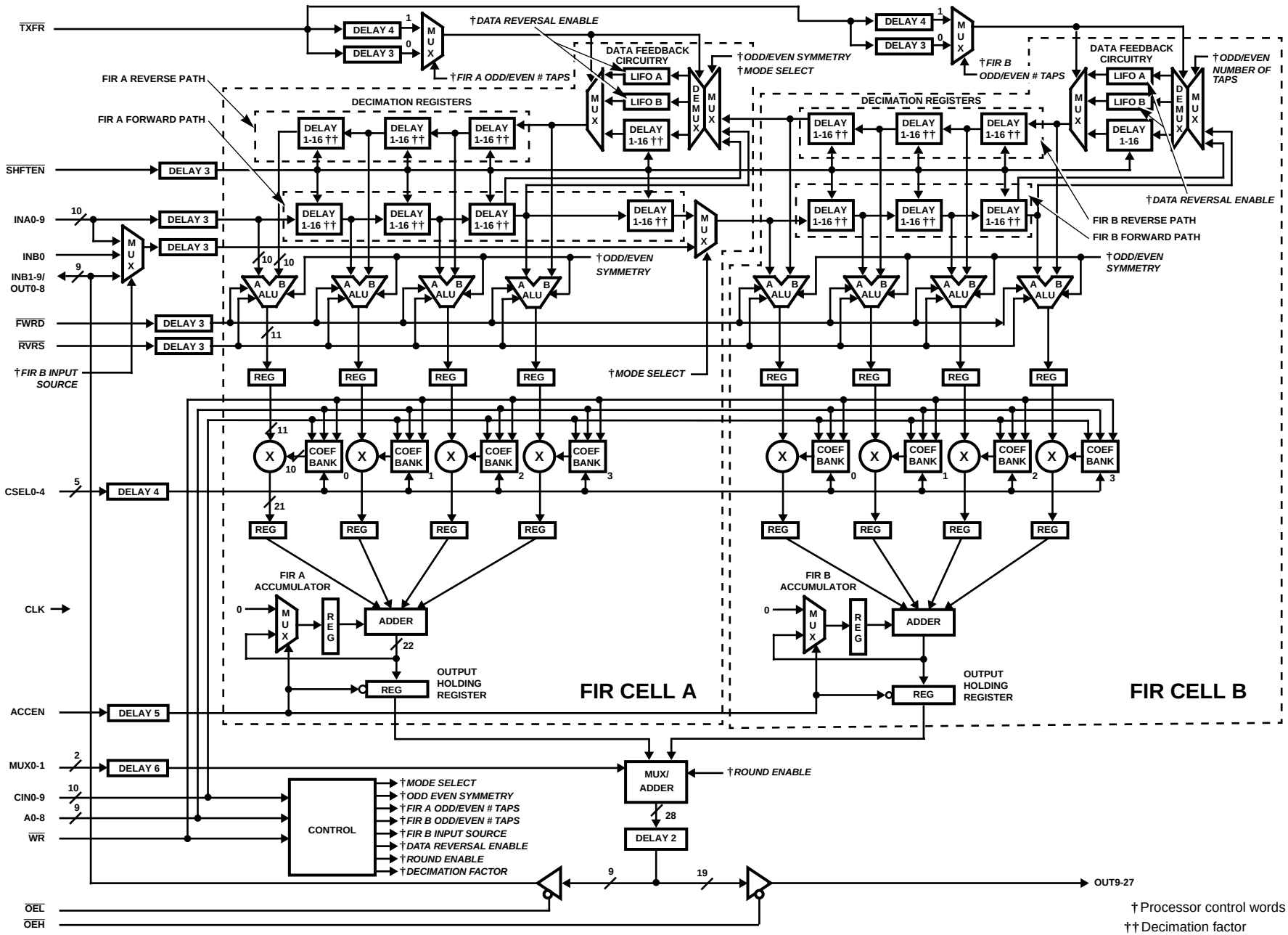


FIGURE 1. DUAL FIR FILTER

Functional Description

As shown in Figure 1, the HSP43168 consists of two 4-multiplier FIR filter cells which process 10-bit data and coefficients. The FIR cells can operate as two independent 8-tap FIR filters or two 4-tap asymmetric filters at maximum I/O rates. A single filter mode is provided which allows the FIR cells to operate as one 16-tap FIR filter or one 8-tap asymmetric filter. On board coefficient storage for up to 32 sets of 8 coefficients is provided. The coefficient sets are user selectable and are programmed through a microprocessor interface. Programmable decimation to 16 is also provided. By utilizing Decimation Registers together with the coefficient sets, polyphase filters are realizable which allow the user to trade data rate for filter taps. The MUX/Adder can be configured to either add or multiplex the outputs of the filter cells depending upon whether the cells are operating in single or dual filter mode. In addition, a shifter in the MUX/Adder is provided for implementation of filters with 10-bit data and 20-bit coefficients or vice versa.

Preparing the Dual FIR for Operation

Two configuration steps are required to prepare the Dual FIR Filter for normal operation: 1) loading the Configuration Control Registers, and 2) loading the FIR Filter Coefficients.

Configuration Control Registers are loaded by placing the control register address on address lines A0-8, placing the configuration data on the configuration input lines CIN0-9, and asserting the $\overline{WR}$ line (followed by a release of the assertion). This action creates a rising edge on the $\overline{WR}$ line, which clocks the address and configuration data into the part. The details of the “Load Configuration” process are outlined in the Microprocessor Interface Section.

FIR Coefficients are loaded by placing the address of the Coefficient Data Bank on the address lines A0-8, placing the FIR 10-bit coefficient values on the configuration input lines CIN0-9 and then asserting the $\overline{WR}$ line (followed by a release of the assertion). This action creates a rising edge on the $\overline{WR}$ line, which clocks the FIR Coefficient Band address and FIR Coefficient data into the part. The details of the “Load FIR Coefficient” process are outlined in the FIR Filter Cells Section, Coefficient Bank Subsection.

Both the Configuration Load and FIR Coefficient Load can be done as a sequence of asynchronous write commands to the Dual FIR Filter. Once these actions are complete, the part is ready for normal filter operation. The CLK, $\overline{TXFR}$, $\overline{FWRD}$, $\overline{RVRS}$, ACCEN, and SHFTEN signals must be asserted in a manner determined by the application. MUX0-1 must meet the setup and hold times with respect to clock for proper filter operation. Details of the MUX1-0 control can be found in the Output MUX/Adder Section. Details of the ACCEN control can be found in the Fir Cell Accumulator Section. Bit locations for the various filter control/configuration signals can be found in the Input/Output Formats Section.

The Dual FIR Filter has a “pipeline” delay of 8 CLK periods, once normal filtering operations begin. Five typical filtering operation examples are provided in the Applications Examples Section as a guide to configuration and control of the Dual FIR Filter.

During normal filter operations, the location and duration of the $\overline{TXFR}$ signal assertions are determined by the filter configuration and operation mode. Once set, these signal parameters must be maintained during normal operation to ensure proper data alignment in the part. Once the part is reset, do not change $\overline{TXFR}$ unless you load the configuration again.

NOTE: The fixed or periodic relationship between the $\overline{TXFR}$ signal and CLK must be maintained for valid filter operation. This relationship can only change when CLK is halted and new configuration control words are loaded into the device.

Microprocessor Interface

The Dual FIR has a 20 pin write only microprocessor interface for loading data into the Control Block and Coefficient Banks. The interface consists of a 10-bit data bus (CIN0-9), a 9-bit address bus (A0-8), and a write input ($\overline{WR}$) to latch the data into the on-board registers on a rising edge. The configuration control and coefficient data loading is asynchronous to CLK.

Control Block

The Dual FIR is configured by writing to the registers within the Control Block. Figure 2 shows the timing diagram for writing to the Configuration Control Registers. These Control Registers are memory mapped to Address 000H (H = Hexadecimal) and 001H on A0-8. The Filter Coefficient Registers are mapped to 1XXH (X = value described in the “Coefficient Banks” chapter of the ALU Section).

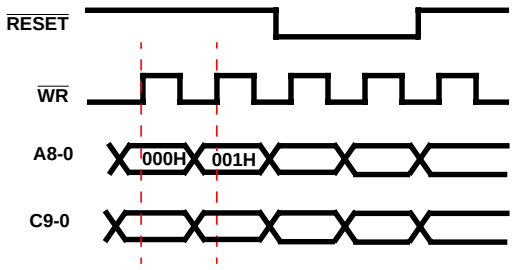


FIGURE 2. LATCHING C9-0 VALUES INTO ADDRESS A8-0 REGISTERS

The format of the Control Registers is shown in Table 1 and Table 2. Writing to any of the Control/Configuration Registers causes a reset which lasts for 6 CLK cycles following the assertion of $\overline{WR}$. The reset caused by Writing Registers in the Control Block will not clear the contents of the Coefficient

Bank. As shown in Figure 2, either Configuration Control Register can be written to during reset.

TABLE 1. CONFIGURATION/CONTROL WORD 0 BIT DEFINITIONS

CONTROL ADDRESS 000H		
BITS	**FUNCTION**	**DESCRIPTION**
3-0	Decimation Factor (N)	R = N + 1 0000 = No Decimation. 1111 = Decimation by 16.
4	Mode Select	0 = Single Filter Mode. 1 = Dual Filter Mode. (also 20-Bit Coefficient Filter)
5	Odd/Even Filter Coefficient Symmetry	0 = Even Symmetric Coefficients. 1 = Odd Symmetric Coefficients.
6	FIR A Odd/Even Number of Taps	0 = Odd Number of Taps in Filter. 1 = Even Number of Taps in Filter.
7	FIR B Odd/Even Number of Taps	(Defined Same as FIR A Above).
8	FIR B Input Source	0 = Input from INA0-9. 1 = Input from INB0-9.
9	Not Used	Set to 0 for Proper Operation.

NOTE: Address locations 002H to 011H are reserved, and writing to these locations will have unpredictable effects on part configuration.

TABLE 2. CONFIGURATION/CONTROL WORD 1 BIT DEFINITIONS

CONTROL ADDRESS 001H		
BITS	**FUNCTION**	**DESCRIPTION**
0	FIR A Input Format	0 = Unsigned. 1 = Two's Complement.
1	FIR A Coefficient Format	(Defined same as FIR A input).
2	FIR B Input Format	(Defined same as FIR A input).
3	FIR B Coefficient	(Defined same as FIR A input).
4	$\overline{\text{Data Reversal Enable}}$	0 = Enabled. 1 = Disabled.
8-5	Round Position	0000 = $2^{-10.}$ 1011 = $2^{1.}$ (See Figure 4)
9	Round Enable	0 = Enabled. 1 = Disabled.

NOTE: Address locations 002H to 011H are reserved, and writing to these locations will have unpredictable effects on part configuration.

The 4 LSBs of the control word loaded at address 000H are used to select the decimation factor. The Decimation Factor is programmed to one less than the number of delays between filter taps

$$DF = (CLK \text{ delays between taps}) - 1 \quad \text{(EQ. 1)}$$

For example, if the 4 LSBs are programmed with a value of 0010, the Forward and Reverse Shifting Decimation Registers are each configured with a delay of 3. Bit 4 is used to select whether the FIR cells operate as two independent filters or one extended length filter. Dual filter mode assumes Filter A and Filter B are separate independent filters. In the single filter mode, the data is routed through the forward paths of Filters A and B before entering the reverse paths of Filters A and B (see Figure 1). Coefficient symmetry is selected by bit 5. Bits 6 and 7 are programmed to configure the FIR cells for odd or even filter lengths (number of taps). Bit 8 selects the FIR B input source when the FIR cells are configured for independent operation. Bit 9 must be programmed to 0. ***NOTE: When the filter is programmed for even-taps, the $\overline{\text{TXFR}}$ signal is delayed by only three CLKS (see Figure 1). For odd-taps, the $\overline{\text{TXFR}}$ signal is delayed by four CLKS.***

The 4 LSBs of the control word loaded at address 001H are used to configure the format of the FIR cell's data and coefficients. Bit 4 is programmed to enable or disable the reversal of data sample order prior to entering the Reverse Path Decimation Registers. Data reversal is required for symmetric filter coefficient sets of both even or odd numbers of filter taps. Asymmetric filters and some decimated symmetric filters require the data reversal to be off. Bits 5-9 are used to support programmable rounding on the output.

FIR Filter Cells

Each FIR filter cell is based on an array of four 11x10-bit two's complement multipliers. One input of the multipliers comes from the ALU's which combine data shifting through the Forward and Reverse Decimation Registers. The second multiplier input comes from the user programmable coefficient bank. The multiplier outputs are fed to an accumulator whose result is passed to the output section where it is multiplexed or added with the result from the other FIR cell.

Decimation Registers

The Forward and Reverse Decimation Shift Registers can be configured for decimation factors from 1 to 16 (see Table 1, bits 0-3). ***NOTE: Setting the decimation factor only affects the Delay Registers between filter taps, not the filter control multiplexers.*** Example 4 and Example 5 in the Applications Section discuss how to configure the part for actual decimation applications.

The Reverse Shifting Registers with the data reversal logic are used to take advantage of symmetry in linear phase filters by aligning data at the ALUs for pre-addition prior to multiplication by the common coefficient. When the FIR cells are configured in single filter mode, the Decimation Registers in FIR cell A and FIR cell B are cascaded. This extended filter tap delay path allows computation of a filter which is twice the size of that capable using a single cell. The Decimation Registers also provide data storage for polyphase or 2-D filtering applications (See Applications Examples Section).

The Data Feedback Circuitry in each FIR cell is responsible for transferring data from the Forward to the Reverse Shifting Decimation Registers. This circuitry feeds blocks of samples into the reverse shifting decimation path in either reversed or non-reversed sample order. The MUX/DEMUX structure at the input to the Feedback Circuitry routes data to the LIFOs or the delay stage depending on the selected

configuration. The MUX on the Feedback Circuitry Output selects which storage element feeds the Reverse Shifting Decimation Registers.

In applications requiring reversal of sample order, the FIR cells are configured with data reversal enabled (see Table 2, CW5, bit 4 = 0). In this mode, data is transferred from the forward to the backward Shifting Registers through a pingponged LIFO structure. While one LIFO is being read into the backward shifting path, the other LIFO is written with data samples. The MUX/DEMUX controls which LIFO is being written, and the MUX on the Feedback Circuitry output controls which LIFO is being read. A low on $\overline{\text{TXFR}}$ and $\overline{\text{SHIFTEN}}$, switches the LIFOs being read and written, which causes the block of data to be read from the structure in reversed in sample order (See Example 4 in the Application Examples Section).

The frequency with which $\overline{\text{TXFR}}$ is asserted determines size of the data blocks in which sample order is reversed. For example, if $\overline{\text{TXFR}}$ is asserted once every three CLKs, blocks of 3 data samples with order reversed, would be fed into the Backward Decimation Registers. ***NOTE: Altering the frequency or phase of $\overline{\text{TXFR}}$ assertion once a filtering operation has begun will invalidate the filtering result.***

In applications which do not require sample order reversal, the FIR cells must be configured with data reversal disabled (see Table 2, CW5, bit 4 = 1). In addition, TXFR must be asserted to ensure proper data flow. In this configuration, data to the backward shifting decimation path is routed though a delay stage instead of the pingpong LIFOs. The number of registers in the delay stage is based on the programmed decimation factor. ***NOTE: Data reversal must be disabled and TXFR must be asserted for filtering applications which do not use decimation.***

The shifting of data through the Forward and Reverse Decimation Registers is enabled by asserting the $\overline{\text{SHFTEN}}$ input. When $\overline{\text{SHFTEN}}$ is high, data shifting is disabled, and the data sample latched into the part on the previous clock is the last input to the filter structure. The data sample at the filter input when $\overline{\text{SHFTEN}}$ is asserted, will be the next data sample into the forward decimation path.

When operating the FIR cells as two independent filters, FIR A receives input data via INA0-9 and FIR B receives data from either INA0-9 or INB0-9 depending on the application (see Table 1).

When the FIR cells are configured as a single extended length filter, the forward and reverse decimation paths of the two FIR cells are cascaded. In this mode, data is transferred from the forward decimation path to the reverse decimation path by the Data Feedback Circuitry in FIR B. Thus, the manner in which data is read into the reverse decimation path is determined by FIR B's configuration. When the decimation paths are cascaded, data is routed through the fourth delay stage in FIR A's forward path to FIR B.

The configuration of the FIR cells as even or odd length filters determines the point in the forward decimation path from which data is multiplexed to the Data Feedback Circuitry. For example, if the FIR cell is configured as an odd length filter, data prior to the last register in the third forward decimation stage is routed to the Feedback Circuitry. If the FIR cell is configured as an even length filter, data output from the third forward decimation stage is multiplexed to the Feedback Circuitry. This is required to ensure proper data alignment with symmetric filter coefficients (See Application Examples).

ALUs

Data shifting through the forward and reverse decimation paths feed the “a” and “b” inputs of the ALUs respectively. The ALUs perform an “b+a” operation if the FIR cell is configured for even symmetric coefficients or an “b-a” operation if configured for odd symmetric coefficients. Control Word 0, Bit 5 is used to set the ALU operation.

For applications in which a pre-add or subtract is not required, the “a” or “b” input can be zeroed by disabling $\overline{\text{FWRD}}$ or $\overline{\text{RVRS}}$ respectively. This has the effect of producing an ALU output which is either “a”, “-a”, or “b” depending on the filter symmetry chosen. For example, if the FIR cell is configured for an even symmetric filter with $\overline{\text{FWRD}}$ low and $\overline{\text{RVRS}}$ high, the data shifting through the Forward Decimation Registers would appear on the ALU output.

Table 3 details the ALU configurations, where “a” is the ALU data input from the front decimation delay registers and “b” is the ALU data from the back decimation delay registers.

TABLE 3. ALU CONFIGURATIONS

ALU OUT	SYMMETRY	$\overline{\text{FWD}}$	$\overline{\text{RVS}}$	DESCRIPTION
a+b	0 (Even)	0	0	Even Number of Taps, Even Symmetry (Example 1)
+b	0 (Even)	0	1	Even Symmetry
+a	0 (Even)	1	0	Even Symmetry
-	0 (Even)	1	1	Even Symmetry
b-a	1 (Odd)	0	0	Even Number of Taps, Odd Symmetry (Example 2)
+b	1 (Odd)	0	1	Odd Symmetry
-a	1 (Odd)	1	0	Odd Symmetry
-	1 (Odd)	1	1	Odd Symmetry

Coefficient Bank

The output of the ALU is multiplied by a coefficient from one of 32 user programmable coefficient sets. Each set consists of 8 coefficients (4 coefficients for FIR A and 4 for FIR B). CSEL0-4 is used to select a coefficient set to be used. Coefficient sets may be switched every clock to support polyphase filtering operations.

The coefficients are loaded into On-Board Registers using the microprocessor interface, CIN0-9, A0-8, and $\overline{\text{WR}}$. Each multiplier within the FIR Cells is driven by a coefficient bank

with one of 32 coefficients. These coefficients are addressed as shown in Table 4. The inputs A0-1 specify the Coefficient Bank for one of the four multipliers in each FIR Cell; A2 specifies FIR Cell A or B; Bits A7-3 specify one of 32 sets in which the coefficient is to be stored. For example, an address of 10dH would access the coefficient for the second multiplier in FIR B in the second coefficient set.

TABLE 4. FIR COEFFICIENT WRITE ADDRESSES

FIR COEFF.	CSEL (4-0) COEFF. SET	CELL A/B	MULTIPLIER	DESTINATION	
A8	A7-3	A2	A1-0	FIR	BANK
1	xxxx x	0	00	A	0
1	xxxx x	0	01	A	1
1	xxxx x	0	10	A	2
1	xxxx x	0	11	A	3
1	xxxx x	1	00	B	0
1	xxxx x	1	01	B	1
1	xxxx x	1	10	B	2
1	xxxx x	1	11	B	3

FIR Cell Accumulator

The registered outputs from the multipliers in each FIR cell feed an accumulator. The ACCEN input controls each accumulator's running sum and the latching of data from the accumulator into the Output Holding Registers. When ACCEN is low, feedback from the accumulator adder is zeroed which disables accumulation. Also, output from the accumulator is latched into the Output Holding Registers. When ACCEN is asserted, accumulation is enabled and the contents of the Output Holding Registers remain unchanged.

Output MUX/Adder

The contents of each FIR Cell's Output Holding Register is summed or multiplexed in the Mux/Adder. The operation of the Mux/Adder is controlled by the MUX1-0 inputs as shown in Table 5. Applications requiring 10-bit data and 20-bit coefficients or 20-bit data and 10-bit coefficients are made possible by configuring the MUX/Adder to scale FIR B's output by 2^{-10} prior to summing with FIR A. When the Dual FIR is configured as two independent filters, the MUX1-0 inputs would be used to multiplex the filter outputs of each cell. For applications in which FIR A and B are configured as a single filter, the MUX/Adder is configured to sum the output of each FIR cell.

NOTE: While a 20-bit coefficient filter is a single filter, the mode select is set to 1 and MUX1-0 is set to 00.

TABLE 5. MUX1-0 BIT DEFINITIONS

MUX1-0 DECODING	
MUX1-0	OUT0-27
00	FIRA + FIRB (FIR B Scaled by 2^{-10})
01	FIRA + FIRB
10	FIRA
11	FIRB

Input/Output Formats

The Dual FIR supports mixed mode arithmetic with both unsigned and two's complement data and coefficients. The input and output formats for both data types are shown below. If the Dual FIR is configured as an even symmetric filter with unsigned data and coefficients, the output will be unsigned. Otherwise, the output will be two's complement.

The MUX/Adder can be configured to implement programmable rounding at bit locations 2^{-10} through 2^{1}. The round is implemented by adding a 1 to the specified location (see Table 2). Figure 4 illustrates the rounding operation. For example, to configure the part such that the output is rounded to the 10 MSBs, OUT18 - 27, the round position would be chosen to be 2^{-1}. The negative sign on the MSB indicates 2's complement format.

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL TWO'S COMPLEMENT

9	8	7	6	5	4	3	2	1	0
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL TWO'S COMPLEMENT

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
-2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL TWO'S COMPLEMENT

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL UNSIGNED

9	8	7	6	5	4	3	2	1	0
2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL UNSIGNED

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL UNSIGNED

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

FIGURE 3. INPUT/OUTPUT FORMAT DEFINITIONS

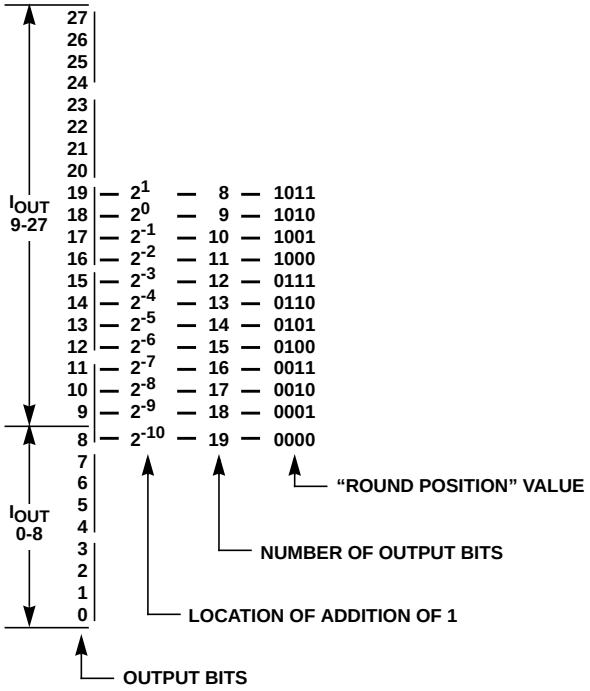


FIGURE 4. ROUND POSITION BIT DEFINITION

Application Examples

In this section a number of examples are presented which detail even, odd, symmetric, asymmetric, decimating and dual FIR filter configurations. These examples are intended to illustrate the different operational features of the HSP43168 and should be used as a guide in developing an application specific filter configuration. Use Table 6 to select and find the example that best matches your application.

TABLE 6. FILTER EXAMPLE SELECTION GUIDE

FILTER TYPE	EXAMPLE NUMBER
Even Tap Even Symmetric	1
Odd Tap Even Symmetric	2
Asymmetric	3
Even Tap Decimating	4
Odd Tap Decimating	5
Dual Decimating	6

Examples 1-5 are explained using a single four tap FIR cell, but the same concept applies to FIR filters which use both FIR cells (A and B) in a single filter configuration. Example 6 details a dual filter mode where FIR cell A and B implement different digital filters. All examples are functionally verified configurations. Each example details a complete design solution, including a block diagram, a data/coefficient alignment illustration, a data flow diagram and a control signal timing diagram.

Two programmable Configuration Control Registers define a unique FIR filter configuration. Register 000H has all filter configuration unique parameters, while Register 001H, bit 4, is filter configuration unique. Table 7 details the configuration control register values, the number of filter coefficient banks required and the MUX1-0 control values for each filter example.

TABLE 7. CONFIGURATION CONTROL REGISTER VALUES

FILTER TYPE	REG 000 HEX	REG 001 HEX	# OF FILTER COEFFICIENT BANKS	MUX 1-0
Even Tap Even Symmetric	1d0	010	1	10
Odd Tap Even Symmetric	110	010	1	10
Asymmetric	110	010	2	10
Even Tap Decimate by N+1	1dN	000	N+1	10
Odd Tap Decimate by N+1	11N	000	N+1	10
Dual: Even and Odd Tap Decimate by N+1	15N or 19N	000 ↑ Bit 4	N+1	10 and 11

Example 1. Even-Tap Even Symmetric Filter Example

The HSP43168 may be configured as two independent 8-tap symmetric filters as shown by the Block Diagram in Figure 5. Each of the FIR cells takes advantage of symmetric filter coefficients by pre-adding data samples common to a given coefficient. As a result, each FIR cell can implement an 8-tap symmetric filter using only four multipliers. Similarly, when the HSP43168 is configured in single filter mode a 16-tap symmetric filter is possible by using the multipliers in both cells.

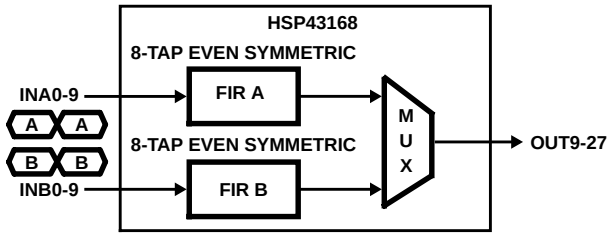


FIGURE 5. USING HSP43168 AS TWO INDEPENDENT FILTERS

The operation of the FIR cell is better understood by comparing the data and coefficient alignment for a given filter output, Figure 6, with the data flow through the FIR cell, as shown in Figure 7. The Block Diagrams in Figure 7 are a simplification of the FIR cell shown in Figure 1. For simplicity, the ALUs and FIR Cell Accumulators were replaced by adders, and the Pipeline Delay Registers were omitted. In this example, we will only show the data flow through one of the two FIR cells.

In Figure 7, the order of the data samples within the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is

given by the equation at the bottom of each block diagram. Figure 7A shows the data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 6.

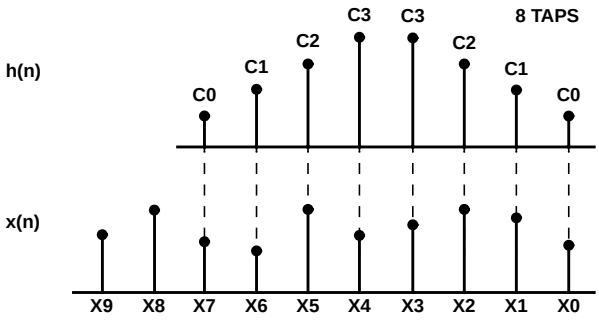


FIGURE 6. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP EVEN SYMMETRIC FILTER

The dual filter application is configured by writing 1d0H to address 000H via the microprocessor interface, CIN0-9, A0-8, and $\overline{WR}$. Since this application does not use decimation, the 4th bit of the Control Register at Address 001H must be set to disable data reversal (see Table 2). Failure to disable data reversal will produce erroneous results.

Using this architecture, only the unique coefficients need to be stored in the Coefficient Bank. For example, the above filter would be stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to Address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H.

To operate the HSP43168 in this mode, $\overline{TXFR}$ is tied low to ensure proper data flow; both $\overline{FWRD}$ and $\overline{RVRS}$ are tied low to enable data samples from the forward and reverse data paths to the ALUs for pre-adding; ACCEN is tied low to prevent accumulation over multiple CLKs; $\overline{SHFTEN}$ is tied low to allow shifting of data through the Decimation Registers; MUX0-1 is programmed to multiplex the output the of either FIR A or FIR B; CSEL0-4 is programmable to access the stored coefficient set, in this example CSEL = 00000.

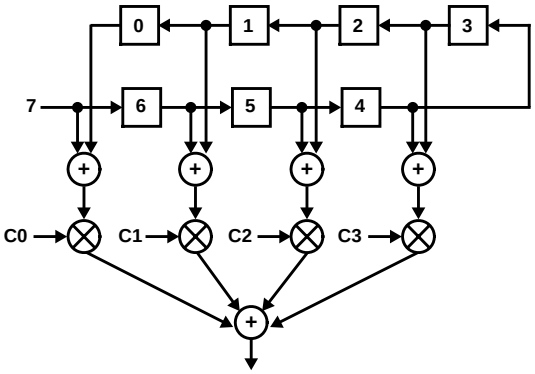


FIGURE 7A. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE

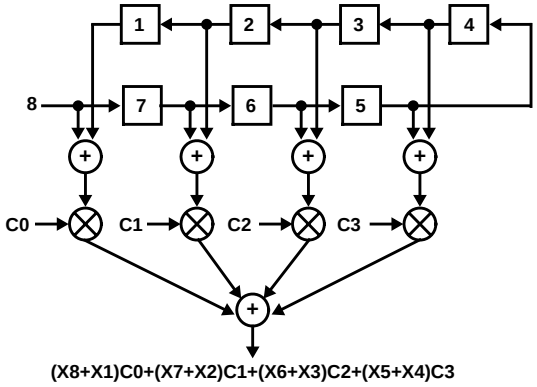


FIGURE 7B. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE

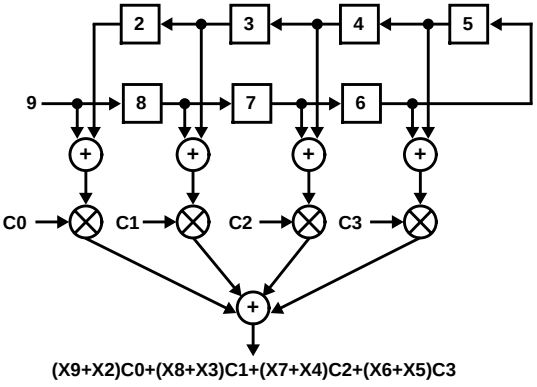


FIGURE 7C. DATA FLOW AS DATA SAMPLE 9 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 7. DATA FLOW DIAGRAMS FOR 8-TAP SYMMETRIC FILTER

Example 2. Odd-Tap Even Symmetric Filter Example

The HSP43168 may be configured as two independent 7-tap symmetric filters with a Functional Block Diagram shown in Figure 8. Again, this example shows data flow through one of the two FIR cells. As in the 8-tap filter example, the HSP43168 implements the filtering operation by summing data samples sharing a common coefficient prior to multiplication by that coefficient. However, for odd length filters the pre-addition requires that the center coefficient be scaled by 1/2.

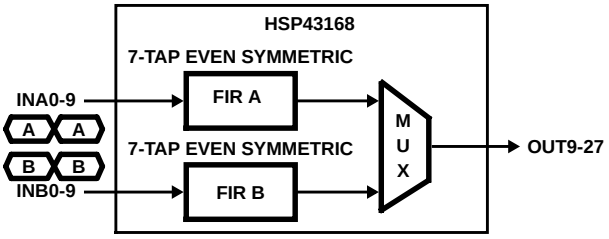


FIGURE 8. USING HSP43168 AS TWO INDEPENDENT FILTERS

The operation of the FIR cell for odd length filters is better understood by comparing the data/coefficient alignment in Figure 9 with the Data Flow Diagrams in Figure 10. The Block Diagrams in Figure 10 are a simplification of the FIR cell shown in Figure 1.

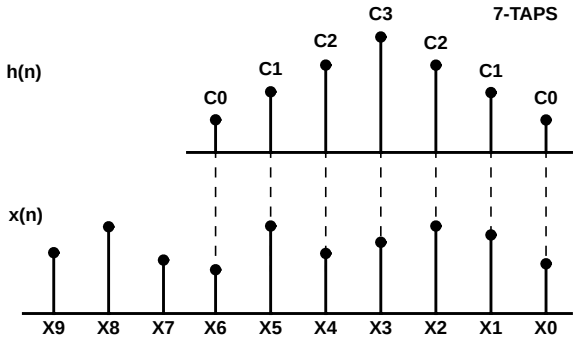


FIGURE 9. DATA/COEFFICIENT ALIGNMENT FOR 7-TAP SYMMETRIC FILTER

For odd length filters, proper data/coefficient alignment is ensured by routing data entering the last register in the third forward decimation stage to the Backward Shifting Registers. In this configuration, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from both the Forward and Backward Shifting Registers.

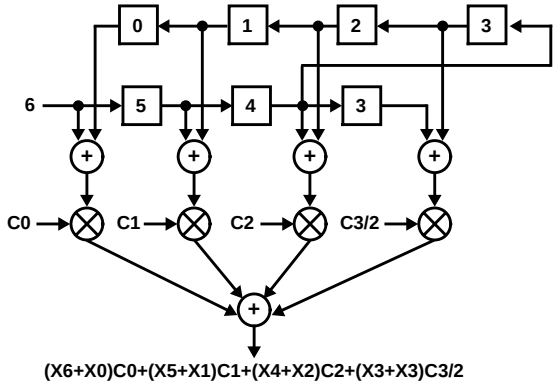


FIGURE 10A. DATA FLOW AS DATA SAMPLE 6 IS CLOCKED INTO THE FEED FORWARD STAGE

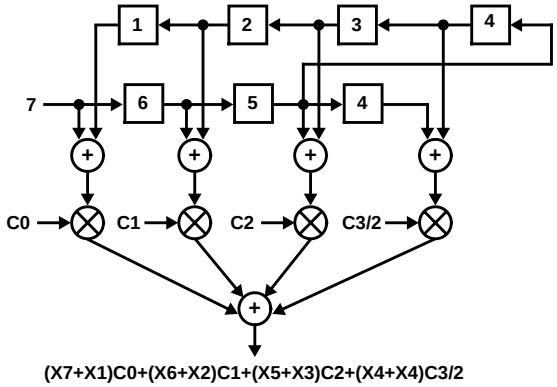


FIGURE 10B. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE

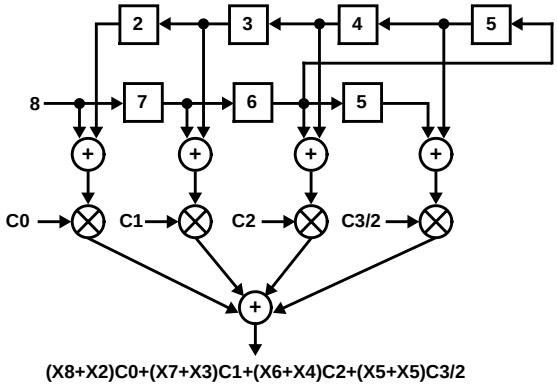


FIGURE 10C. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 10. DATA FLOW DIAGRAMS FOR 7-TAP SYMMETRIC FILTER

In the Data Flow Diagrams of Figure 10, the order of the data samples input in to the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of the block. The Diagram in Figure 10A shows data sample alignment at the pre-adders for the Data/Coefficient Alignment shown in Figure 9.

This dual filter application is configured by writing 110H to Address 000H via the microprocessor interface, CIN0-9, A0-8, and WR. Also, data reversal must be disabled by setting bit 4 of the Control Register at Address 0001H. As in the 8-tap example, only the unique coefficients need to be stored in the Coefficient Bank. These coefficients are stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to Address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H. The control signals TXFR, FWRD, RVRS, ACCEN, SHFTEN, and CSEL0-4 are controlled as described in Example 1.

Example 3. Asymmetric Filter Example

The FIR cells within the HSP43168 can each calculate 4 asymmetric taps on each clock. Thus, a single FIR cell can implement an 8-tap asymmetric filter if the HSP43168 is clocked at twice the input data rate. Similarly, if the Dual is configured as a single filter, a 16-tap asymmetric filter is realizable. Only one of the two FIR cells are used in this example for the Block Diagram shown in Figure 11.

For this example, the FIR cells are configured as two 8-tap asymmetric filters which are clocked at twice the input data rate. New data is shifted into the forward and backward decimation paths every other CLK by the assertion of $\overline{\text{SHFTEN}}$. The filter output is computed by passing data from each decimation path to the multipliers on alternating clocks. Two sets of coefficients are required, one for data on the forward decimation path, and one for data on the reverse path. The filter output is generated by accumulating the multiplier outputs for two CLKs.

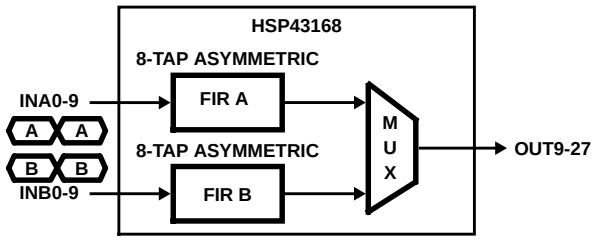


FIGURE 11. USING HSP43168 AS TWO INDEPENDENT FILTERS

The operation of this configuration is better understood by comparing the Data/Coefficient Alignment in Figure 12 with the Data Flow Diagrams in Figure 13. The ALUs have been omitted from the FIR cell diagrams because data is fed to the multipliers directly from the forward and reverse decimation paths. The data samples within the FIR cell are shown by the numbers in the decimation paths.

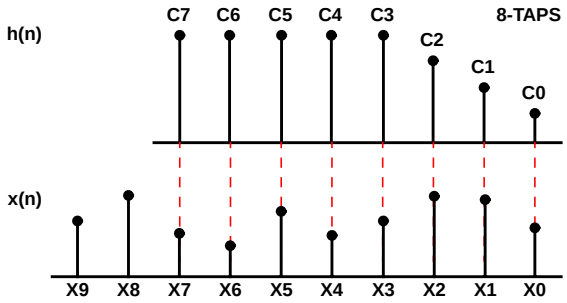


FIGURE 12. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP ASYMMETRIC FILTER

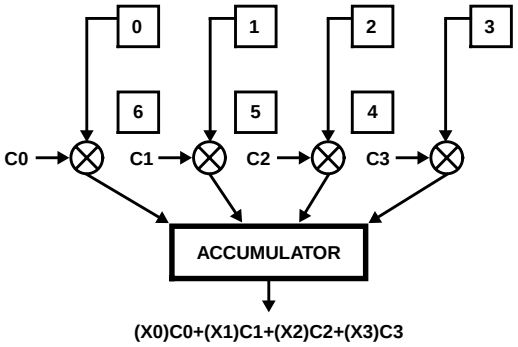


FIGURE 13A. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS

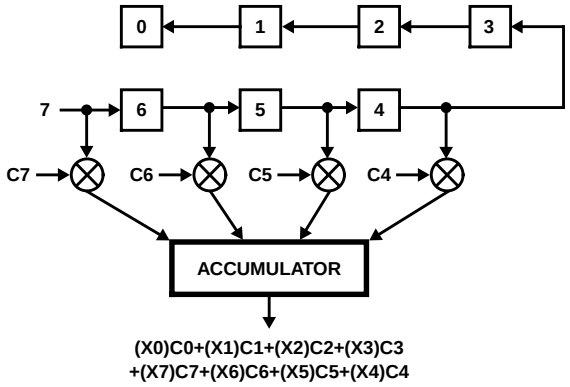


FIGURE 13B. SHIFTING OF DATA SAMPLE 7 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS

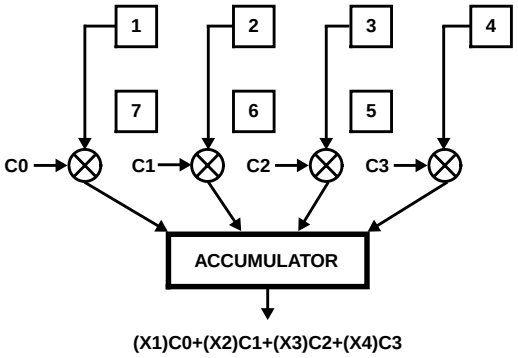


FIGURE 13C. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS

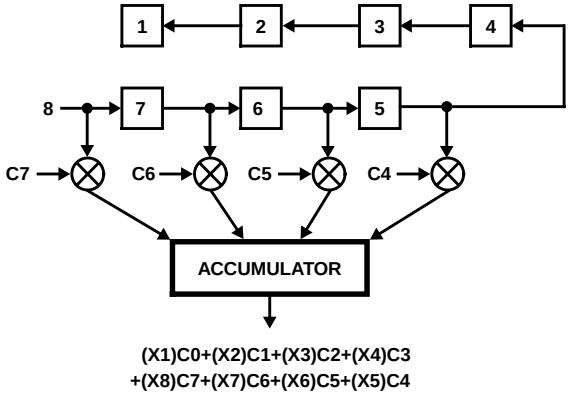
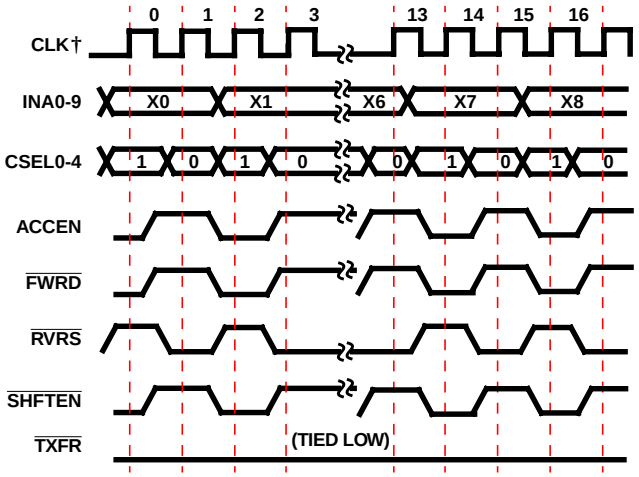


FIGURE 13D. SHIFTING OF DATA SAMPLE 8 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS

FIGURE 13. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER

For this application, each filter cell is configured as an odd length filter by writing 110H to the Control Register at Address 000H. Even though an even tap filter is being implemented, the filter cells must be configured as odd length to ensure proper data flow. In addition, the filters must be set to even symmetry. Also, the 4th bit at Control Address 001H must be set to disable data reversal, and TXFR must be tied low. Since an 8-tap asymmetric filter is being implemented, two sets of coefficients must be stored. These eight coefficients could be loaded into the first two coefficient sets for FIR A by writing C0, C1, C2, C3, C7, C6, C5, and C4 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, and 10bH respectively.

The sum of products required for this 8-tap filter require dynamic control over $\overline{\text{FWRD}}$, $\overline{\text{RVRS}}$, ACCEN, and CSEL0-4. The relative timing of these signals is shown in Figure 14.



†Note that CLK is 2X data rate.

FIGURE 14. CONTROL TIMING FOR 8-TAP ASYMMETRIC FILTER

Example 4. Even-Tap Decimating Filter Example

The HSP43168 supports filtering applications requiring decimation to 16. In these applications the output data rate is reduced by a factor of N. As a result, N clock cycles can be used for the computation of the filter output. For example, each FIR cell can calculate 8 symmetric or 4 asymmetric taps in one clock. If the application requires decimation by two, the filter output can be calculated over two clocks thus, boosting the number of taps per FIR cell to 16 symmetric or 8 asymmetric. For this example, each FIR cell is configured as an independent 24-tap decimate x3 filter. Again, the data flow diagrams show only one of the FIR cells shown in Figure 15.

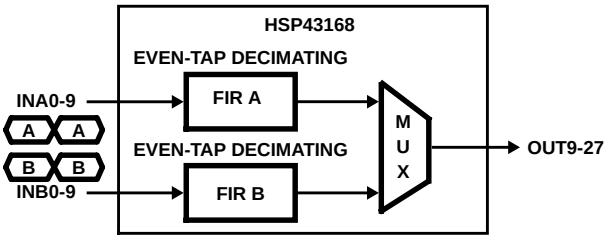


FIGURE 15. EVEN-TAP DECIMATING FILTER, 24-TAP DEC = 3

The alignment of data relative to the 24 filter coefficients for a particular output is depicted graphically in Figure 16. As in previous examples, the HSP43168 implements the filtering operation by summing data samples prior to multiplication by the common coefficient. In this example an output is required every third CLK which allows 3 CLKs for computation. On each CLK, one of three sets of coefficients are used to calculate 8 of the filter taps. The Block Diagrams in Figure 17 show the data flow and accumulator output for the data/coefficient alignment in Figure 16.

Proper data and coefficient alignment is achieved by asserting $\overline{\text{TXFR}}$ once every three CLKs to switch the LIFOs which are being read and written. This has the effect of feeding blocks of three samples into the backward shifting decimation path which are reversed in sample order. In addition, ACCEN is deasserted once every three clocks to allow accumulation over three CLKs. The three sets of coefficients required in the calculation of a 24-tap symmetric filter are cycled through using CSEL0-4. The timing relationship between the CSEL0-4, ACCEN, and $\overline{\text{TXFR}}$ are shown in Figure 18.

To operate in this mode the Dual is configured by writing 1d2 to Address 000H via the microprocessor interface, CIN0-9, A0-8, and WR. Data reversal must be enabled see (Table 2). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, C11, C1, C4, C7, C10, C0, C3, C6, and C9 to Address [100H, 101H, 102H, 103H], CSEL = 0; [108H, 109H, 10aH, 10bH], CSEL = 1; [110H, 111H, 112H, and 113H], CSEL = 2, respectively.

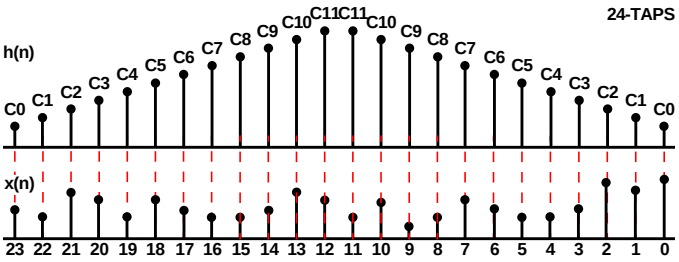


FIGURE 16. DATA/COEFFICIENT ALIGNMENT FOR 24-TAP DECIMATE BY 3 FIR FILTER

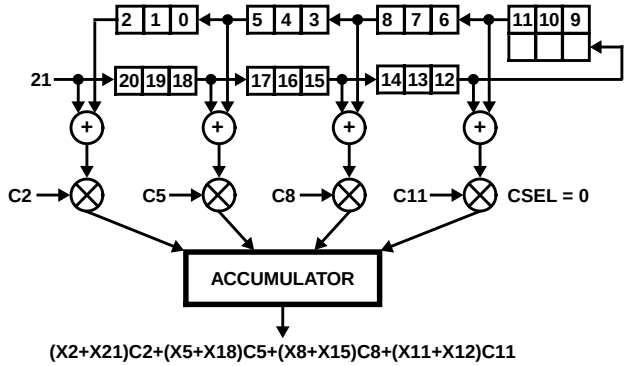


FIGURE 17A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE

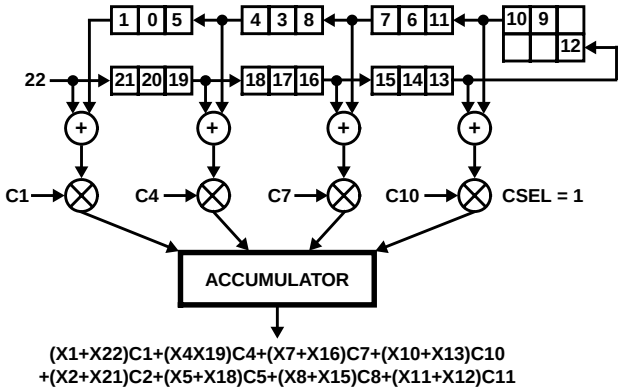


FIGURE 17B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE

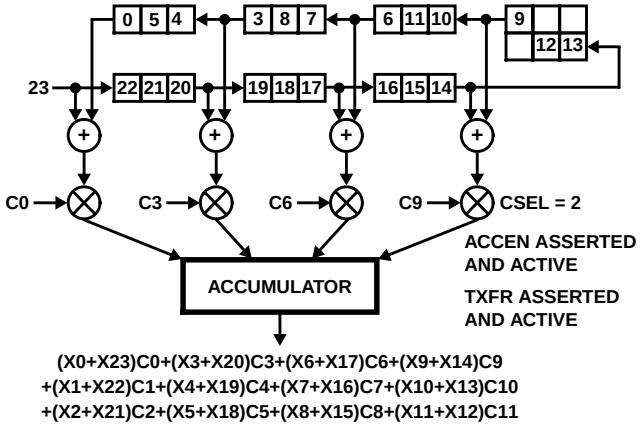


FIGURE 17C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

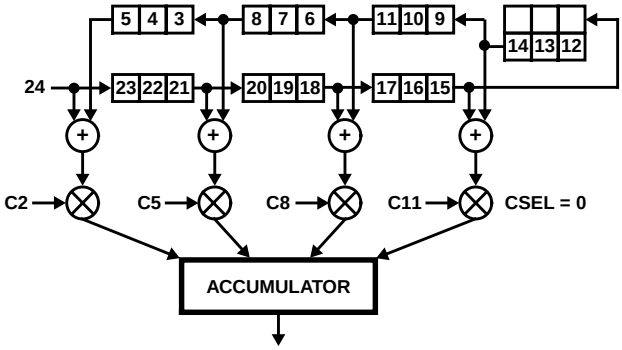
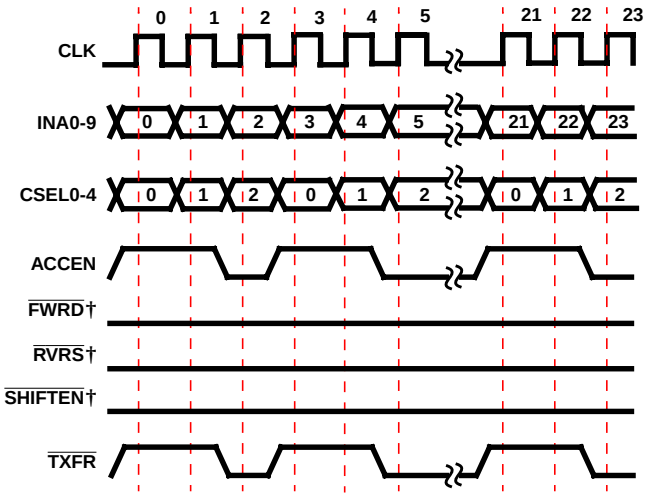


FIGURE 17D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 17. DATA FLOW DIAGRAMS FOR 24-TAP DECIMATED BY 3 FIR FILTER



†Tied low.

FIGURE 18. CONTROL SIGNAL TIMING FOR 24-TAP DECIMATE X3 FILTER

Example 5. Odd-Tap Decimating Symmetric Filter

This example highlights the use of the HSP43168 as two independent, 23-tap, symmetric, decimate by 3 filters. In this example, the operational differences in the control signals and data reversal structure may be compared to the previously discussed even-tap decimating filter. Figure 19 shows two FIR cells. The data flow in this example uses only one of the FIR cells.

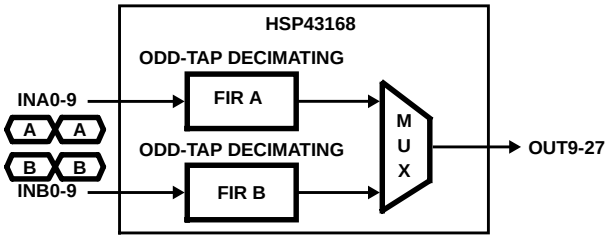


FIGURE 19. USING HSP43168 AS TWO INDEPENDENT FILTERS

As in the 24-tap example, an output is required every third CLK which allows 3 CLKs for computation. On each CLK, one of three sets of coefficients are used to calculate the filter taps. Since this is an odd length filter, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from the forward and backward shifting decimation paths. The Block Diagrams in Figure 20 show the data flow, and the accumulator output for the data coefficient alignment is shown in Figure 21.

Proper data and coefficient alignment is achieved by asserting TXFR once every three CLKs to switch the LIFOs which are being read and written. In the odd-tap mode, TXFR is internally delayed by one clock cycle with respect to ACCEN so that the convolutional sum will be computed correctly. For odd length filters, data prior to the last register in the forward decimation path is routed to the feedback circuitry. As a result, TXFR should be asserted one cycle prior to the input data samples which align with the center tap. The timing relationship between the CSEL0-5, ACCEN, and TXFR are shown in Figure 22.

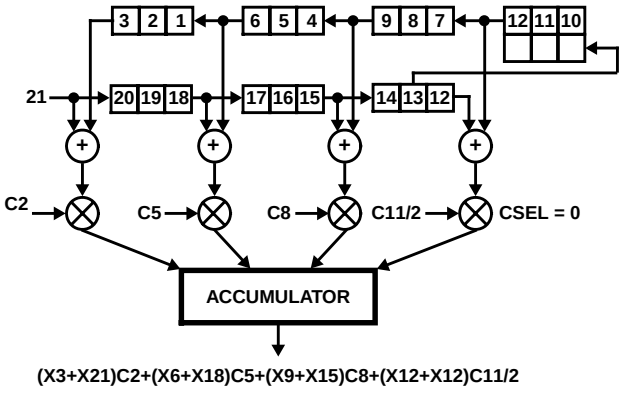


FIGURE 20A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE $\overline{\text{TXFR}}$ TAKES AFFECT ON THIS CLOCK CYCLE

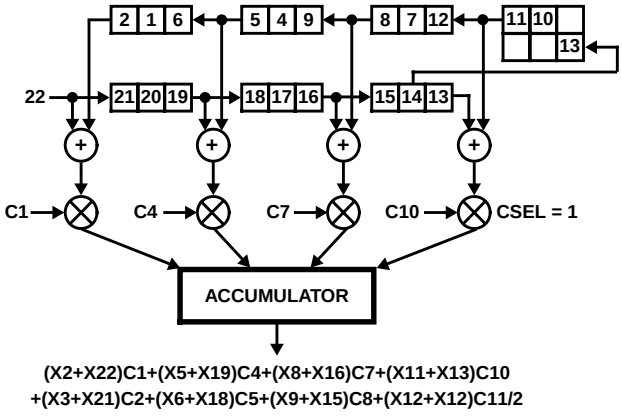


FIGURE 20B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE

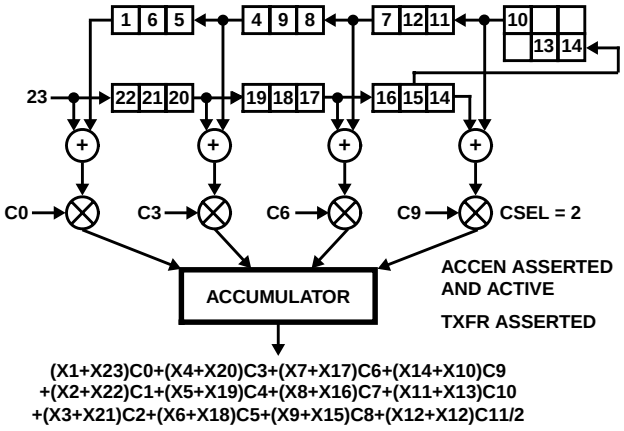


FIGURE 20C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

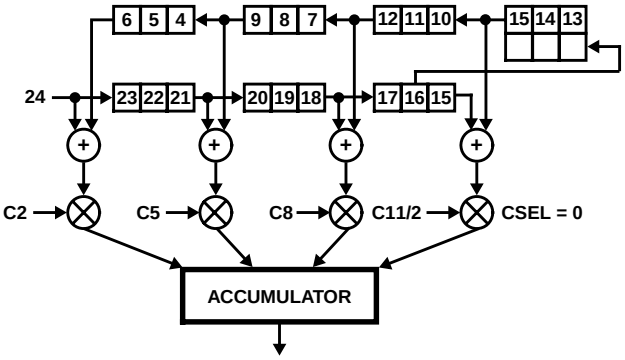


FIGURE 20D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE $\overline{\text{TXFR}}$ TAKES AFFECT ON THIS CLOCK CYCLE

FIGURE 20. DATA FLOW DIAGRAMS FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER

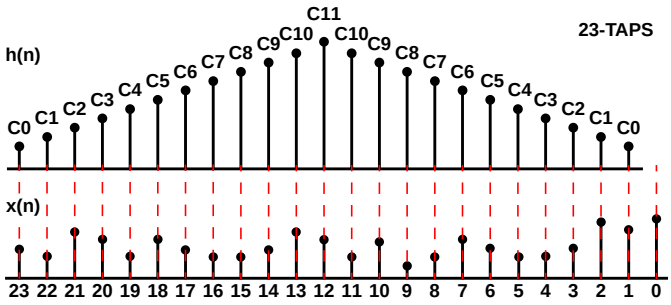
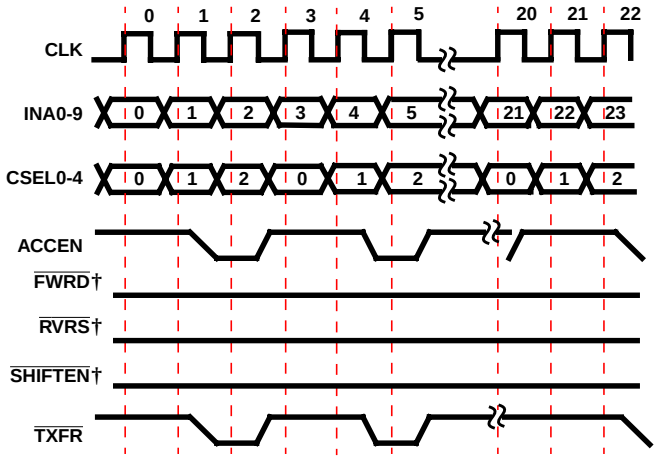


FIGURE 21. DATA/COEFFICIENT ALIGNMENT FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER



†Tied low.

FIGURE 22. CONTROL SIGNAL TIMING FOR 23-TAP SYMMETRIC FILTER

To operate in this mode, the Dual is configured by writing 112H to Address 000H via the microprocessor interface, CIN0-9, A0-8, and $\overline{WR}$. Data reversal must be enabled (see Table 2). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing [C2, C5, C8, (C11)/ 2], CSEL = 0; [C1, C4, C7, C10], CSEL = 1; [C0, C3, C6, and C9], CSEL = 2; to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H, respectively.

Example 6. Dual Decimation Example

The purpose of this example is to give an overview of one of the more complex applications of the HSP43168. The input is two data streams (A) and (B) samples. Figure 23 shows the upper level block diagram of the system being implemented. The decimation rate was set to N. N-1 is loaded into the decimation factor in Control Word 000H.

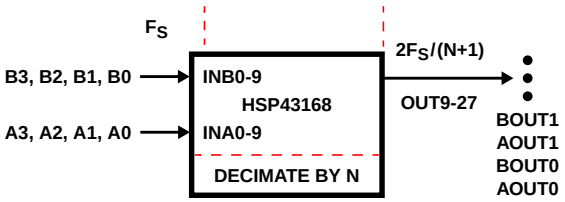


FIGURE 23. MULTIPLEXED DECIMATION BLOCK DIAGRAM

To demonstrate the muxed decimation, lets suppose that the application requires filter A to be configured as an even-decimate-by-3 filter and filter B to be configured as a odd-decimate-by-3 filter. The output data is made of the two decimated data streams multiplexed together and has a data rate equal to 2 times the input sampling rate divided by the decimation factor. Figure 24 shows the data/coefficient alignment for FIR A and FIR B.

To operate in this mode, Control Word 000H must be written with a 0x152. Data reversal must be enabled by setting bit 4 of Control Word 001H = 0. The filter set selected by CSEL0-4 = 0 should be loaded by writing C2, C5, C8, C11, D2, D5, D8, and (D11)/ 2 into 100H, 101H, 102H, 103H, 104H, 105H, 106H, and 107H. The filter set selected by CSEL0-4 = 1 should be loaded by writing C1, C4, C7, C10, D1, D4, D7, and D10 into 108H, 109H, 10aH, 10bH, 10cH, 10dH, 10eH, and 10fH. The filter set selected by CSEL0-4 = 2 should be loaded by writing C0, C3, C6, C9, D0, D3, D6, and D9 into 110H, 111H, 112H, 113H, 114H, 115H, 116H, and 117H.

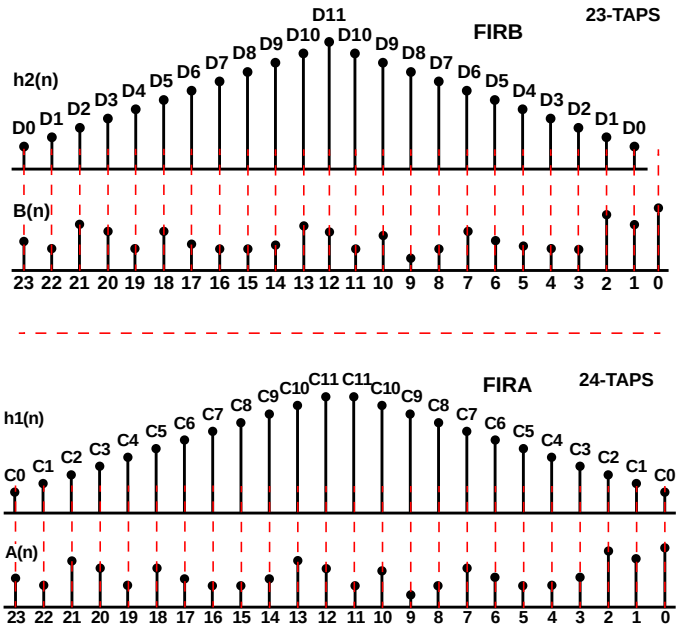


FIGURE 24. DATA/COEFFICIENT ALIGNMENT FOR MULTIPLEXED DECIMATION EXAMPLE

Figure 25 shows the Timing Diagram required to obtained the multiplexed/decimated output. The output of the two filters are provided at by selecting the odd-decimation filter first, then the even-decimation second using MUX0-1. Figure 26 shows the Data Flow Diagram for the multiplexed decimation example.

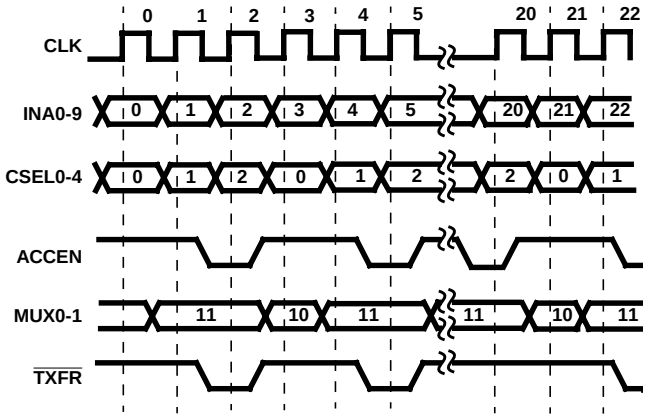


FIGURE 25. TIMING DIAGRAM FOR MULTIPLEXED DECIMATION EXAMPLE

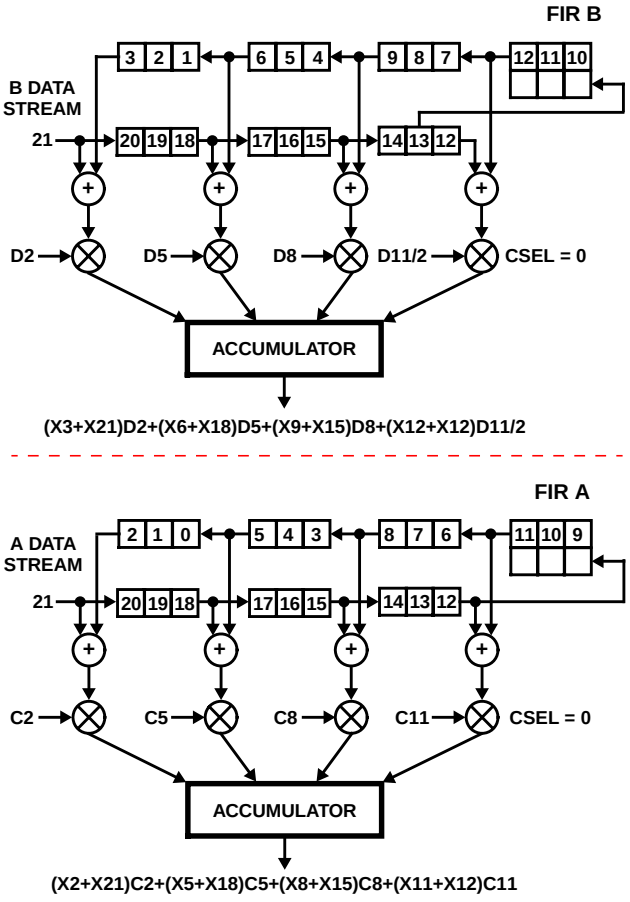


FIGURE 26A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE

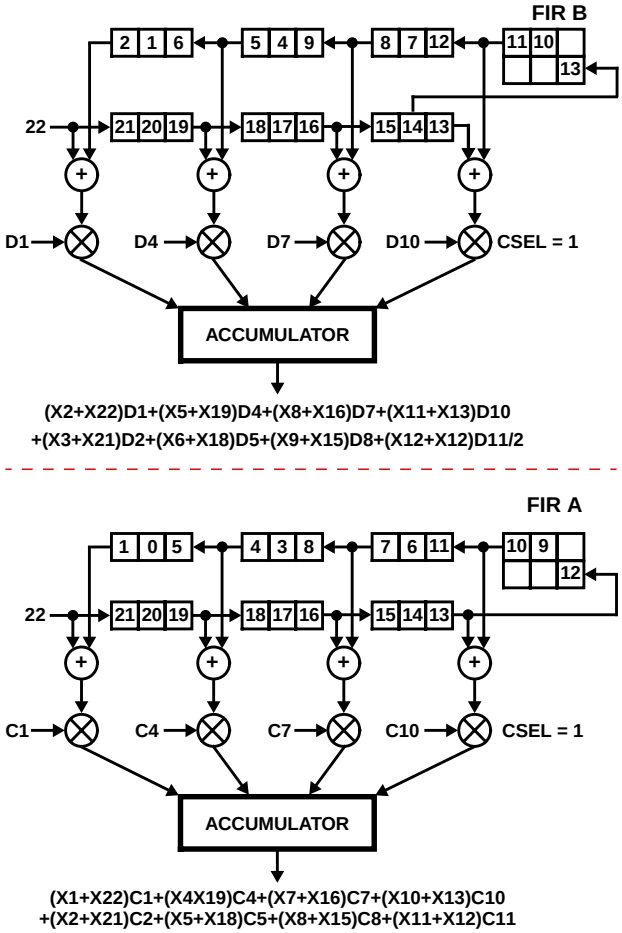


FIGURE 26B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE

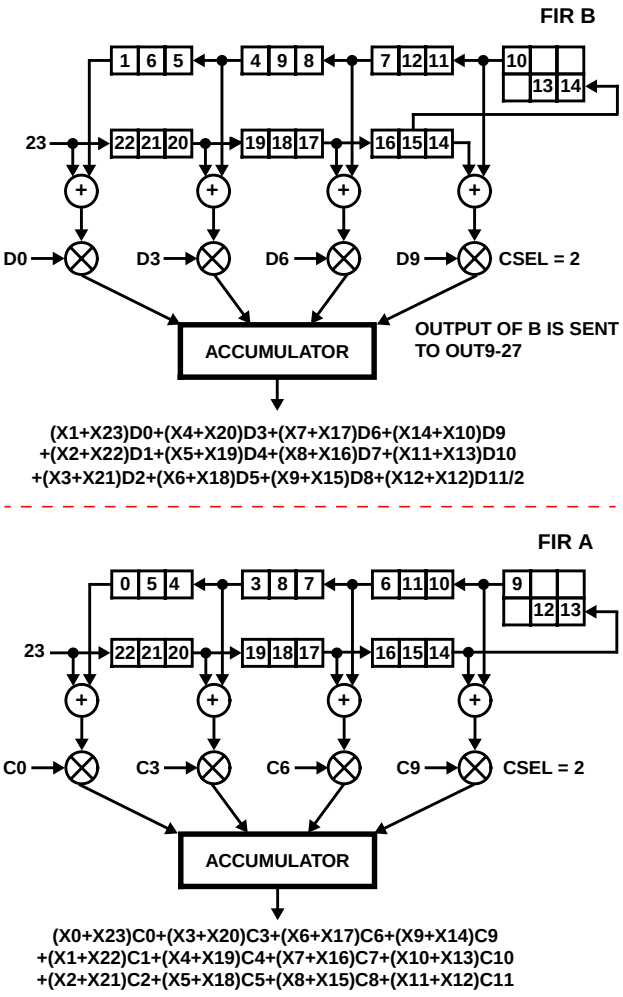


FIGURE 26C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

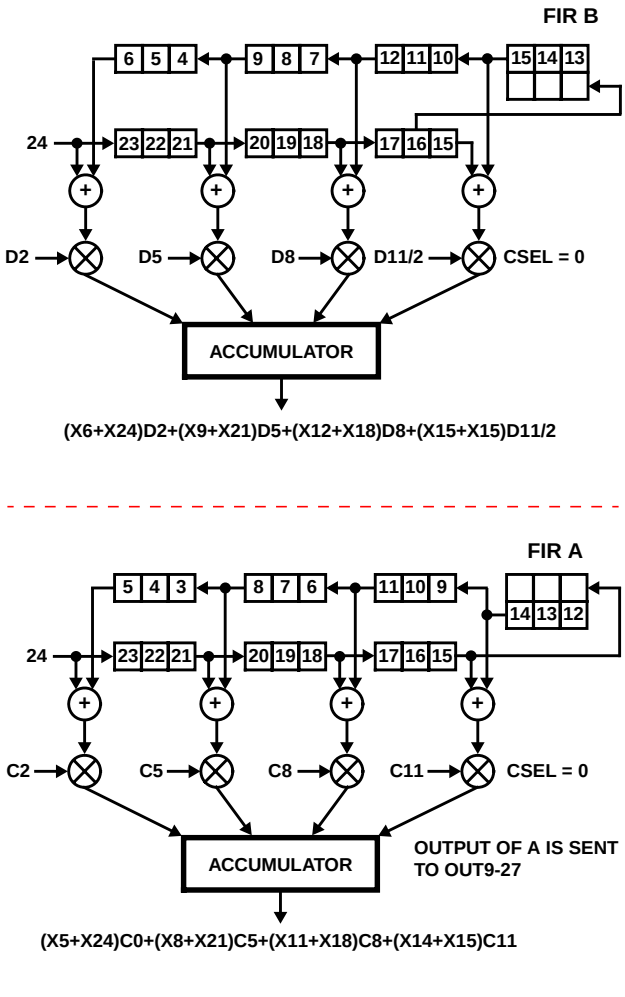


FIGURE 26D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 26. DATA FLOW DIAGRAM FOR MULTIPLEXED DECIMATION EXAMPLE

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . 5V ±5%
Temperature Range, Commercial . . . . . 0^oC to 70^oC
Temperature Range, Industrial. . . . . -40^oC to 85^o

Die Characteristics

Back Side Potential . . . . . +5V
Number of Transistors or Gates 32529

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CPGA Package	35	6
MQFP Package	33.0	N/A
PLCC Package	23.0	N/A

Maximum Junction Temperature
CPGA Package . . . . . 175^oC
MQFP and PLCC Packages. . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP and PLCC - Leads Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max CLK Frequency 33MHz Notes 3, 4, 5	-	363	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.4	V
Clock Input High	V_{IHC}	V_{CC} = Max	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = Min	-	0.8	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz All measurements referenced to GND. $T_A = 25^oC$, Note 2	-	12	pF
Output Capacitance	C_{OUT}		-	12	pF

NOTES:

2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
3. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 11mA/MHz.
4. Output load per test load circuit and C_L = 40pF.
5. Maximum junction temperature must be considered when operating part at high clock frequencies.

AC Electrical Specifications

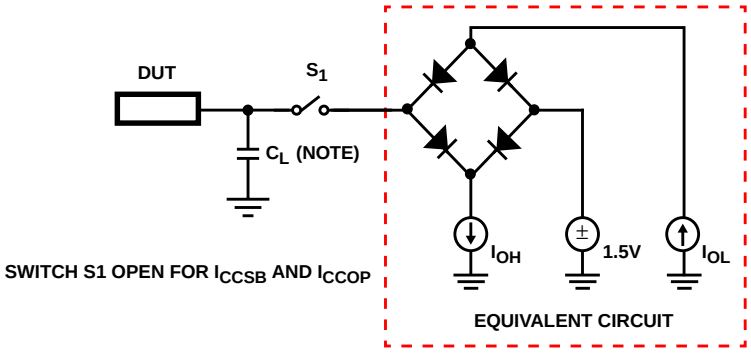
V_{CC} = +4.75V to +5.25V, T_A = 0°C to 70°C Commercial, T_A = -40°C to 85°C Industrial (Note 6)

PARAMETER	SYMBOL	NOTES	-33 (33MHz)		-40 (40.8MHz)		-45 (45MHz)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		30	-	24.5	-	22	-	ns
CLK High	t_{CH}		12	-	10	-	8	-	ns
CLK Low	t_{CL}		12	-	10	-	8	-	ns
$\overline{WR}$ Period	t_{WP}		30	-	24.5	-	22	-	ns
$\overline{WR}$ High	t_{WH}		12	-	10	-	10	-	ns
$\overline{WR}$ Low	t_{WL}		12	-	10	-	10	-	ns
Setup Time A0-8 to $\overline{WR}$ Going Low	t_{AWS}		10	-	8	-	8	-	ns
Hold Time A0-8 from $\overline{WR}$ Going High	t_{AWH}		0	-	0	-	0	-	ns
Setup Time CIN0-9 to $\overline{WR}$ Going High	t_{CWS}		12	-	11	-	10	-	ns
Hold Time CIN0-9 from $\overline{WR}$ Going High	t_{CWH}		1	-	1	-	1	-	ns
Setup Time $\overline{WR}$ Low to CLK Low	t_{WLCL}	Note 7	5	-	4	-	3	-	ns
Setup Time CIN0-9 to CLK Low	t_{CVCL}	Note 7	7	-	7	-	7	-	ns
Setup Time CSEL0-5, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, $\overline{TXFR}$, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	t_{ECS}		15	-	13	-	12	-	ns
Hold Time CSEL0-5, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, $\overline{TXFR}$, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	t_{ECH}		0	-	0	-	0	-	ns
CLK to Output Delay OUT0-27	t_{DO}		-	14	-	13	-	12	ns
Output Enable Time	t_{OE}		-	12	-	12	-	12	ns
Output Disable Time	t_{OD}	Note 8	-	12	-	12	-	12	ns
Output Rise, Fall Time	t_{RF}	Note 8	-	6	-	6	-	6	ns

NOTES:

6. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
7. Setup time requirement for loading of data on CIN0-9 to guarantee recognition on the following clock.
8. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

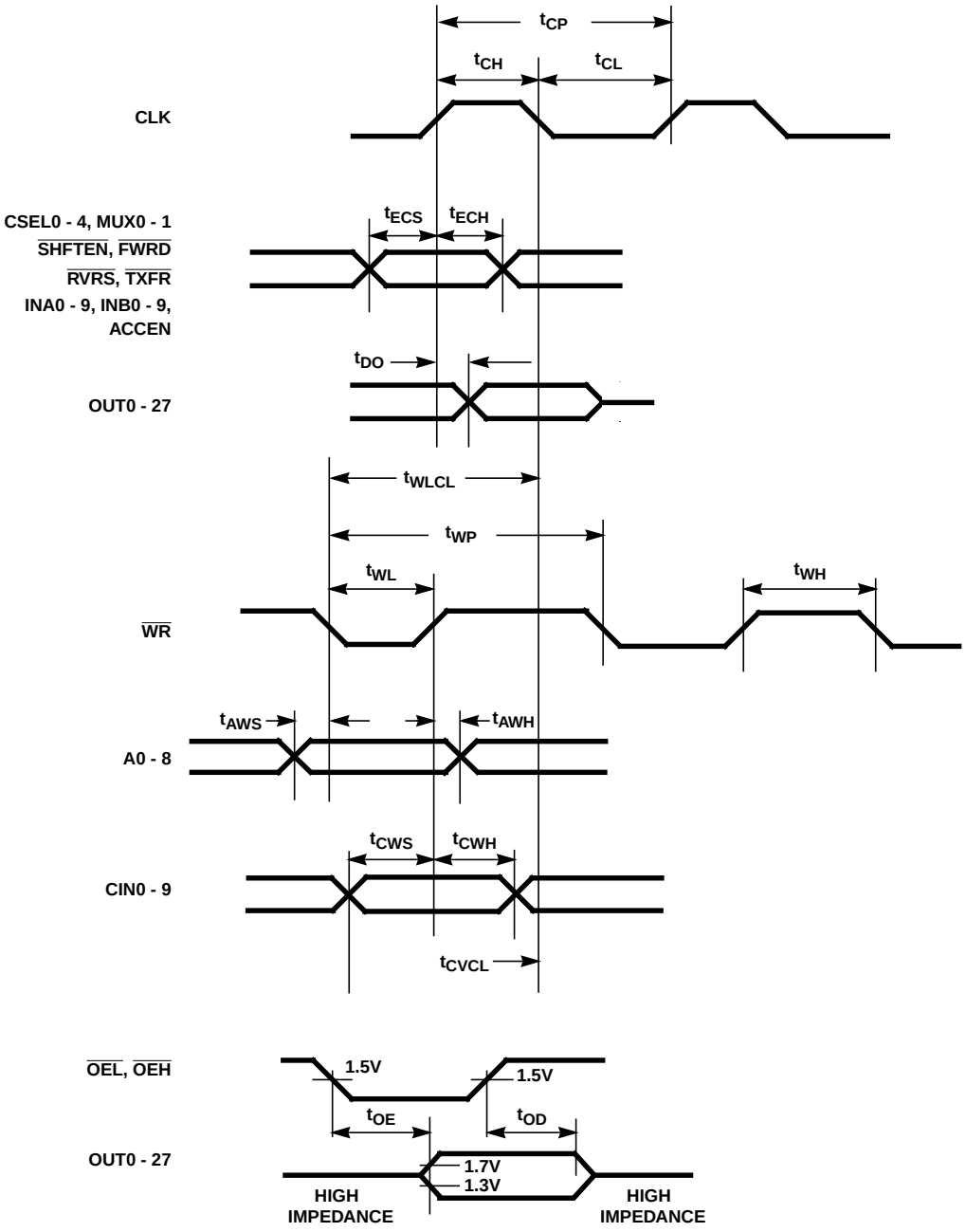


FIGURE 27. OUTPUT ENABLE, DISABLE TIMING

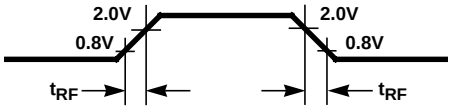
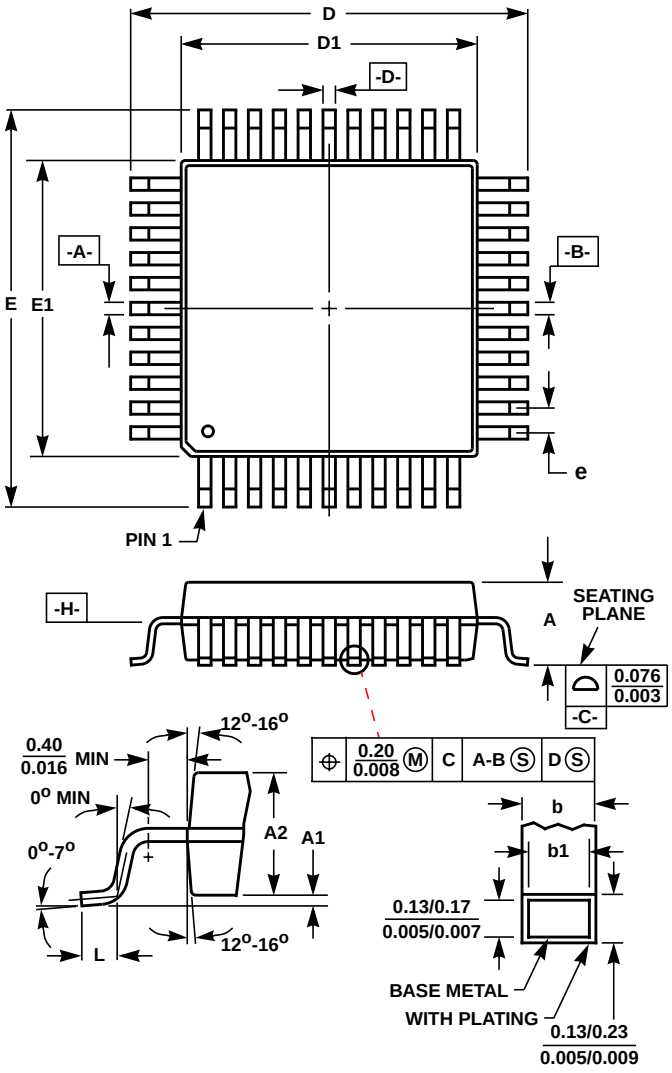


FIGURE 28. OUTPUT RISE AND FALL TIMES

Metric Plastic Quad Flatpack Packages (MQFP)



Q100.14x20 (JEDEC MS-022GC-1 ISSUE B)
100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

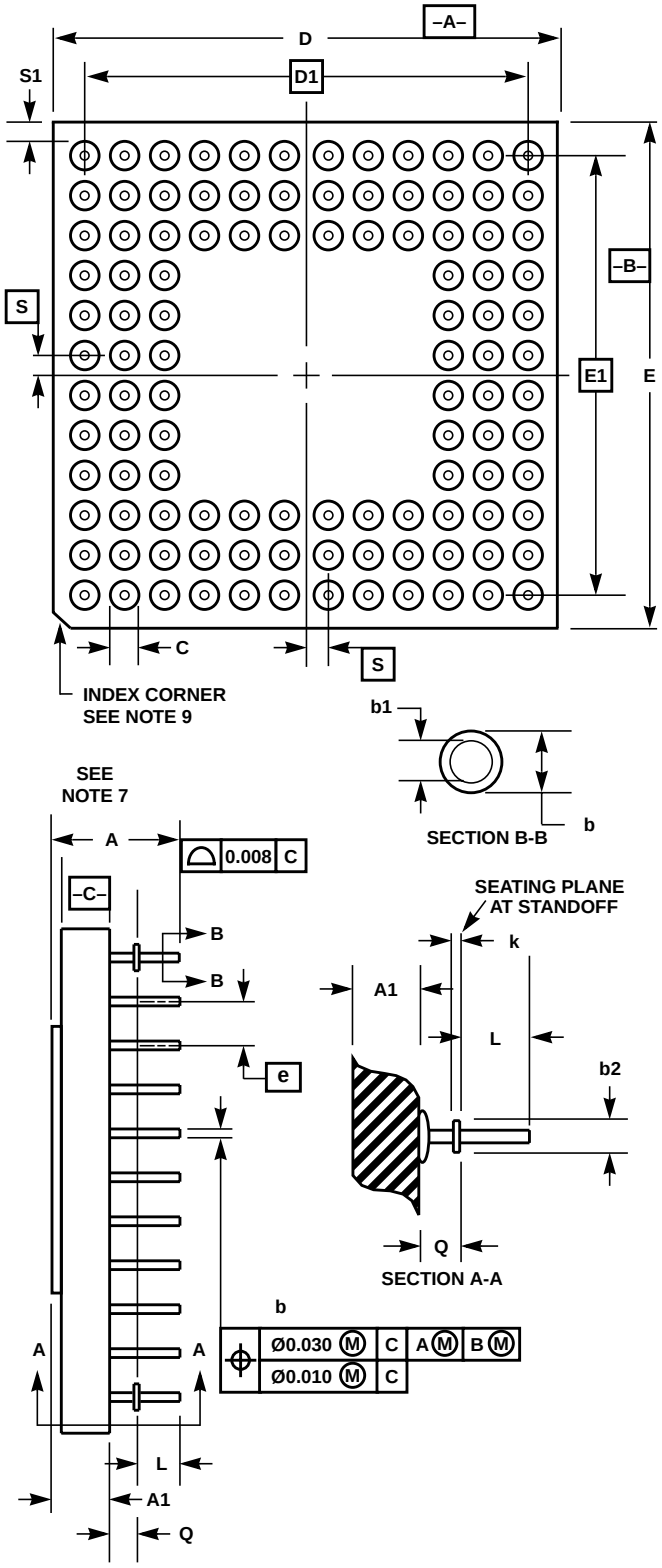
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.101	0.113	2.57	2.87	-
b	0.009	0.015	0.22	0.38	6
b1	0.009	0.013	0.22	0.33	-
D	0.908	0.918	23.08	23.32	3
D1	0.782	0.792	19.88	20.12	4, 5
E	0.673	0.681	17.10	17.30	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

Rev. 1 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

Ceramic Pin Grid Array Packages (CPGA)



G84.A MIL-STD-1835 CMGA3-P84C (P-AC)
84 LEAD CERAMIC PIN GRID ARRAY PACKAGE

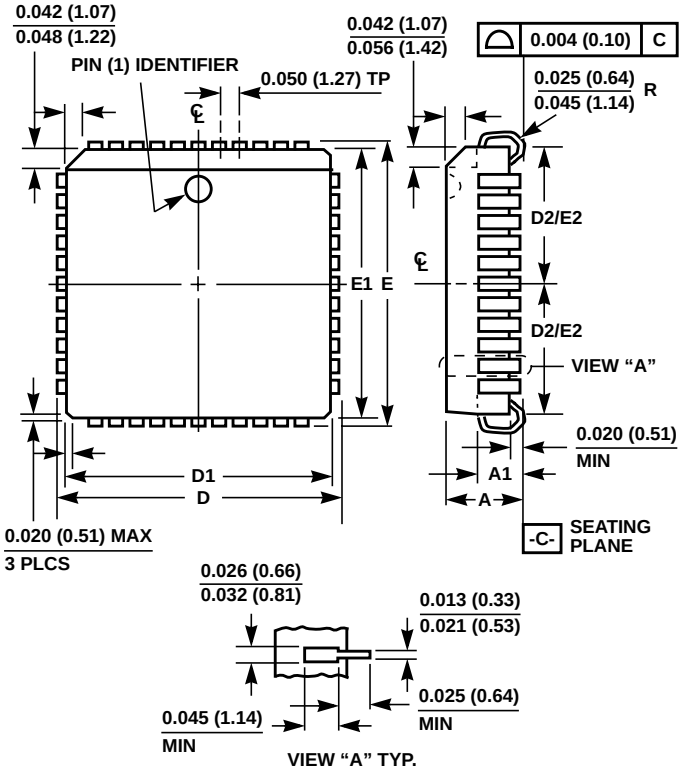
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 1 6/28/95

NOTES:

1. “M” represents the maximum pin matrix size.
2. “N” represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension “A1” includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension “A1” does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension “Q” applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension “S” is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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