

16-Bit Numerically Controlled Oscillator

The Intersil HSP45106/883 is a high performance 16-bit quadrature Numerically Controlled Oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the Block Diagram, the HSP45106/883 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.006Hz at 25.6MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8 level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 32-bit phase argument which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude. The outputs of the Sine/Cosine Section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel or serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 25.6MHz Clock Rate
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8 Level PSK Supported Through Three Pin Interface
- Simultaneous 16-Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.006Hz Tuning Resolution at 25.6MHz
- Serial or Parallel Outputs
- Spurious Frequency Components < -90dBc
- 16-Bit Microprocessor Compatible Control Interface

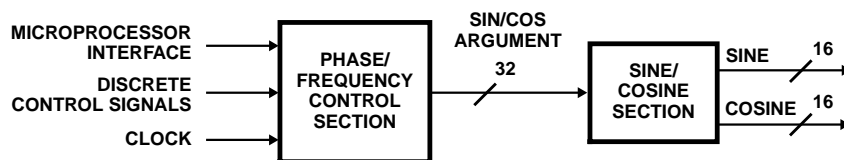
Applications

- Direct Digital Synthesis
- Quadrature Signal Generation
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Precision Signal Generation

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP45106GM-25/883	-55 to 125	85 Ld PGA	G85.A

Block Diagram



Absolute Maximum Ratings

Supply Voltage +8.0V
 Input, Output Voltage Applied GND -0.5V to V_{CC} +0.5V
 ESD Classification Class 1

Operating Conditions

Temperature Range -55°C to 125°C
 Voltage Range +4.5V to +5.5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PGA Package 36.0 7.0
 Maximum Package Power Dissipation at 125°C
 PGA Package 1.39W
 Maximum Junction Temperature 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Die Characteristics

Gate Count. 18,750

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logical One Input Voltage	V _{IH}	V _{CC} = 5.5V	1, 2, 3	55 ≤ T _A ≤ +125	2.2	-	V
Logical Zero Input Voltage	V _{IL}	V _{CC} = 4.5V	1, 2, 3	55 ≤ T _A ≤ +125	-	0.8	V
Output HIGH Voltage	V _{OH}	I _{OH} = -400µA V _{CC} = 4.5V (Note 2)	1, 2, 3	55 ≤ T _A ≤ +125	2.6	-	V
Output LOW Voltage	V _{OL}	I _{OL} = +2.0mA V _{CC} = 4.5V (Note 2)	1, 2, 3	55 ≤ T _A ≤ +125	-	0.4	V
Input Leakage Current	I _I	V _{IN} = V _{CC} or GND V _{CC} = 5.5V	1, 2, 3	55 ≤ T _A ≤ +125	-10	+10	µA
Output Leakage Current	I _O	V _{OUT} = V _{CC} or GND V _{CC} = 5.5V	1, 2, 3	55 ≤ T _A ≤ +125	-10	+10	µA
Clock Input High	V _{IHC}	V _{CC} = 5.5V	1, 2, 3	55 ≤ T _A ≤ +125	3.0	-	V
Clock Input Low	V _{ILC}	V _{CC} = 4.5V	1, 2, 3	55 ≤ T _A ≤ +125	-	0.8	V
Standby Power Supply Current	I _{CCSB}	V _{IN} = V _{CC} or GND V _{CC} = 5.5V, (Note 5)	1, 2, 3	55 ≤ T _A ≤ +125	-	500	µA
Operating Power Supply Current	I _{CCOP}	f = 25.6MHz V _{CC} = 5.5V (Notes 3, 5)	1, 2, 3	55 ≤ T _A ≤ +125	-	205	mA
Functional Test	FT	(Note 4)	7, 8	55 ≤ T _A ≤ +125	-	-	-

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating supply current is proportional to frequency, typical rating is 8mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
5. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUP	TEMPERATURE (°C)	-25 (25.6MHz)		UNITS
					MIN	MAX	
CLK Period	t _{CP}		9, 10, 11	-55 ≤ T _A ≤ 125	39	-	ns
CLK High	t _{CH}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
CLK Low	t _{CL}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
\overline{WR} Period	t _{WP}		9, 10, 11	-55 ≤ T _A ≤ 125	39	-	ns
\overline{WR} High	t _{WH}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
\overline{WR} Low	t _{WL}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
Setup Time A(2:0), \overline{CS} to \overline{WR} Going High	t _{AWS}		9, 10, 11	-55 ≤ T _A ≤ 125	13	-	ns
Hold Time A(2:0), \overline{CS} from \overline{WR} Going High	t _{AWH}		9, 10, 11	-55 ≤ T _A ≤ 125	2	-	ns
Setup Time C(15:0) to \overline{WR} Going High	t _{CWS}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
Hold Time C(15:0) from \overline{WR} Going High	t _{CWH}		9, 10, 11	-55 ≤ T _A ≤ 125	1	-	ns
Setup Time \overline{WR} High to CLK High	t _{WC}	Note 8	9, 10, 11	-55 ≤ T _A ≤ 125	16	-	ns
Setup Time MOD(2:0) to CLK Going High	t _{MCS}		9, 10, 11	-55 ≤ T _A ≤ 125	15	-	ns
Hold Time MOD(2:0) from CLK Going High	t _{MCH}		9, 10, 11	-55 ≤ T _A ≤ 125	1	-	ns
Setup Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, \overline{ENPHAC} , $\overline{ENTIREG}$, \overline{INHOFR} , \overline{PMSEL} , $\overline{INITPAC}$, \overline{BINFMT} , \overline{TEST} , $\overline{PAR/SER}$, \overline{PACI} , $\overline{INITTAC}$ to CLK Going High	t _{ECS}		9, 10, 11	-55 ≤ T _A ≤ 125	12	-	ns
Setup Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, \overline{ENPHAC} , $\overline{ENTIREG}$, \overline{INHOFR} , \overline{PMSEL} , $\overline{INITPAC}$, \overline{BINFMT} , \overline{TEST} , $\overline{PAR/SER}$, \overline{PACI} , $\overline{INITTAC}$ from CLK Going High	t _{ECH}		9, 10, 11	-55 ≤ T _A ≤ 125	1	-	ns
CLK to Output Delay SIN(15:0), COS(15:0), \overline{TICO}	t _{DO}		9, 10, 11	-55 ≤ T _A ≤ 125	-	18	ns
CLK to Output Delay $\overline{DACSTRB}$	t _{DSO}		9, 10, 11	-55 ≤ T _A ≤ 125	2	18	ns
Output Enable Time	t _{OE}	Note 7	9, 10, 11	-55 ≤ T _A ≤ 125	-	12	ns

NOTES:

- AC Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and 0". CLK is driven at 4.0V and 0V and measured at 2.0V. Output load per test load circuit with switch closed and C_L = 40pF.
- Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.
- If $\overline{ENOFRACTL}$, $\overline{ENCFRACTL}$, $\overline{ENTICTL}$, or $\overline{ENPHREG}$ are active, care must be taken to not violate setup and hold times to these registers when writing data into the chip via the C(15:0) port.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (°C)	-25 (25MHz)		UNITS
					MIN	MAX	
Input Capacitance	C _{IN}	V _{CC} = Open, f = 1MHz, all measurements are referenced to device GND.	9	T _A = 25	-	10	pF
Output Capacitance	C _{OUT}	V _{CC} = Open, f = 1MHz, all measurements are referenced to device GND.	9	T _A = 25	-	10	pF
Output Disable Delay	t _{OEZ}		9, 10	-55 ≤ T _A ≤ 125	-	15	ns
Output Rise Time	t _{OR}	From 0.8V to 2.0V	9, 10	-55 ≤ T _A ≤ 125	-	8	ns
Output Fall Time	t _{OF}	From 2.0V to 0.8V	9, 10	-55 ≤ T _A ≤ 125	-	8	ns

NOTES:

9. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

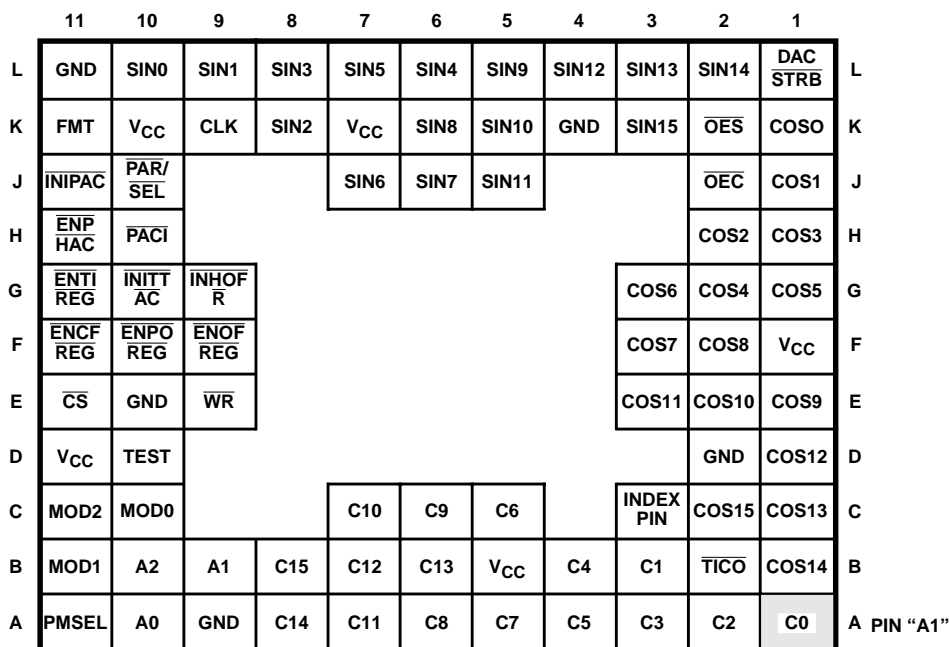
10. Loading is as specified in the test load circuit with switch closed and C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP45106/833 (PGA)



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	C0	F7	B11	MOD1	F13	F9	ENOFREG	F8	K2	OES	F14
A2	C2	F7	C1	COS13	V _{CC} /2	F10	ENPOREG	F4	K3	SIN15	V _{CC} /2
A3	C3	F7	C2	COS15	V _{CC} /2	F11	ENCFREQ	F7	K4	GND	GND
A4	C5	F8	C5	C6	F8	G1	COS5	V _{CC} /2	K5	SIN10	V _{CC} /2
A5	C7	F8	C6	C9	F10	G2	COS4	V _{CC} /2	K6	SIN8	V _{CC} /2
A6	C8	F10	C7	C10	F10	G3	COS6	V _{CC} /2	K7	V _{CC}	V _{CC}
A7	C11	F10	C10	MOD0	F12	G9	INHOF R	F11	K8	SIN2	V _{CC} /2
A8	C14	F11	C11	MOD2	F14	G10	INITTAC	F13	K9	CLK	F0
A9	GND	GND	D1	COS12	V _{CC} /2	G11	ENTIREG	F12	K10	V _{CC}	V _{CC}
A10	A0	F8	D2	GND	GND	H1	COS3	V _{CC} /2	K11	BINFMT	F6
A11	PMSEL	F14	D10	TEST	F14	H2	COS2	V _{CC} /2	L1	DACSTRB	V _{CC} /2
B1	COS14	V _{CC} /2	D11	V _{CC}	V _{CC}	H10	PACI	F11	L2	SIN14	V _{CC} /2
B2	TICO	V _{CC} /2	E1	COS9	V _{CC} /2	H11	ENPHAC	F10	L3	SIN13	V _{CC} /2
B3	C1	F7	E2	COS10	V _{CC} /2	J1	COS1	V _{CC} /2	L4	SIN12	V _{CC} /2
B4	C4	F8	E3	COS11	V _{CC} /2	J2	OEC	F14	L5	SIN9	V _{CC} /2
B5	V _{CC}	V _{CC}	E9	WR	F4	J5	SIN11	V _{CC} /2	L6	SIN4	V _{CC} /2
B6	C13	F11	E10	GND	GND	J6	SIN7	V _{CC} /2	L7	SIN5	V _{CC} /2
B7	C12	F11	E11	CS	F6	J7	SIN6	V _{CC} /2	L8	SIN3	V _{CC} /2
B8	C15	F11	F1	V _{CC}	V _{CC}	J10	PAR/SER	F13	L9	SIN1	V _{CC} /2
B9	A1	F7	F2	COS8	V _{CC} /2	J11	INITPAC	F12	L10	SIN0	V _{CC} /2
B10	A2	F10	F3	COS7	V _{CC} /2	K1	COS0	V _{CC} /2	L11	GND	GND

NOTES:

- V_{CC}/2 (2.7V ±10%) used for outputs only.
- 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
- V_{CC} = 5.5V ±0.5V.
- 0.1µF (min) capacitor between V_{CC} and GND per position.
- F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2..., F11 = F10/2, 40% - 60% Duty Cycle.
- Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%.

Die Characteristics

DIE DIMENSIONS:

251 mils x 240 mils x 19 ±1mils

METALLIZATION:

Type: Si-Al, or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

0.8×10^5 A/cm²

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029