Data Sheet July 1999 File Number 2838.3

2A, 60V, 0.160 Ohm, Logic Level, N-Channel Power MOSFET

The RFW2N06RLE N-Channel, logic level, ESD protected, power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFW2N06RLE was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor and relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA9861.

Ordering Information

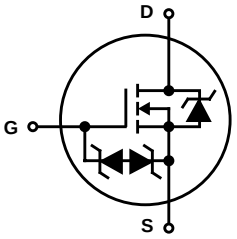
PART NUMBER	PACKAGE	BRAND
RFW2N06RLE	HEXDIP	RFW2N06RLE

NOTE: When ordering, use the entire part number.

Features

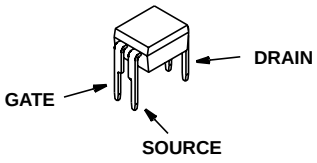
- 2A, 60V
- $r_{DS}(on) = 0.160\Omega$
- UIS Rating Curve (Single Pulse)
- Design Optimized For 5 Volt Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Electrostatic Discharge Protected
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

4 PIN HEXDIP



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFW2N06RLE	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Continuous Drain Current	I_D	2	A
Pulsed Drain Current (Note 3)	I_{DM}	14	A
Gate to Source Voltage	V_{GS}	-5 to 10	V
Maximum Power Dissipation (Figure 1)	P_D	1.09	W
Linear Derating Factor (Figure 1)		0.009	$W/^oC$
Single Pulse Avalanche Energy Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating, MIL-STD-883, Catagory B(2)	ESD	2	KV
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D =250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V $T_C = 125^oC$		-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} =-5V to 10V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 2A, V_{GS} = 5V (Figure 8)		-	-	160	mΩ
		I_D = 2A, V_{GS} = 4.3V (Figure 8)		-	-	200	mΩ
Turn-On Time	$t_{(ON)}$	V_{DD} = 30V, I_D = 2A, R_L = 15Ω, V_{GS} = 5V, R_G = 25Ω (Figures 12, 13, 14)		-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$			-	13	-	ns
Rise Time	t_r			-	42	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	95	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	$t_{(OFF)}$				-	200	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to 10V	V_{DD} = 48V, I_D = 2A, $I_{G(REF)}$ =0.5mA, R_L = 24Ω (Figures 12, 15, 16)	-	20	30	nC
Gate Charge at 5V	$Q_g(5)$	V_{GS} = 0 to 5V		-	11	16	nC
Threshold Gate Charge	$Q_g(TH)$	V_{GS} = 0 to 1V		-	0.6	1.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	535	-	pF
Output Capacitance	C_{OSS}			-	175	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	32	-	pF
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	-	115	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 2A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/μs	-	-	200	ns

NOTES:

2. Pulse test: width ≤ 300μs duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

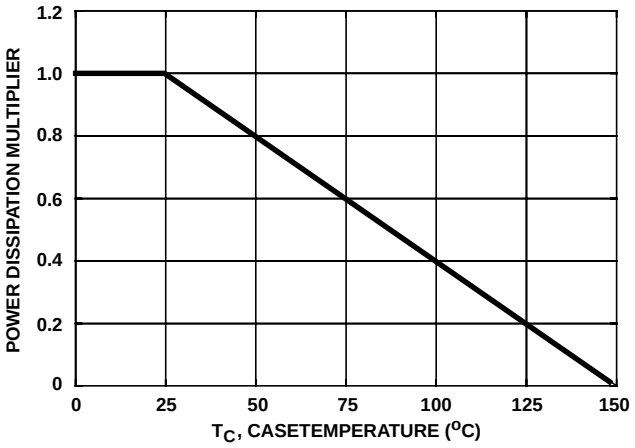


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

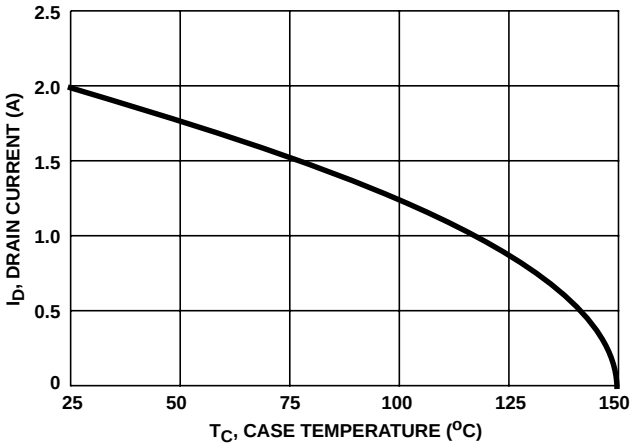


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

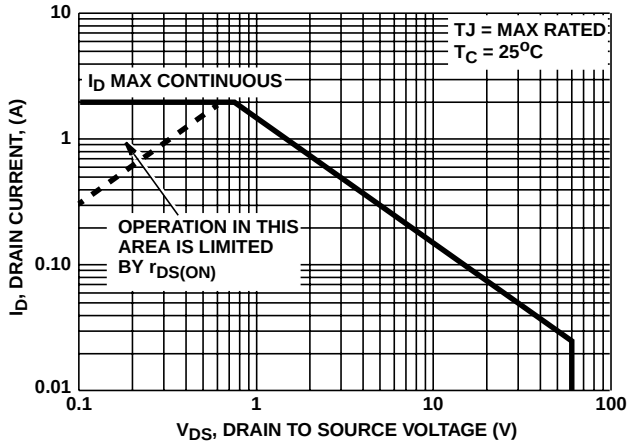


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

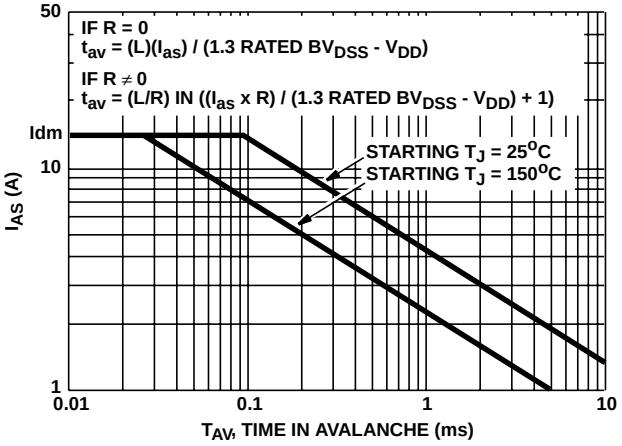


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

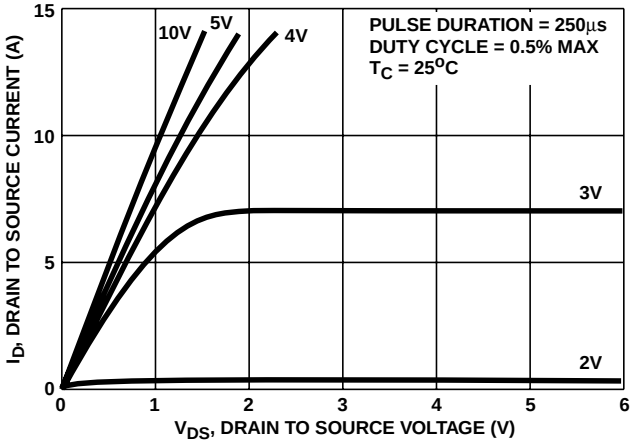


FIGURE 5. SATURATION CHARACTERISTICS

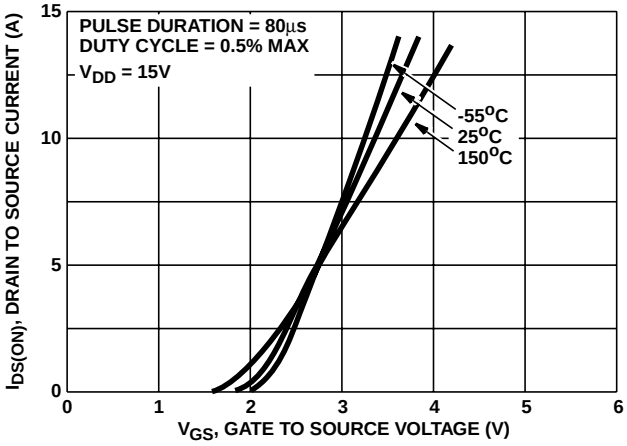


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

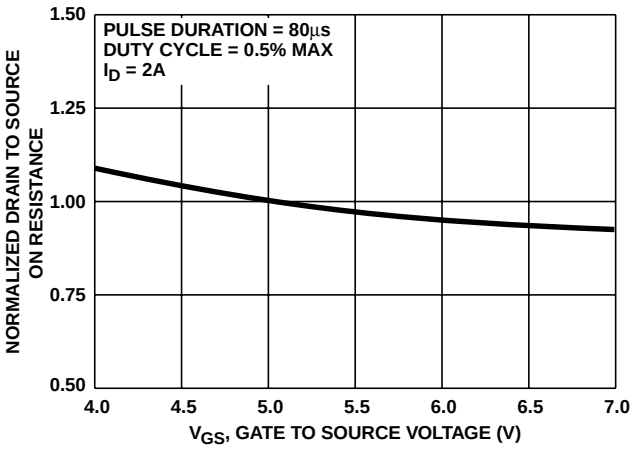


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON VOLTAGE vs GATE VOLTAGE

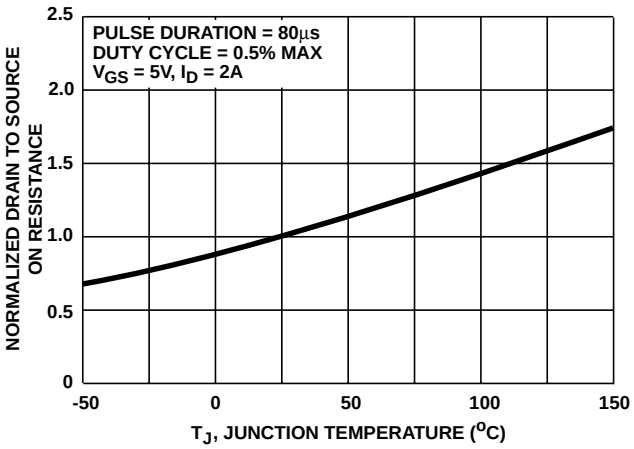


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

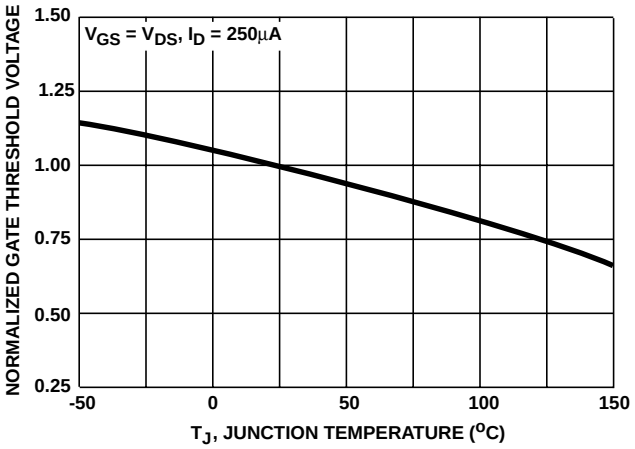


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

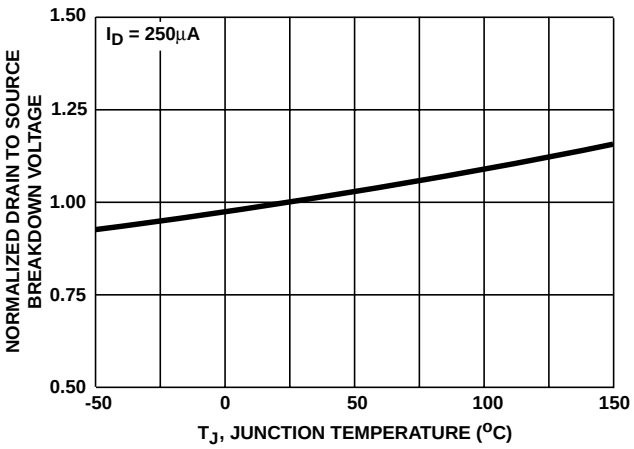


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

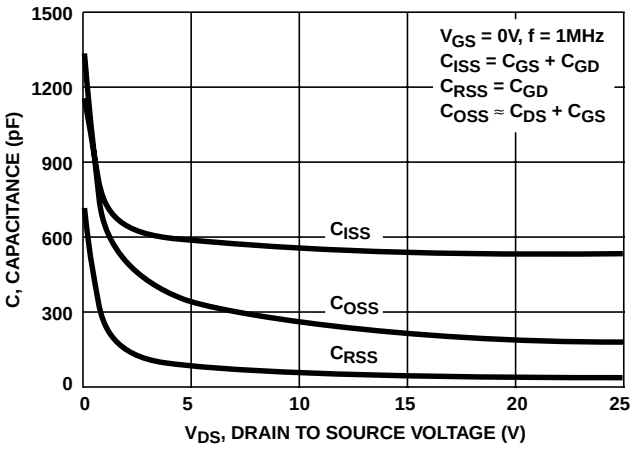
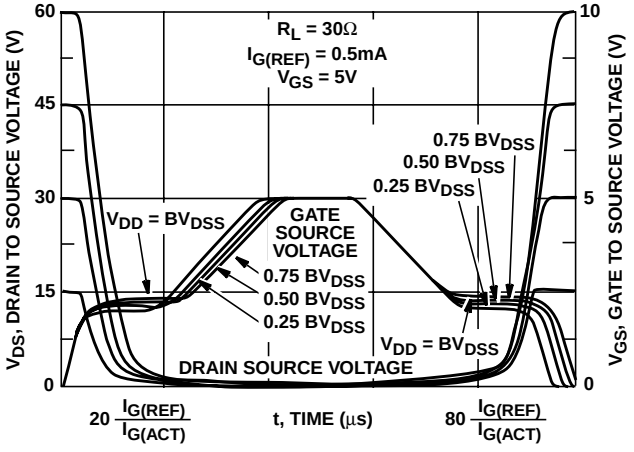


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

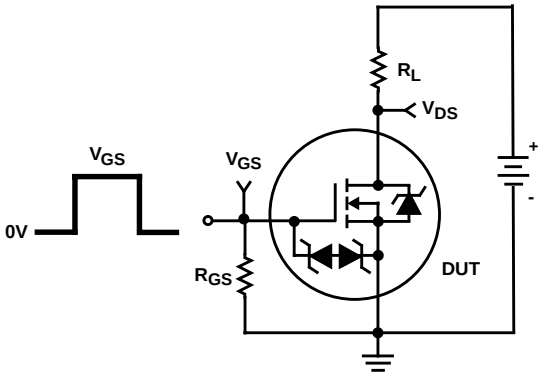


FIGURE 13. SWITCHING TIME TEST CIRCUIT

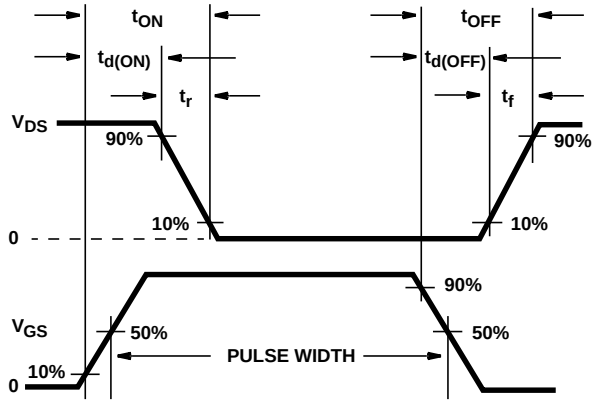


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

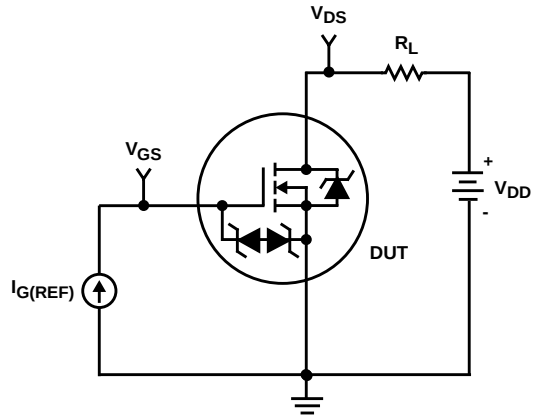


FIGURE 15. GATE CHARGE TEST CIRCUIT

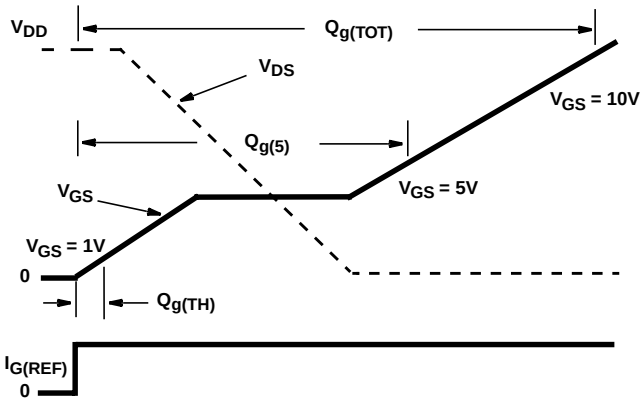


FIGURE 16. GATE CHARGE WAVEFORMS

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