

4.3A, 1000V, 3.500 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09850.

Ordering Information

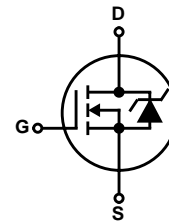
PART NUMBER	PACKAGE	BRAND
IRFPG40	TO-247	IRFPG40

NOTE: When ordering, include the entire part number.

Features

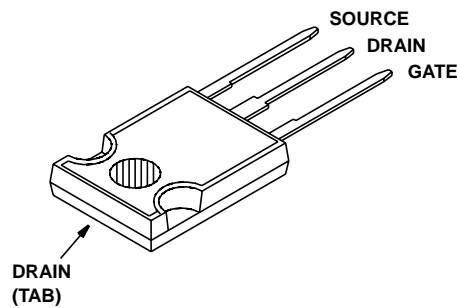
- 4.3A, 1000V
- $r_{DS(ON)} = 3.500\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to 150°C Operating and Storage Temperature

Symbol



Packaging

JEDEC STYLE TO-247



IRFPG40

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFPG40	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	1000 V
Drain to Gate Voltage (Note 1)	V_{DGR}	1000 V
Continuous Drain Current	I_D	4.3 A
Pulsed Drain Current (Note 3)	I_{DM}	17 A
Gate to Source Voltage	V_{GS}	± 20 V
Maximum Power Dissipation	P_D	150 W
Linear Derating Factor		1.2 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	490 mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 9)	1000	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}$	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2.5\text{A}$, $V_{GS} = 10\text{V}$ (Figures 7, 8)	-	3.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$I_D = 2.5\text{A}$, $V_{DS} = 100\text{V}$ (Figure 11)	3.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 500\text{V}$, $I = 3.9\text{A}$, $R_{GS} = 9.1\Omega$, $R_L = 120\Omega$ $V_{GS} = 10\text{V}$	-	30	ns
Rise Time	t_r		-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	170	ns
Fall Time	t_f		-	50	ns
Total Gate Charge	$Q_{g(TOT)}$	$I_D = 3.9\text{A}$, $V_{DS} = 800\text{V}$, $V_{GS} = 10\text{V}$ (Figure 13)	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	0.83	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	40	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 4.3\text{A}$ (Figure 12)	-	1.8	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 3.9\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1000	ns

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by Max junction temperature.
- $V_{DD} = 25\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 640\mu\text{H}$, $R_G = 25\Omega$, peak $I_{AS} = 9.2\text{A}$ (Figure 3).

Typical Performance Curves Unless Otherwise Specified

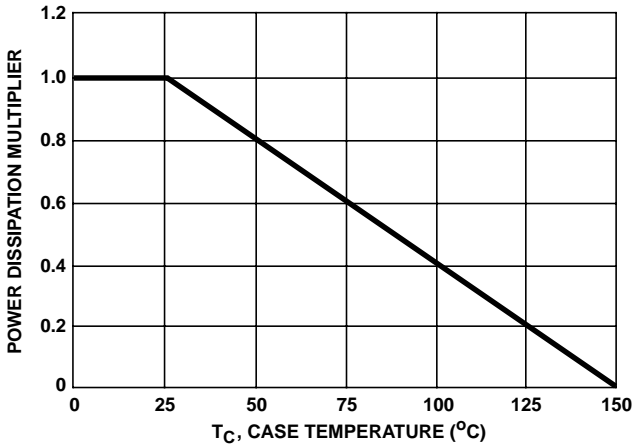


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

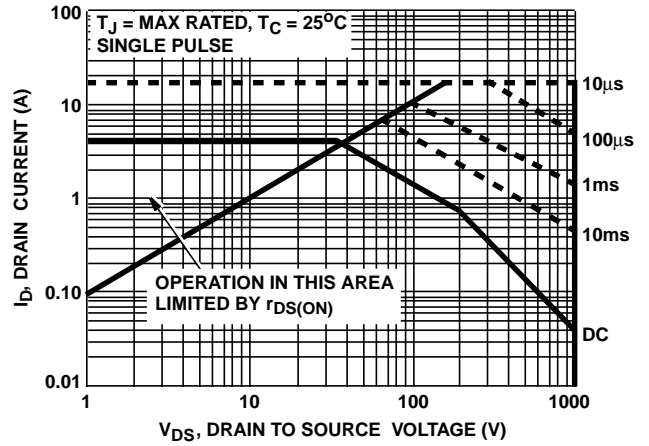


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

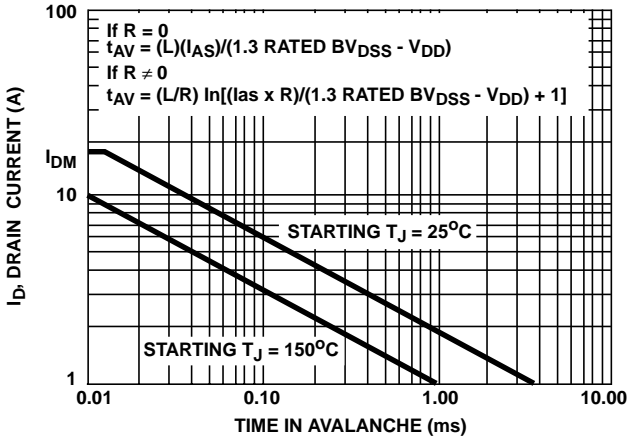


FIGURE 3. UNCLAMPED INDUCTIVE SWITCHING SOA

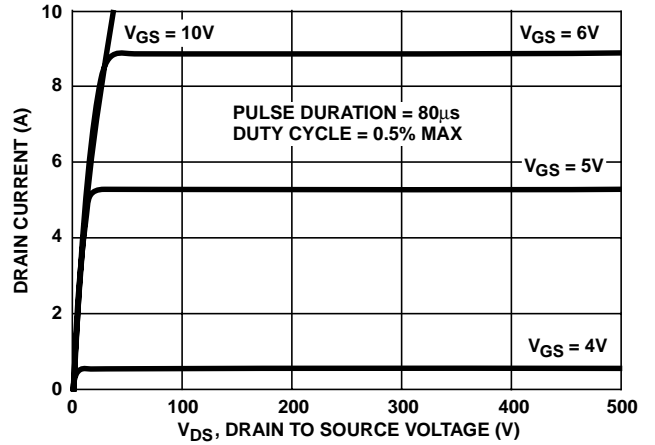


FIGURE 4. OUTPUT CHARACTERISTICS

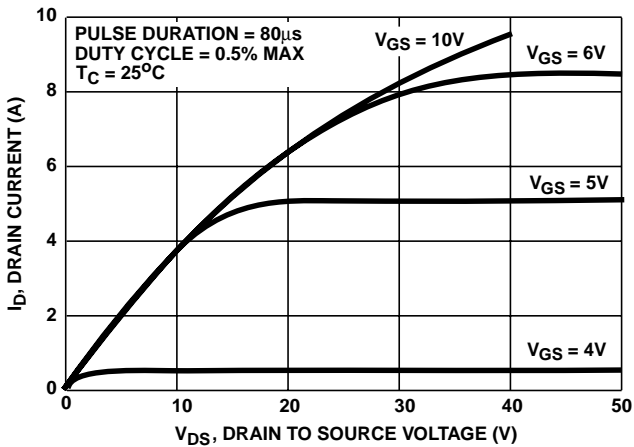


FIGURE 5. SATURATION CHARACTERISTICS

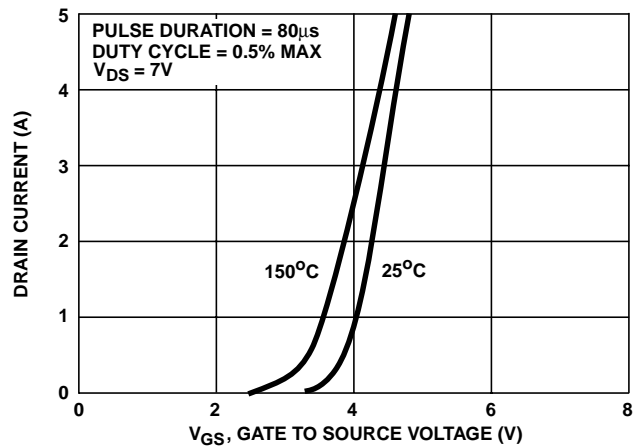


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

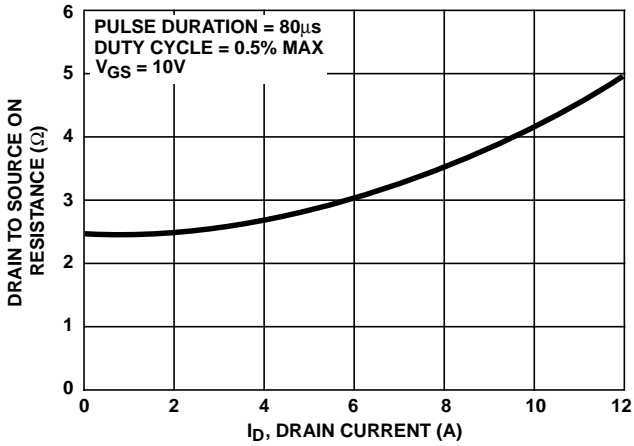


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

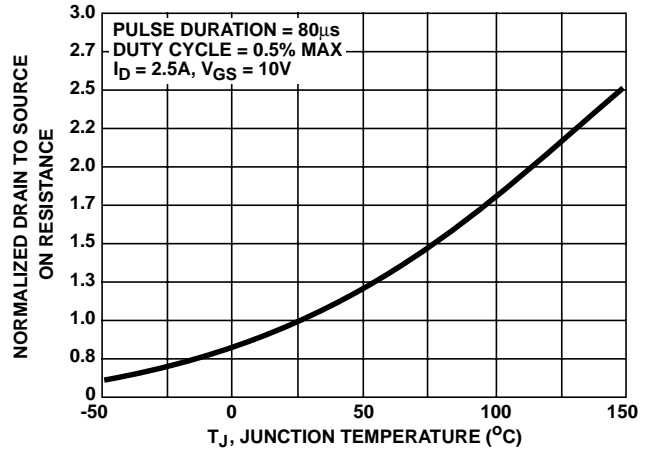


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

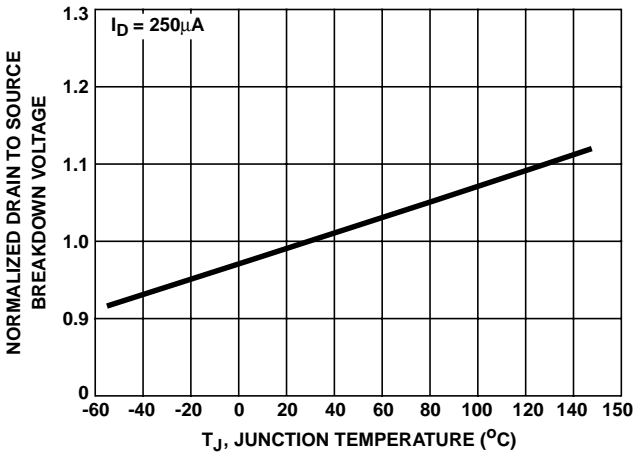


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

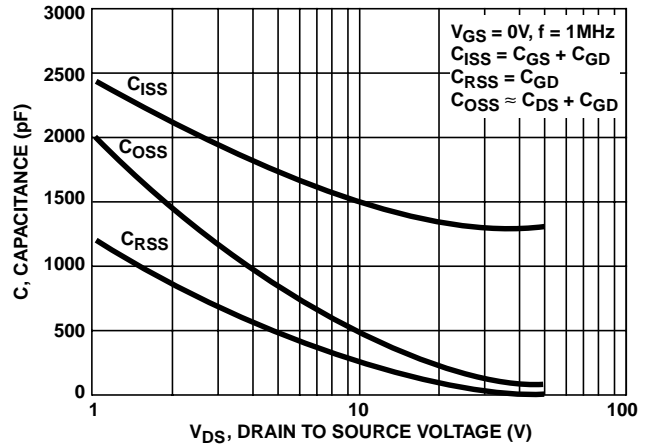


FIGURE 10. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

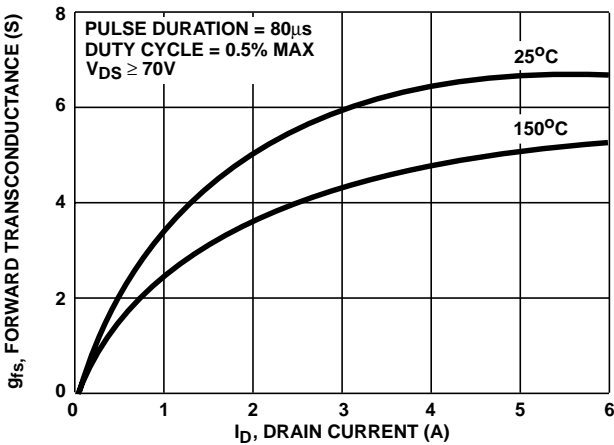


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

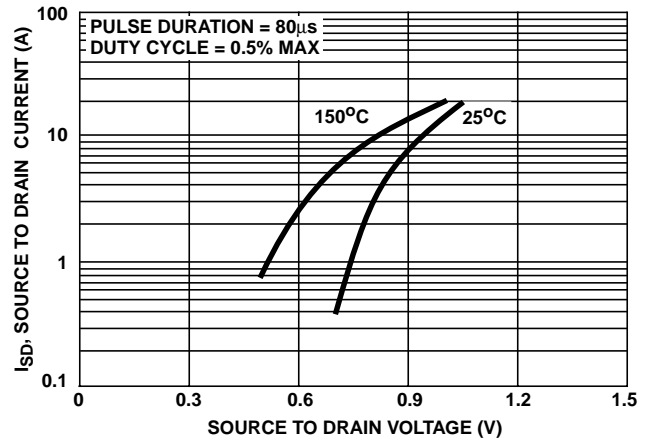


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

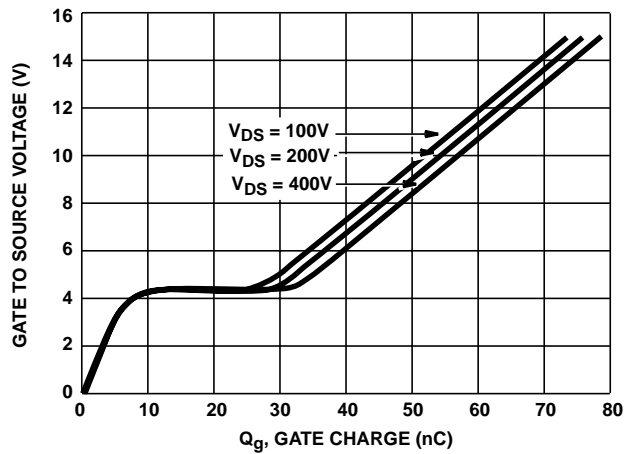


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

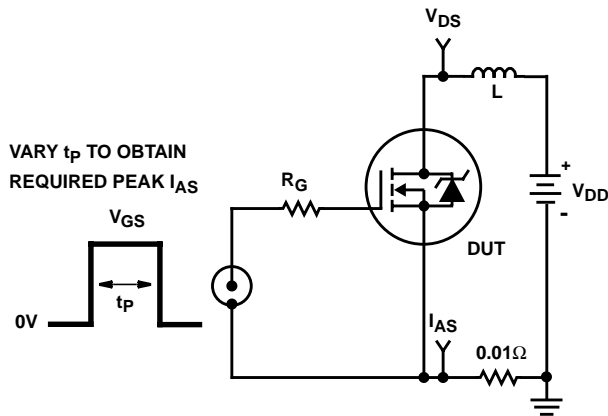


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

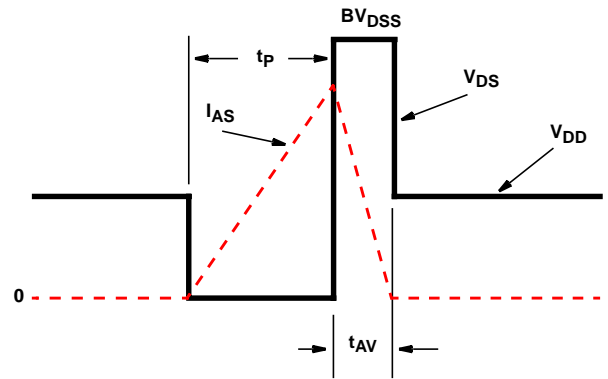


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

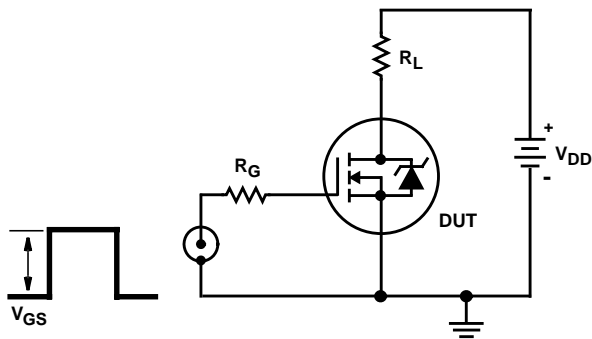


FIGURE 16. SWITCHING TIME TEST CIRCUIT

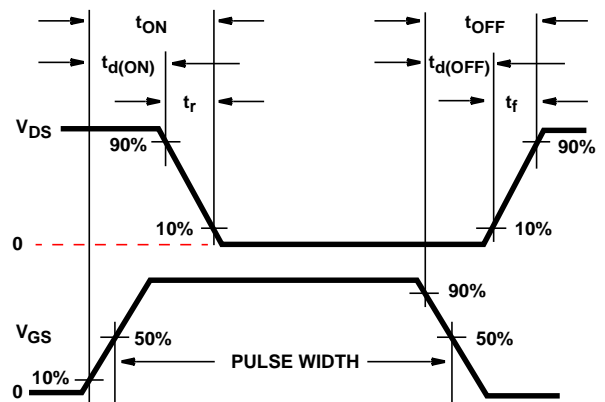


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

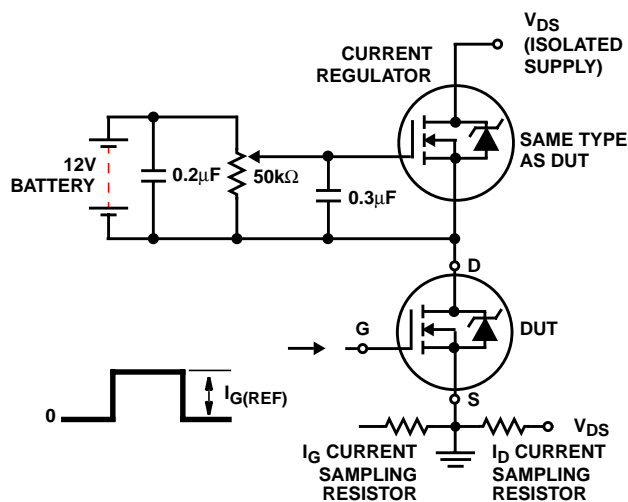


FIGURE 18. GATE CHARGE TEST CIRCUIT

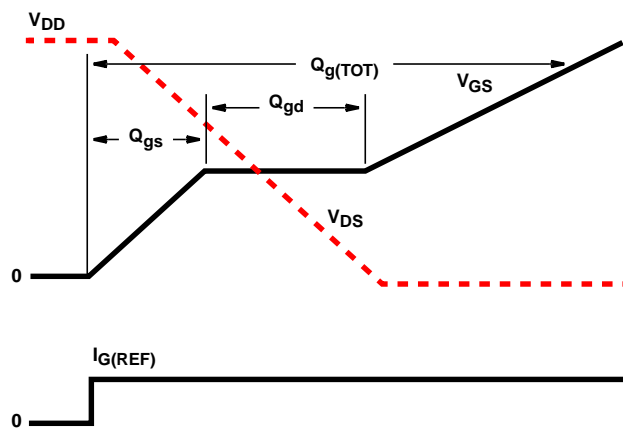


FIGURE 19. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

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Intersil Corporation
 P. O. Box 883, Mail Stop 53-204
 Melbourne, FL 32902
 TEL: (407) 724-7000
 FAX: (407) 724-7240

EUROPE

Intersil SA
 Mercure Center
 100, Rue de la Fusee
 1130 Brussels, Belgium
 TEL: (32) 2.724.2111
 FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
 7F-6, No. 101 Fu Hsing North Road
 Taipei, Taiwan
 Republic of China
 TEL: (886) 2 2716 9310
 FAX: (886) 2 2715 3029