Data Sheet | September 1998 | File Number 2897.3

400MHz, Fast Settling Operational Amplifier

The Intersil HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of ±10V into a 1kΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

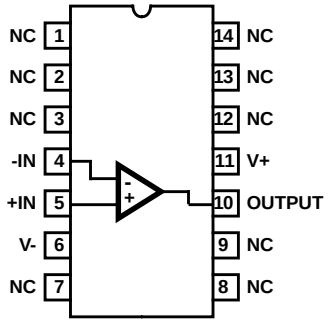
A 400V/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth product is ideally suited for wideband signal amplification. A settling time of 140ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

Refer to Application Note AN541 and Application Note AN556 for more information on High Speed Op Amp applications. HA-2540/883 MIL-STD-883 data sheet is available on request.

For a lower power version of this product, please see the HA-2850 datasheet.

Pinout

HA-2540
(CERDIP, PDIP)
TOP VIEW



Features

- Very High Slew Rate 400V/µs
- Fast Settling Time. 140ns
- Wide Gain Bandwidth ($A_V \geq 10$) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise . . . . . 6nV/$\sqrt{Hz}$
- Output Voltage Swing. . . . . ±10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA1-2540-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2540-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2540-5	0 to 75	14 Ld PDIP	E14.3
HA3-2540C-5	0 to 75	14 Ld PDIP	E14.3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current . . . . . $33mA_{RMS}$ Continuous, $50mA_{PEAK}$

Operating Conditions

Temperature Range
HA-2540-2 . . . . . -55^oC to 125^oC
HA-2540/2540C-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	107	N/A

Maximum Internal Power Dissipation (Note 1)
Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175^oC for the ceramic package, and below 150^oC for the plastic package. By using Application Note AN556 on Safe Operating Area Equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75^oC.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

PARAMETER	TEMP (^oC)	HA-2540-2			HA-2540-5			HA-2540C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	$\mu V/^oC$
Bias Current	25	-	5	20	-	5	20	-	5	20	μA
	Full	-	-	25	-	-	25	-	-	25	μA
Offset Current	25	-	1	6	-	1	6	-	1	6	μA
	Full	-	-	8	-	-	8	-	-	8	μA
Input Resistance	25	-	10	-	-	10	-	-	10	-	$k\Omega$
Input Capacitance	25	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
Input Noise Current (f = 1kHz, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Noise Voltage (f = 1kHz, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	25	10	15	-	10	15	-	7	10	-	kV/V
	Full	5	-	-	5	-	-	5	-	-	kV/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	25	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product (Notes 5, 6)	25	-	400	-	-	400	-	-	400	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Notes 3, 10)	Full	±10	-	-	±10	-	-	±10	-	-	V
Output Current (Note 3)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	25	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	25	5.5	6	-	5.5	6	-	5.5	6	-	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	25	-	14	-	-	14	-	-	14	-	ns
Overshoot	25	-	5	-	-	5	-	-	5	-	%
Slew Rate	25	320	400	-	320	400	-	320	400	-	$V/\mu s$
Settling Time: 10V Step to 0.1%	25	-	140	-	-	140	-	-	140	-	ns

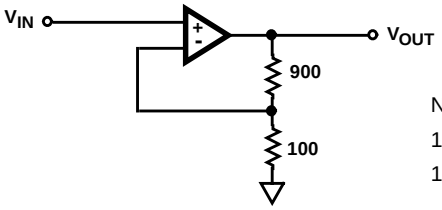
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (^oC)	HA-2540-2			HA-2540-5			HA-2540C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

3. $R_L = 1k\Omega$, $V_O = \pm10V$.
4. $V_{CM} = \pm10V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of the data sheet.
9. $V_{SUPPLY} = +5V, -15V$ and $+15V, -5V$.
10. Guaranteed range for output voltage is $\pm10V$. Functional operation outside of this range is not guaranteed.

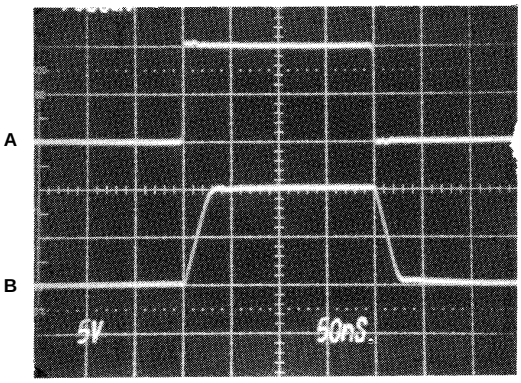
Test Circuits and Waveforms



NOTES:

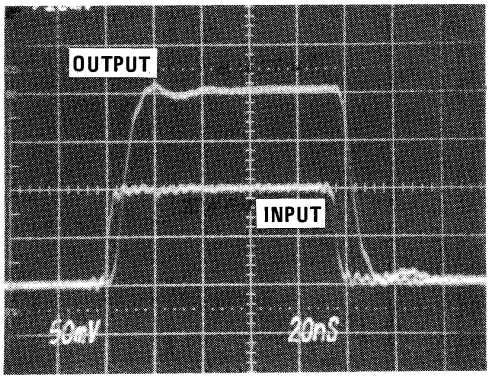
11. $A_V = +10$.
12. $C_L \leq 10pF$.

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



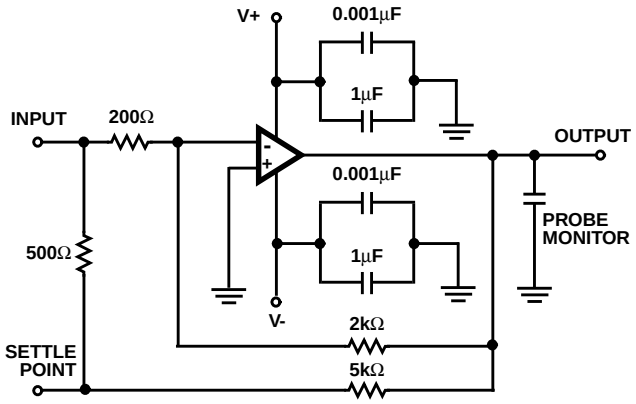
Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: 50ns/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.
Horizontal Scale: 20ns/Div.

SMALL SIGNAL RESPONSE

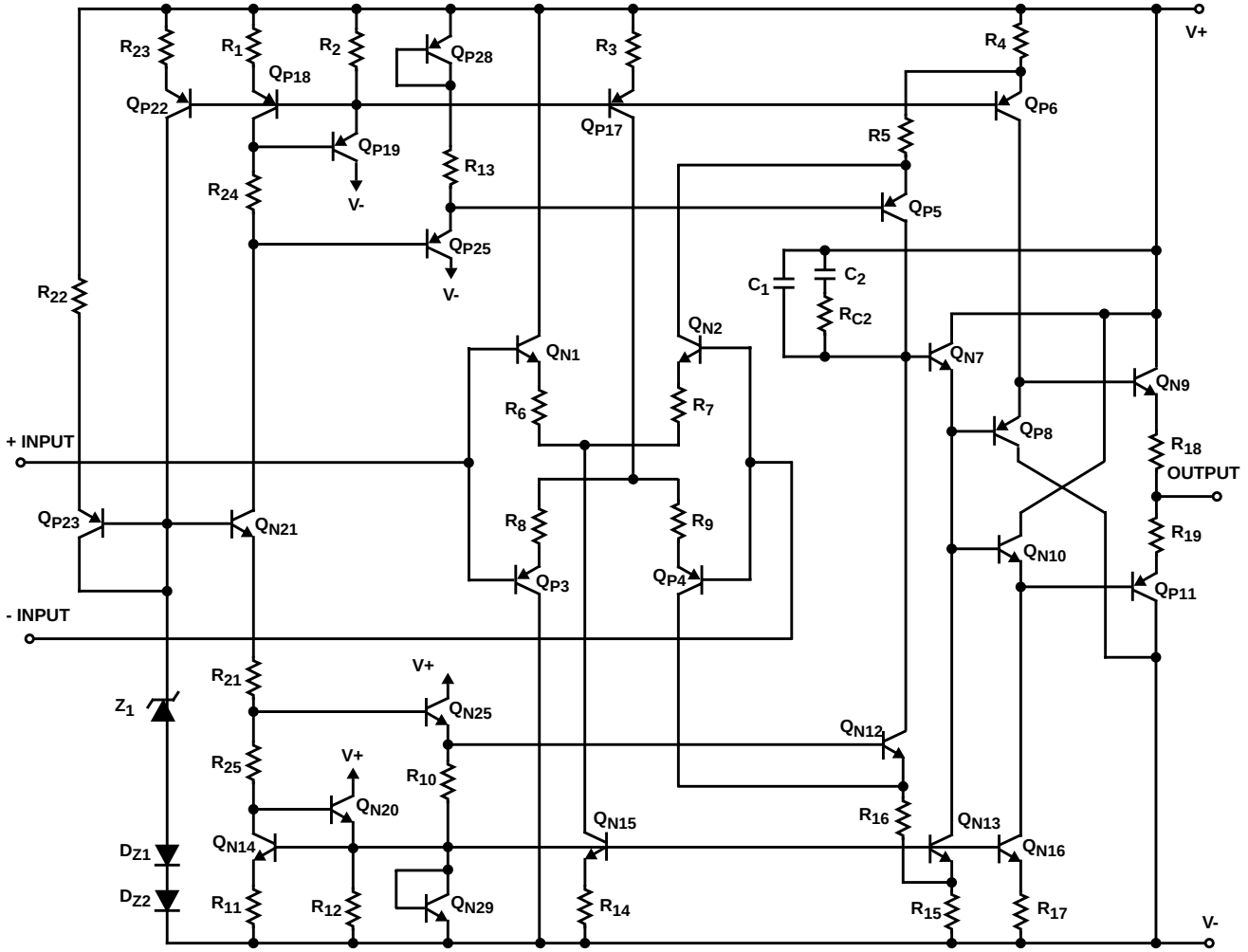


NOTES:

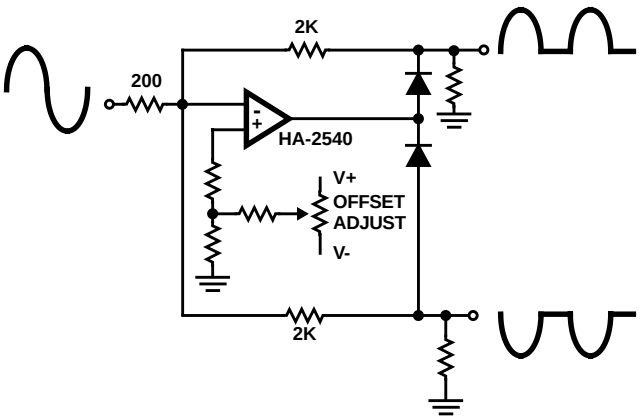
13. $A_V = -10$.
14. Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
15. It is recommended that resistors be carbon composition and the feedback and summing network ratios be matched to 0.1%.
16. SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram

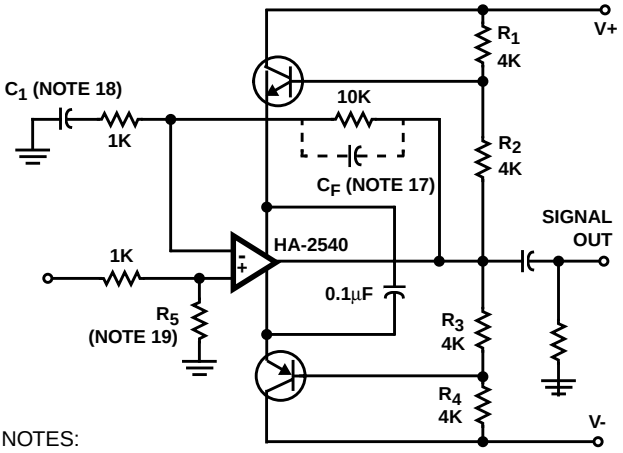


Typical Applications



NOTE: With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.

FIGURE 3. WIDEBAND SIGNAL SPLITTER



NOTES:

17. Used for experimental purposes. $C_F \cong 3pF$.
18. C_1 is optional ($0.001\mu F \rightarrow 0.01\mu F$ ceramic).
19. R_5 is optional and can be utilized to reduce input signal amplitude and/or balance input conditions. $R_5 = 500\Omega$ to $1k\Omega$.

FIGURE 4. BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING

Refer to Application Note AN541 For Further Application Information.

Typical Performance Curves

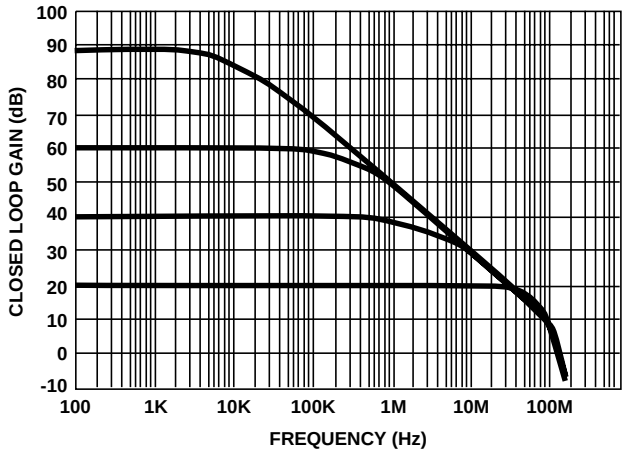


FIGURE 5. CLOSED LOOP FREQUENCY RESPONSE

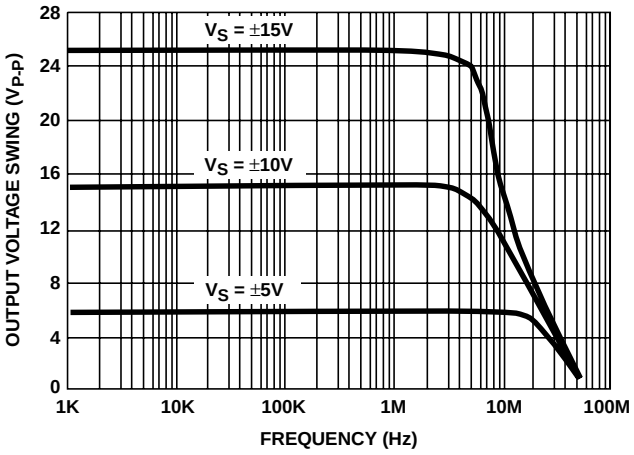


FIGURE 6. OUTPUT VOLTAGE SWING vs FREQUENCY

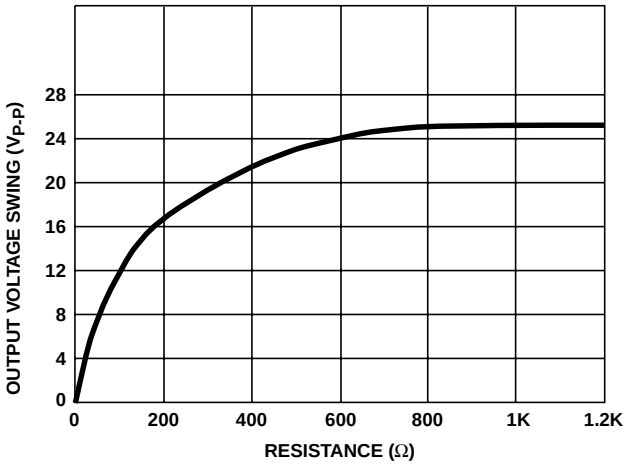


FIGURE 7. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

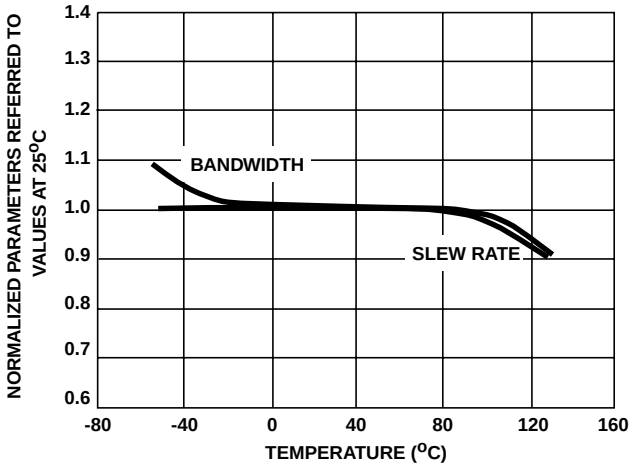


FIGURE 8. NORMALIZED AC PARAMETERS vs TEMPERATURE

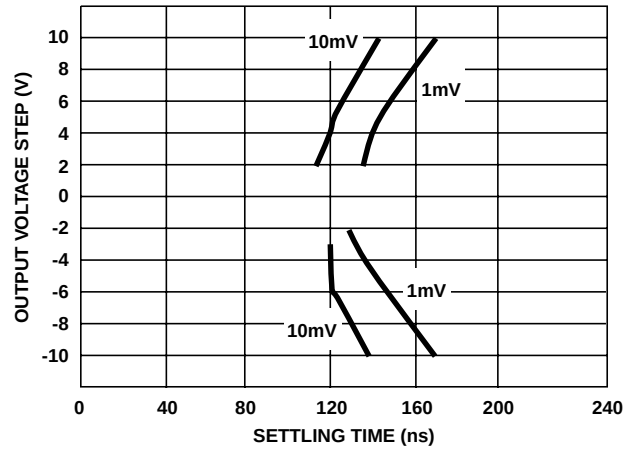


FIGURE 9. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

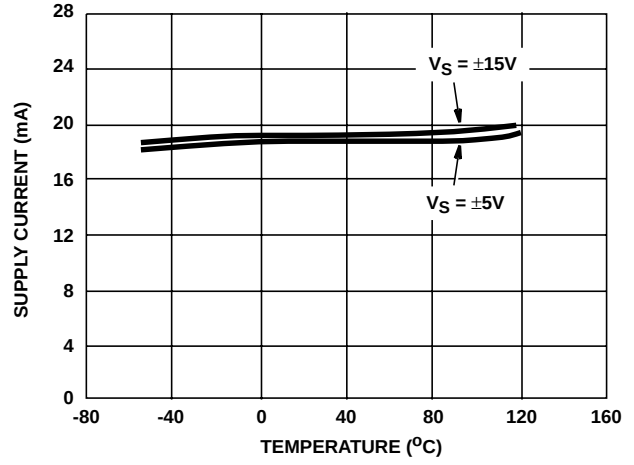


FIGURE 10. POWER SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

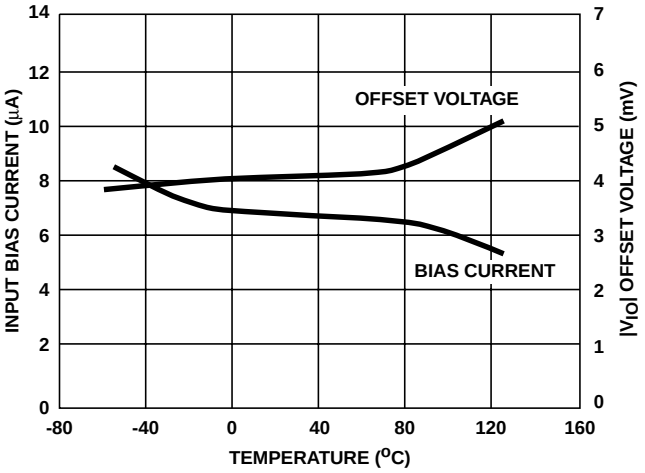


FIGURE 11. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

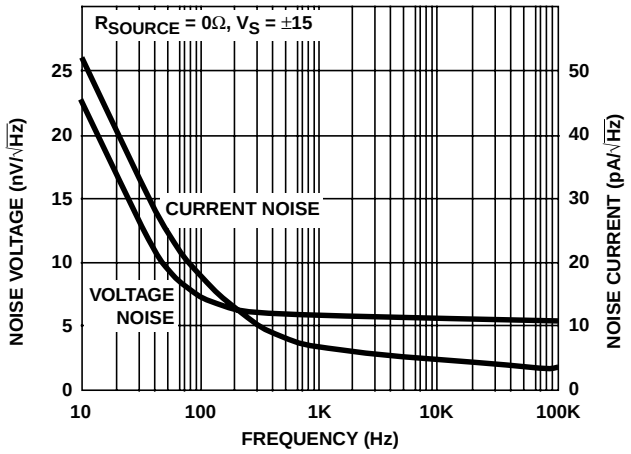
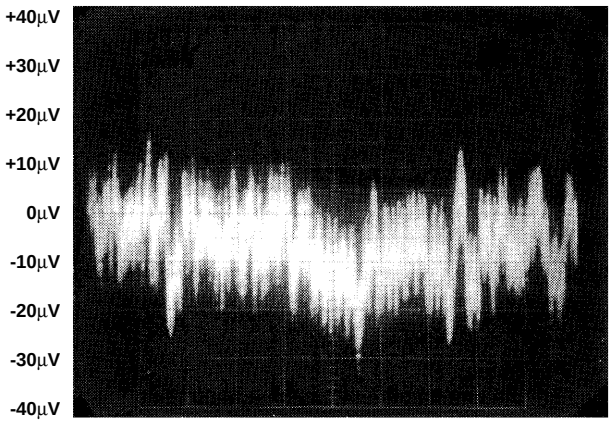


FIGURE 12. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY



Vertical Scale: 10mV/Div.
Horizontal Scale: 50ms/Div.

FIGURE 13. BROADBAND NOISE (0.1Hz TO 1MHz)

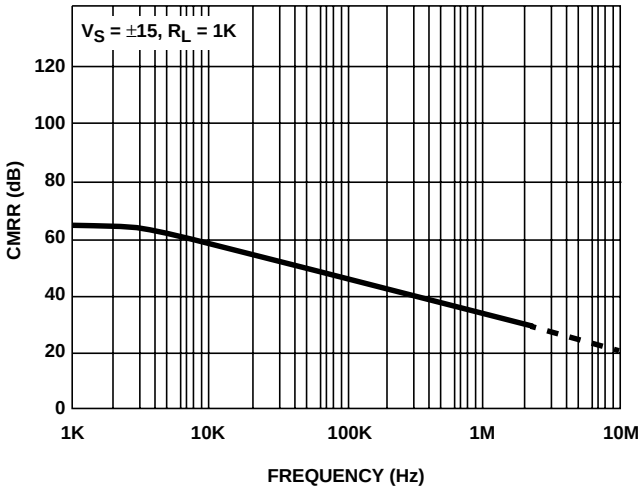


FIGURE 14. COMMON MODE REJECTION RATIO vs FREQUENCY

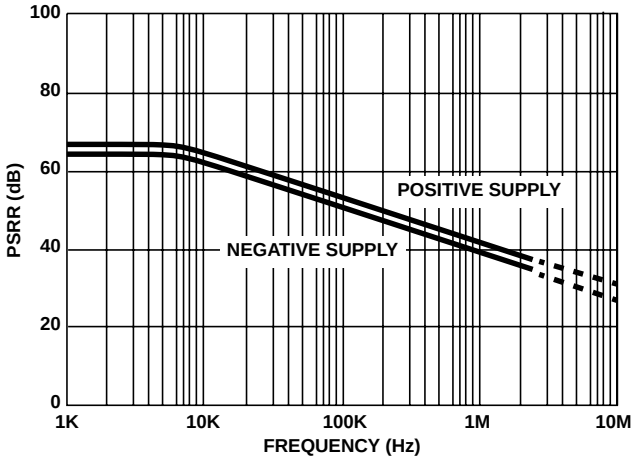


FIGURE 15. POWER SUPPLY REJECTION RATIO vs FREQUENCY

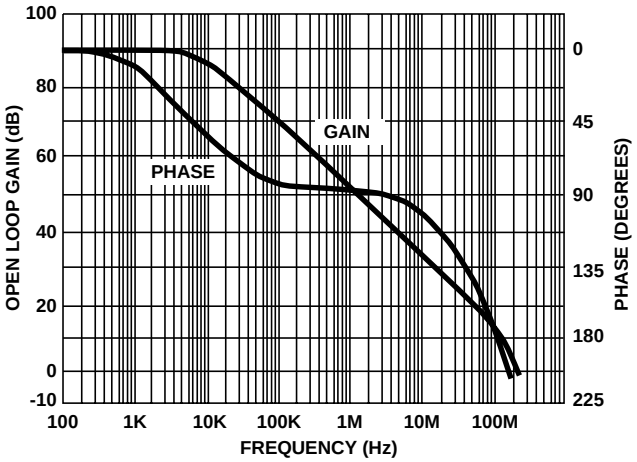


FIGURE 16. OPEN LOOP GAIN/PHASE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

62 mils x 76 mils x 19 mils
1575 µmx 1930µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

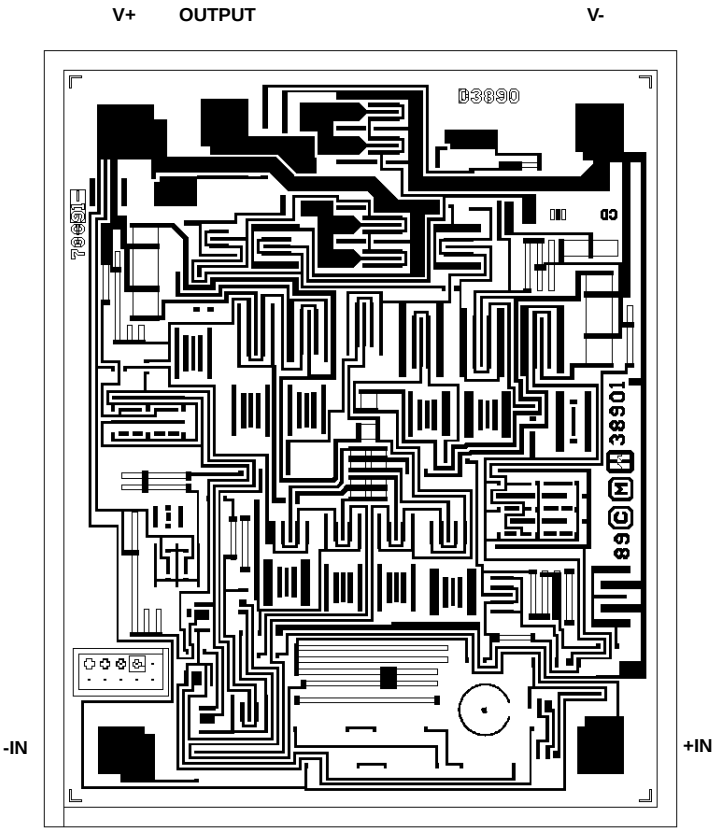
30

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2540



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