HIP4011

April 1994

Three Phase Brushless DC Motor Controller

Features

- **3A DC, 5A Peak Output Current**
- **16V Max. Rated Supply Voltage**
- **Built-in “Free-Wheeling” Diodes**
- **Output dv/dt Limited to Reduce EMI**
- **External Dynamic Brake Control Switch With Undervoltage Sense**
- **Thermal and Current Limiting Protects Against Locked Rotor Conditions**
- **Provides Analog Current Sense and Reference Inputs**
- **Decode Logic with Illegal Code Rejection**

Applications

- **Drive Spindle Motor Controller**
- **3 Phase Brushless DC Motor Controller**
- **Brushless DC Motor Driver for 12V Battery Powered Appliances**
- **Phased Driver for 12V DC Applications**
- **Logic Controlled Driver for Solenoids, Relays and Lamps**

Description

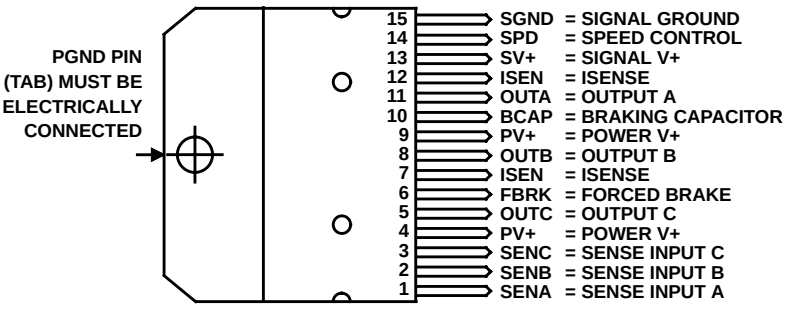
The HIP4011 motor driver is intended for three phase Brushless motor control at continuous output currents up to 3A. It accepts inputs from buffered Hall effect sensors and drives three motor windings, regulating the current through an external current sensing resistor, according to an analog control input. Output “freewheeling” diodes are built in and output dv/dt is limited to decrease the generated EMI. Thermal and current limiting are used to protect the device from locked rotor conditions. A brake control input forces all outputs to ground simultaneously to provide dynamic braking, and an internal voltage sensor does the same when the supply drops below a predetermined switch point. Power down braking energy is stored in an external capacitor.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4011IS	-40^{o}C to +85^{o}C	15 Pin Plastic SIP Surface Mount

Pinout

HIP4011 (SIP)
TOP VIEW



OUTPUT TRUTH TABLE

SENSOR INPUTS			FORCE BRAKE INPUT*	OUTPUTS		
A	B	C	FBRK	A	B	C
0	0	0	0	OFF	OFF	OFF
1	0	0	0	1	OFF	0
0	1	0	0	0	1	OFF
1	1	0	0	OFF	1	0
0	0	1	0	OFF	0	1
1	0	1	0	1	0	OFF
0	1	1	0	0	OFF	1
1	1	1	0	OFF	OFF	OFF
X	X	X	1	0	0	0

* Undervoltage and Force Brake logic truth table entries are identical.

“X” = Don’t Care

File Number **2939.3**

Absolute Maximum Ratings

Supply Voltage, SV+ or PV+. . . . . -1V to +16V
Referred to SGND or PGND (Note 1)
Output Current, Continuous 3A
Output Current, Peak (Note 2) 5A
Substrate (PGND) Current 1A
Logic Input Current. . . . . -20mA to +20mA
(Clamped to SV+ and SGND)

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
15 Lead SIP Power Package.	45°C/W	3°C/W

Power Dissipation (Note 3) 25W
Junction Temperature Range, Operating . . . . . +150°C
Storage Temperature Range. . . . . -55°C to +150°C
Power Dissipation
Up to +125°C without heat sink. 0.56W
Above +125°C without Heat Sink . . Derate Linearly at 22mW/°C
Up to +125°C with Infinite Heat Sink. 8.33W
Above +125°C with Infinite Heat Sink . . . . . .
. . . . . .Derate Linearly at 333mW/°C
Lead Temperature (During Soldering)
At a Distance 1/16 inch ±1/32 inch (1.59mm ±0.79mm)
from Case for 10s Max. . . . . +265°C

NOTES:

1. PV+ and SV+ are to be tied together, as are PGND and SGND.
2. Operating above the continuous current rating causes a decrease in operating life.
3. Derate power dissipation above case temperature of +75°C at 0.33 Watts/°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNITS
SUPPLY (SV+) CURRENT					
No Drive	Outputs Off	-	-	10	mA
With Drive	Outputs On	-	-	15	mA
LOGIC INPUT CURRENT					
Sensor Inputs	SENA, SENB & SENC = 0V to 3V	-0.5	-	-1.5	mA
Brake Input	FBRK = 0.8V to 2.4V	50	-	150	µA
LOGIC INPUT THRESHOLDS					
Sensor Inputs	Logic "0" Input Voltage	-	-	1.8	V
Sensor Inputs	Logic "1" Input Voltage	3	-	-	V
Brake Input	Logic "0" Input Voltage	-	-	0.8	V
Brake Input	Logic "1" Input Voltage	2.4	-	-	V
AMPLIFIER INPUT (SPD)					
Bias Current		-	-	700	nA
Offset Voltage		-	-	3	mV
Input Range (Linear)		0	-	1	V
Input Impedance		1	-	-	MΩ
System Bandwidth	(Note 1)	-	35	-	kHz
Current Limit	Rsense = 0.20Ω	-	5	-	A
THERMAL LIMIT					
Threshold		-	155	-	°C
Hysteresis		-	40	-	°C
OUTPUT DRIVERS					
On Saturation (See Note 5)	I_{OUT} = 3A, V_{PMOS} + V_{NMOS}	-	-	2.2	V
On Saturation (See Note 5)	I_{OUT} = 0.6A, V_{PMOS} + V_{NMOS}	-	-	0.44	V
Off Leakage	PV+ > V_{OUT} > PGND or I_{SEN}	-	-	1	mA
Slew Rate	(See Note 2)	-	0.5	-	V/µS

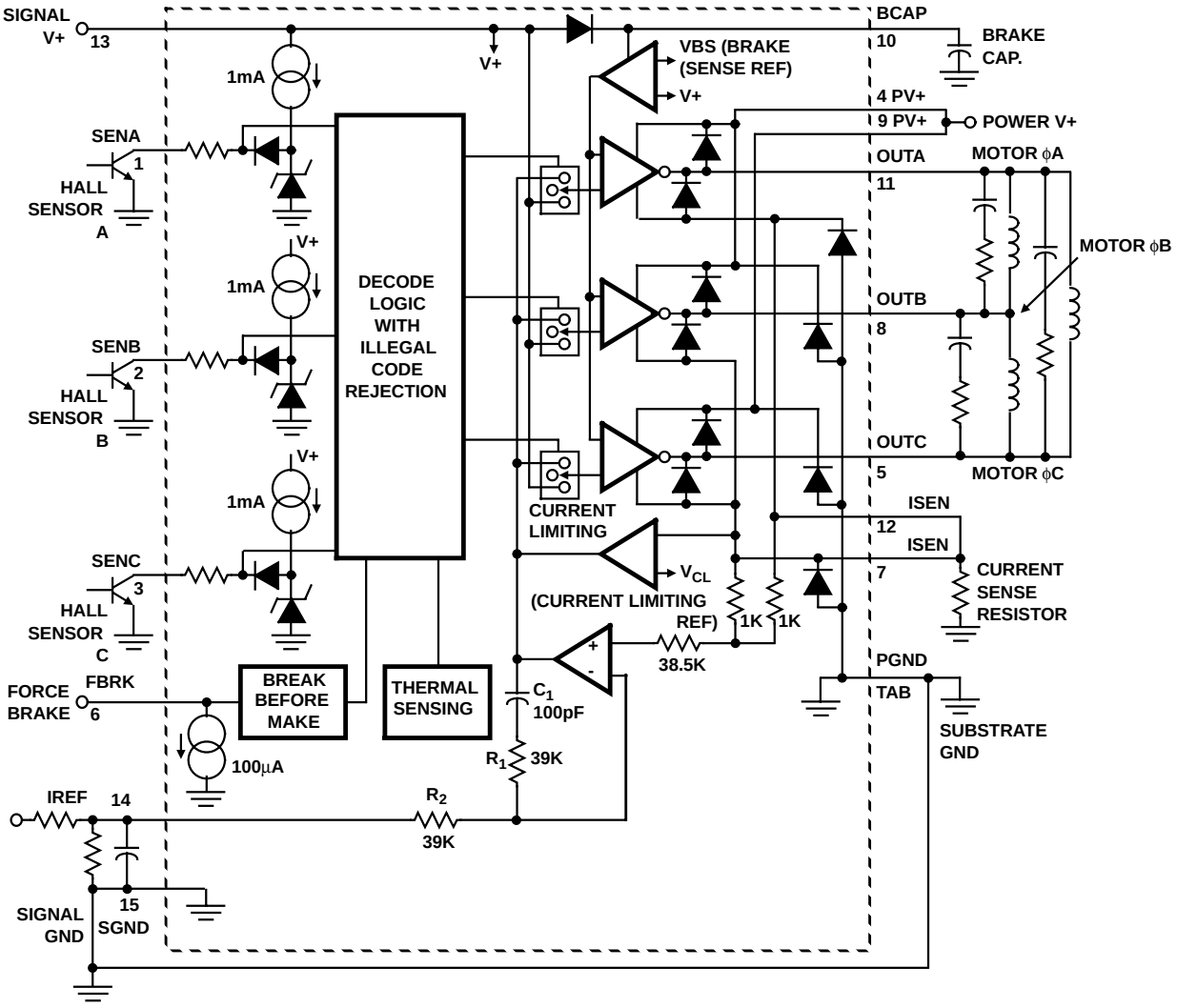
Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNITS
FREEWHEEL DIODES					
Forward Drop	I_{OUT} = 1A	-	-	1.5	V
INTERNAL BRAKE DRIVER					
Undervoltage Trip Point, PV+	(See Note 3)	2.7	-	3.3	V
Hysteresis	(See Note 4)	40	-	60	%
On Saturation	Each N_{MOS}, I_{OUT} = 3A	-	-	0.4	V
BRAKE CAPACITOR (BCAP)					
Discharge Leakage	SV+ = PV+ = 3V to 12V, BCAP = 10V	-	-	5	µA

NOTES:

1. The system bandwidth is fixed by an internal RC network around the amplifier.
2. Internal limiting of turn on and turn off drive is used to limit output dv/dt.
3. The braking action starts at the given trip point with a falling supply voltage.
4. Hysteresis causes the brake to be removed at a higher trip point with a rising supply voltage.
5. This value includes the combined voltage drops of one upper plus one lower switch at the indicated current.

Functional Block Diagram



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File Number