HM-6518

March 1997

1024 x 1 CMOS RAM

Features

- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . .180ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 2 TTL Loads**
- **High Noise Immunity**
- **On-Chip Address Register**
- **Two-Chip Selects for Easy Array Expansion**
- **Three-State Output**

Ordering Information

PACKAGE	TEMP. RANGE	180ns	250ns	PKG. NO.
CERDIP	-40°C to +85°C	HM1-6518B-9	HM1-6518-9	F18.3

Description

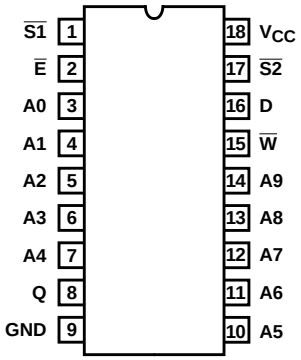
The HM-6518 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over-temperature.

Pinout

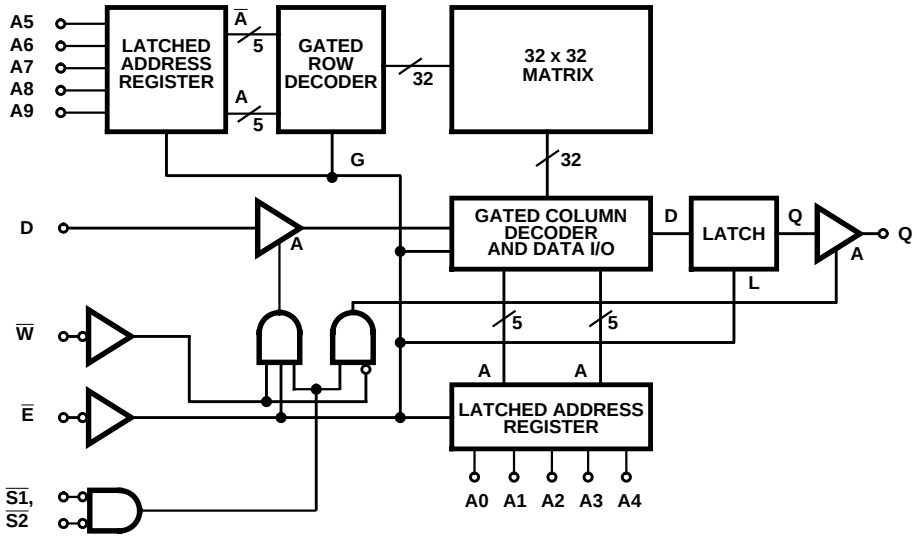
HM-6518
(CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
S	Chip Select
D	Data Input
Q	Data Output

File Number **2987.1**

Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high $\rightarrow$ output active.
3. Data latches: L high $\rightarrow$ Q = D; Q Latches on rising edge of L.
4. Address latches and gated decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6518B-9, HM-6518-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	$75^oC/W$	$15^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-6518B-9, HM-6518-9)

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Standby Supply Current		ICCSB	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
Operating Supply Current (Note 1)		ICCOP	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
Data Retention Supply Current	HM-6518B-9	ICCDR	-	5	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
	HM-6518-9		-	10	µA	
Data Retention Supply Voltage		VCCDR	2.0	-	V	
Input Leakage Current		II	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
Output Leakage Current		IOZ	-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
Input Low Voltage		VIL	-0.3	0.8	V	V_{CC} = 4.5V
Input High Voltage		VIH	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
Output Low Voltage		VOL	-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
Output High Voltage		VOH	2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

PARAMETER	SYMBOL	MAX	UNITS	TEST CONDITIONS
Input Capacitance (Note 2)	CI	6	pF	f = 1MHz, All measurements are referenced to device GND
Output Capacitance (Note 2)	CO	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ± 10%; T_A = -40°C to +85°C (HM-6518B-9, HM-6518-9)

PARAMETER	SYMBOL	LIMITS				UNITS	TEST CONDITIONS
		HM-6518B-9		HM-6518-9			
		MIN	MAX	MIN	MAX		
Chip Enable Access Time	(1) TELQV	-	180	-	250	ns	(Notes 1, 3)
Address Access Time	(2) TAVQV	-	180	-	250	ns	(Notes 1, 3, 4)
Chip Select Output Enable Time	(3) TSLQX	5	120	5	160	ns	(Notes 2, 3)
Write Enable Output Disable Time	(4) TWLQZ	-	120	-	160	ns	(Notes 2, 3)
Chip Select Output Disable Time	(5) TSHQZ	-	120	-	160	ns	(Notes 2, 3)
Chip Enable Pulse Negative Width	(6) TELEH	180	-	250	-	ns	(Notes 1, 3)
Chip Enable Pulse Positive Width	(7) TEHEL	100	-	100	-	ns	(Notes 1, 3)
Address Setup Time	(8) TAVEL	0	-	0	-	ns	(Notes 1, 3)
Address Hold Time	(9) TELAX	40	-	50	-	ns	(Notes 1, 3)
Data Setup Time	(10) TDVWH	80	-	110	-	ns	(Notes 1, 3)
Data Hold Time	(11) TWHDX	0	-	0	-	ns	(Notes 1, 3)
Chip Select Write Pulse Setup Time	(12) TWLSH	100	-	130	-	ns	(Notes 1, 3)
Chip Enable Write Pulse Setup Time	(13) TWLEH	100	-	130	-	ns	(Notes 1, 3)
Chip Select Write Pulse Hold Time	(14) TSLWH	100	-	130	-	ns	(Notes 1, 3)
Chip Enable Write Pulse Hold Time	(15) TELWH	100	-	130	-	ns	(Notes 1, 3)
Write Enable Pulse Width	(16) TWLWH	100	-	130	-	ns	(Notes 1, 3)
Read or Write Cycle Time	(17) TELEL	280	-	350	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

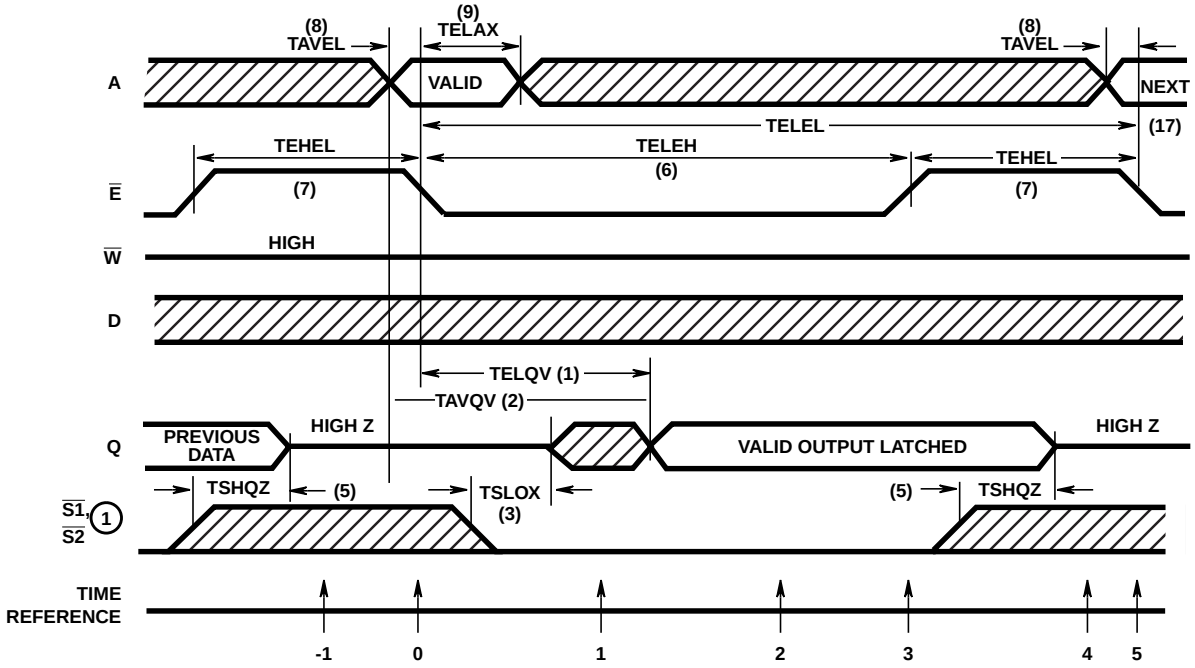


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Memory Disabled
0	↘	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high, the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high, forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Timing Wavforms (Continued)

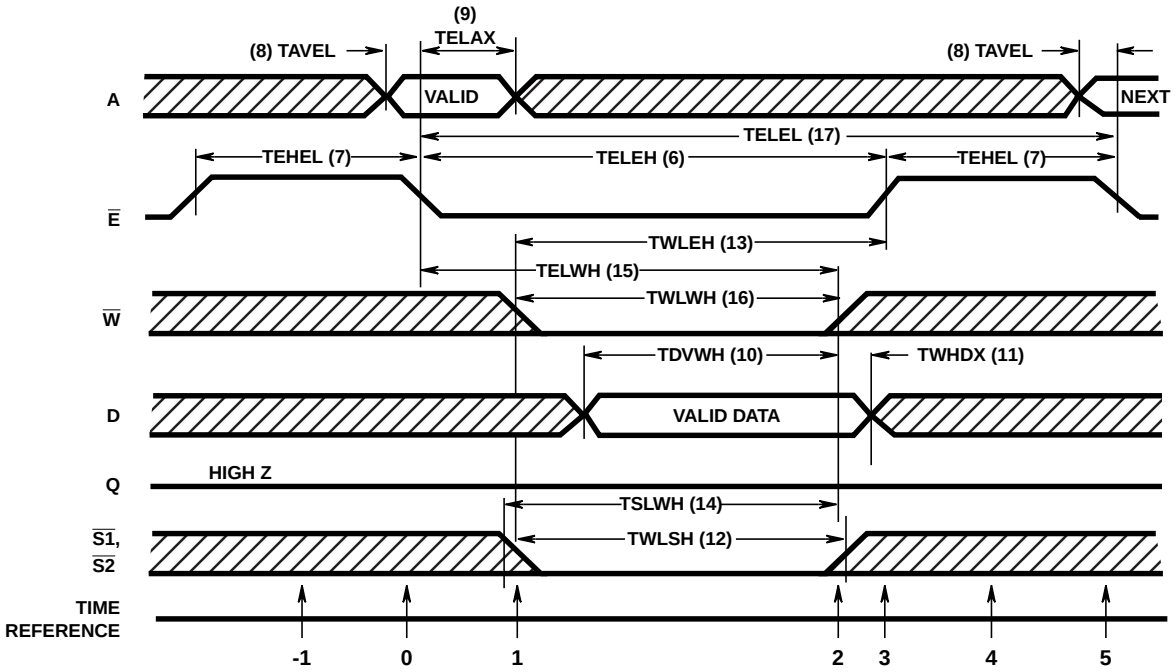


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Memory Disabled
0	↓	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↑	L	X	V	Z	Data is Written
3	↑	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

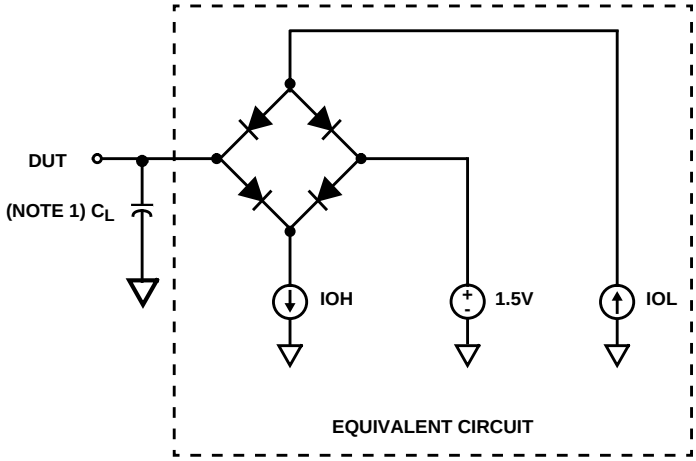
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method, allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

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