HI-5701/883

June 1994

6-Bit, 30 MSPS Flash A/D Converter

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **30 MSPS with No Missing Codes**
- **20MHz Full Power Input Bandwidth**
- **No Missing Codes Over Temperature**
- **Sample and Hold Not Required**
- **Single +5V Supply Voltage**
- **CMOS/TTL**
- **Overflow Bit**

Applications

- **Video Digitizing**
- **Radar Systems**
- **Medical Imaging**
- **Communication Systems**
- **High Speed Data Acquisition Systems**

Description

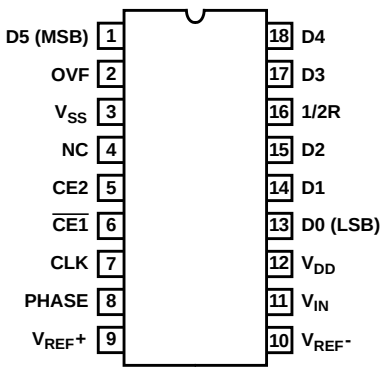
The HI-5701/883 is a monolithic, 6-bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701/883 delivers ±0.7 LSB differential nonlinearity while consuming only 250mW (typical) at 30 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 7-bit resolution.

Ordering Information

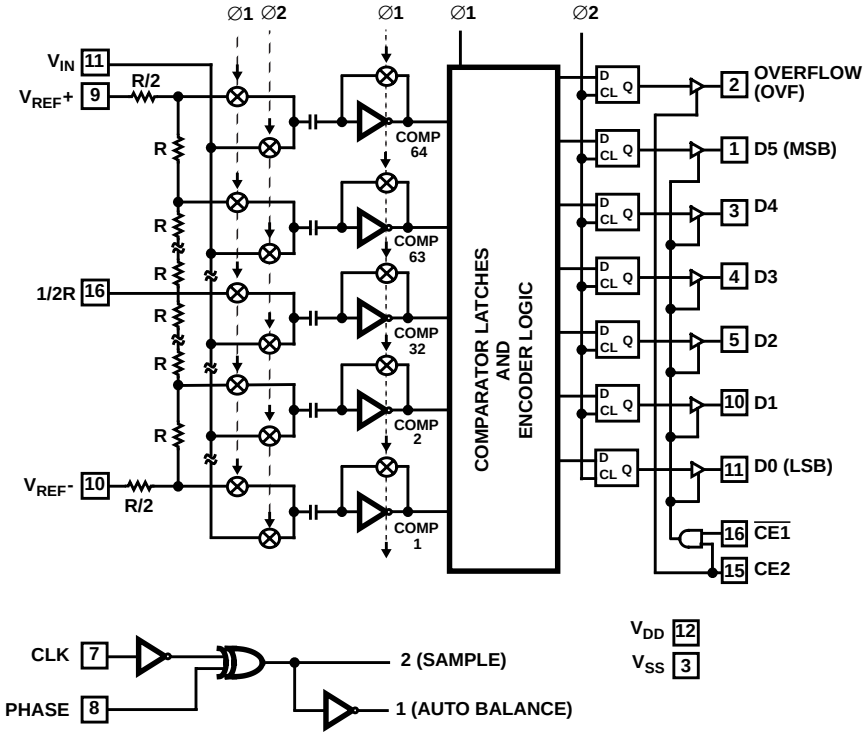
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5701T/883	-55°C to +125°C	18 Lead CerDIP

Pinout

HI-5701/883
(18 LEAD CERDIP)
TOP VIEW



Functional Block Diagram



Spec Number **512031**
File Number **3378**

Pin Description

PIN #	NAME	DESCRIPTION
1	D5	Bit 6, Output (MSB)
2	OVF	Overflow, Output
3	V_{SS}	Digital Ground
4	NC	No Connection
5	CE2	Three-State Output Enable Input, Active high (See Truth Table)
6	$\overline{CE1}$	Three-State Output Enable Input, Active Low (See Truth Table)
7	CLK	Clock Input
8	PHASE	Sample Clock Phase Control Input. When Phase is Low, Sample Unknown (ϕ1) occurs when the Clock is Low and Auto Balance (ϕ2) occurs when the Clock is High (See Phase Control Table)
9	V_{REF}+	Reference Voltage Positive Input
10	V_{REF}-	Reference Voltage Negative Input
11	V_{IN}	Analog Signal Input
12	V_{DD}	Power Supply, +5V
13	D0	Bit 1, Output (LSB)
14	D1	Bit 2, Output
15	D2	Bit 3, Output
16	1/2R	Reference Ladder Midpoint
17	D3	Bit 4, Output
18	D4	Bit 5, Output

Chip Enable Truth Table

$\overline{CE1}$	CE2	D0 - D5	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care.

Phase Control

CLOCK	PHASE	INTERNAL GENERATION
0	0	Sample Unknown (ϕ2)
0	1	Auto Balance (ϕ1)
1	0	Auto Balance (ϕ1)
1	1	Sample Unknown (ϕ2)

Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS} . . . . . $(V_{SS} - 0.5) < V_{DD} < +7.0V$
Analog and Reference Input Pins. . $(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)$
Digital I/O Pins . . . . . $(V_{SS} - 0.5) < V_{I/O} < (V_{DD} +0.5V)$
Operating Temperature Range
HI1-5701T/883 . . . . . -55^oC to $+125^oC$
Junction Temperature . . . . . $+175^oC$
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering, 10s) . . . . . 300^oC
ESD Clasification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1-5701T/883.	$70^oC/W$	$28^oC/W$

Power Dissipation at $+75^oC$ (Note 1)
HI1-5701T/883. . . . . 1.4mW
Power Dissipation Derating Factor Above $+75^oC$
HI1-5701T/883. . . . . $14mW/^oC$
Reliability Information
Transistor Count 4815
Worst Case Density . . . . . $3.05 \times 10^4 A/cm^2$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF}- = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
ACCURACY							
Integral Linearity Error (Best Fit Method)	INL	F_S = 20MHz, f_{IN} = DC	1	$+25^oC$	-	±1.25	LSB
			2, 3	$+125^oC$, -55^oC	-	±2.0	LSB
		F_S = 30MHz, f_{IN} = DC	1	$+25^oC$	-	±1.5	LSB
			2, 3	$+125^oC$, -55^oC	-	±2.5	LSB
Differential Linearity Error (Guaranteed No Missing Codes)	DNL	F_S = 20MHz, f_{IN} = DC	1	$+25^oC$	-	±0.6	LSB
			2, 3	$+125^oC$, -55^oC	-	±0.75	LSB
		F_S = 30MHz, f_{IN} = DC	1	$+25^oC$	-	±0.75	LSB
			2, 3	$+125^oC$, -55^oC	-	±1.0	LSB
Offset Error (Adjustable to Zero)	VOS	F_S = 20MHz, f_{IN} = DC	1	$+25^oC$	-	±2.0	LSB
			2, 3	$+125^oC$, -55^oC	-	±2.5	LSB
Full Scale Error (Adjustable to Zero)	FSE	F_S = 20MHz, f_{IN} = DC	1	$+25^oC$	-	±2.0	LSB
			2, 3	$+125^oC$, -55^oC	-	±2.5	LSB
ANALOG INPUT							
Analog Input Resistance	R_{IN}	V_{IN} = 4V	1	$+25^oC$	4	-	MΩ
			2, 3	$+125^oC$, -55^oC	4	-	MΩ
Analog Input Bias Current	I_B	V_{IN} = 0V, 4V	1	$+25^oC$		±1.0	µA
			2, 3	$+125^oC$, -55^oC		±1.0	µA
REFERENCE INPUT							
Total Reference Resistance	R_L		1	$+25^oC$	250	-	Ω
			2, 3	$+125^oC$, -55^oC	235	-	Ω

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF}- = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNIT
					MIN	MAX	
DIGITAL INPUTS							
Input High Voltage	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Input Low Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0V, +5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±1	µA
DIGITAL OUTPUTS							
Output Leakage	I_{OZ}	CE2 = 0V, V_O = 0V, 5V	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Output Logic Source Current	I_{OH}	V_O = 4.5V	1	+25°C	-3.2	-	mA
			2, 3	+125°C, -55°C	-3.2	-	mA
Output Logic Sink Current	I_{OL}	V_O = 0.4V	1	+25°C	3.2	-	mA
			2, 3	+125°C, -55°C	3.2	-	mA
POWER SUPPLY REJECTION							
Offset Error PSRR	ΔVOS	V_{DD} = 5V ±10%	1	+25°C	-	±1.0	LSB
			2, 3	+125°C, -55°C	-	±1.5	LSB
Gain Error PSRR	ΔFSE	V_{DD} = 5V ±10%	1	+25°C	-	±1.0	LSB
			2, 3	+125°C, -55°C	-	±1.5	LSB
POWER SUPPLY CURRENT							
Supply Current	I_{DD}	F_S = 30MHz	1	+25°C	-	60	mA
			2, 3	+125°C, -55°C	-	75	mA

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF}- = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNIT
					MIN	MAX	
Maximum Conversion Rate		No Missing Codes	9	+25°C	30	-	MSPS
			10, 11	+125°C, -55°C	30	-	MSPS
Data Output Enable Time	t_{EN}		9	+25°C	-	20	ns
			10, 11	+125°C, -55°C	-	20	ns
Data Output Disable Time	t_{DIS}		9	+25°C	-	20	ns
			10, 11	+125°C, -55°C	-	20	ns
Data Output Delay	t_{OD}		9	+25°C	-	20	ns
			10, 11	+125°C, -55°C	-	20	ns
Data Output Hold	t_H		9	+25°C	10	-	ns
			10, 11	+125°C, -55°C	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF}- = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNIT
				MIN	MAX	
Minimum Conversion Rate		No Missing Codes	+25°C, +125°C, -55°C	-	0.125	MSPS

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Die Characteristics

DIE DIMENSIONS:
2220µm x 3320µm x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

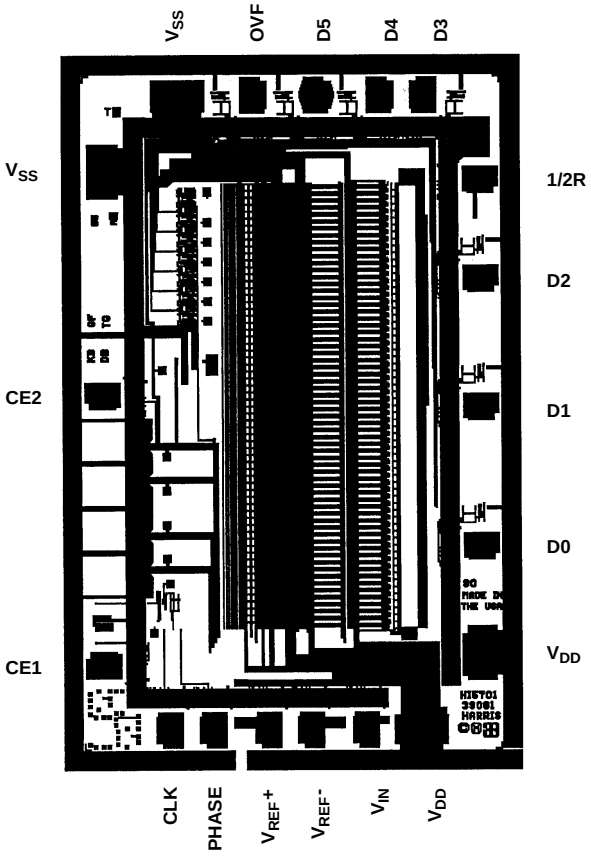
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

WORST CASE CURRENT DENSITY:
3.05×10^4 A/cm^2

Metallization Mask Layout

HI-5701/883



Timing Waveforms

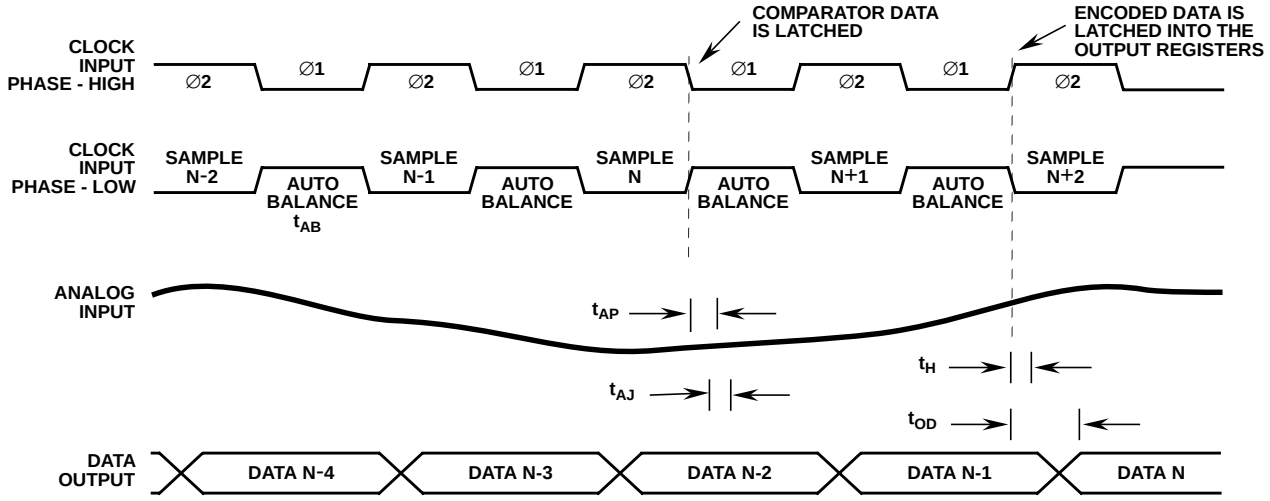


FIGURE 1. INPUT-TO-OUTPUT TIMING

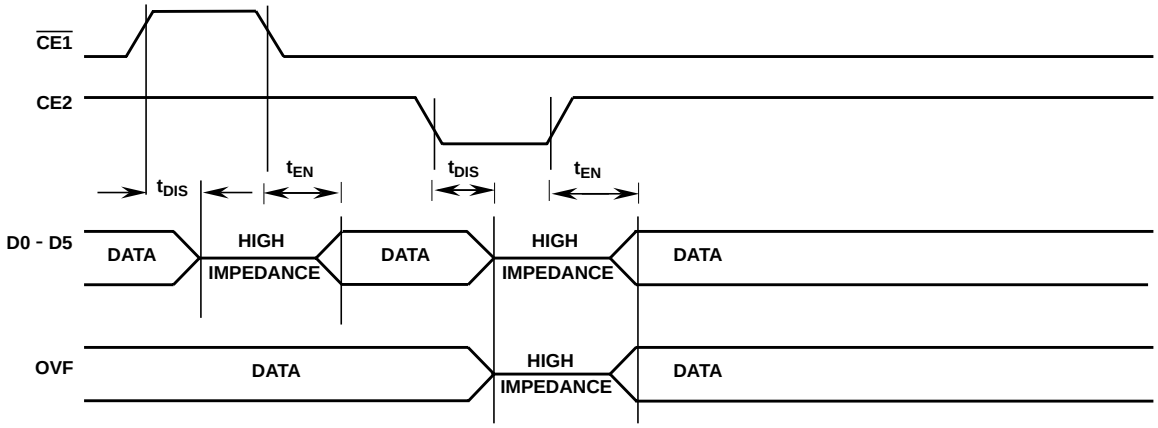
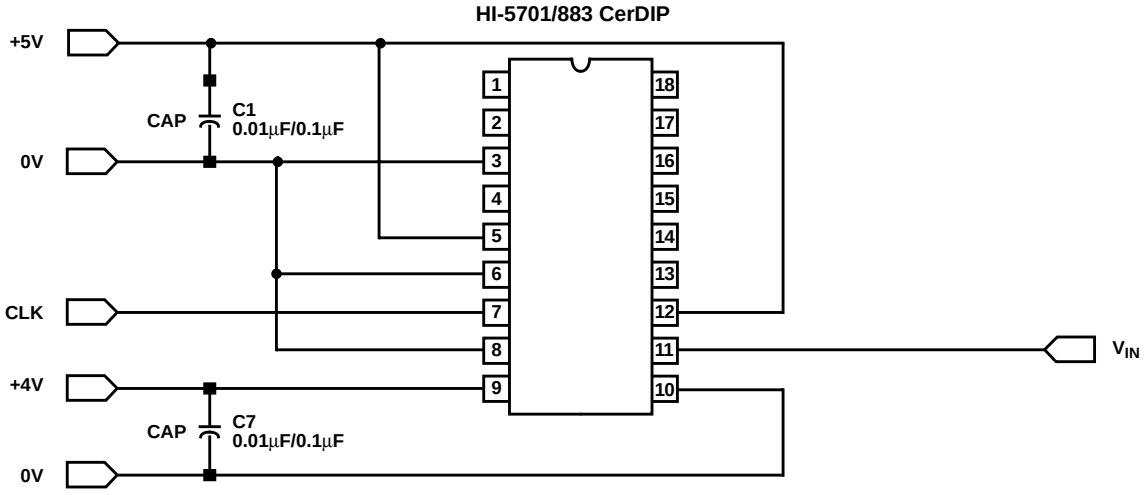


FIGURE 2. OUTPUT ENABLE TIMING

Burn-In Circuit

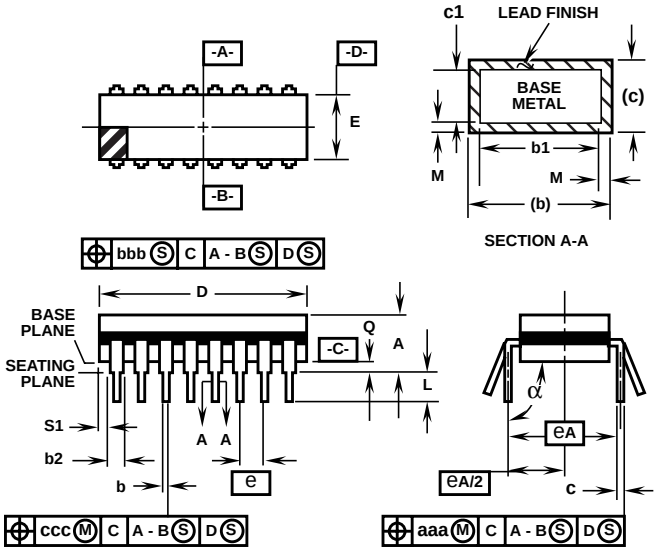


NOTES:

1. Power supply and the reference voltage input to be decoupled by 0.01µF in parallel with 1µF capacitor
2. Clock input is a pulse with 1:10 duty cycle, approximately 100KHz and 0V to 4V amplitude
3. V_{IN}, analog input is a slow triangular waveform (F_{IN} = 10KHz) and 0V to 4V amplitude
4. All supplies to be protected with <7V zener diodes

Packaging

FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE



F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.

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