

# ACS280MS

# Radiation Hardened 9-Bit Odd/ Even Parity Generator Checker

January 1996

#### Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96708 and Intersil' QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose ......>300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10<sup>-10</sup> Errors/Bit/Day (Typ)
- Dose Rate Upset ......>10<sup>11</sup> RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability.....>10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range .....-55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range ...... 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay ...... 23ns (Max), 15ns (Typ)

#### Description

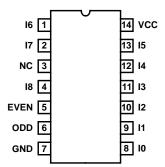
The Intersil ACS280MS is a Radiation Hardened 9-bit odd/even parity generator checker device. Both odd and even parity outputs are available for generating or checking parity for words up to 9 bits long. Even parity is indicated (EVEN output high) when an even number of data inputs are high. Odd parity is indicated (ODD output high) when an odd number of data inputs are high. Parity checking for larger words can be accomplished by tying EVEN output to any input of an additional ACS280MS.

The ACS280MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family.

The ACS280MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

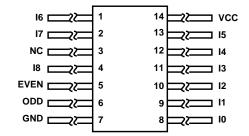
#### **Pinouts**

14 PIN CERAMIC DUAL-IN-LINE MIL-STD-1835 DESIGNATOR, CDIP2-T14, LEAD FINISH C TOP VIEW



14 PIN CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR, CDFP3-F14
LEAD FINISH C

TOP VIEW



## **Ordering Information**

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670801VCC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead SBDIP
5962F9670801VXC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead Ceramic Flatpack
ACS280D/Sample	25°C	Sample	14 Lead SBDIP
ACS280K/Sample	25°C	Sample	14 Lead Ceramic Flatpack
ACS280HMSR	25°C	Die	Die

# Functional Diagram I6 (1) ÂE (5) I5 (13) I4 (12) I3 (11) ÂO (6) I2 (10) NC = 3 **VDD** = 14 **GND** = 7

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

#### ACS280MS

#### Die Characteristics

#### **DIE DIMENSIONS**

88 mils x 88 mils 2.24mm x 2.24mm

#### **METALLIZATION:**

Type: AISi

Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

#### **GLASSIVATION:**

Type: SiO<sub>2</sub>

Thickness: 8kÅ ±1kÅ

# WORST CASE CURRENT DENSITY:

 $<2.0 \times 10^5 \text{ A/cm}^2$ 

#### **BOND PAD SIZE:**

> 4.3 mils x 4.3 mils  $> 110\mu m$  x  $110\mu m$ 

## Metallization Mask Layout

#### ACS280MS

