User's Manual | January 1999 | File Number 3637.1

DDC Evaluation Platform

The HSP50016-EV is the evaluation board for the HSP50016 Digital Down Converter (DDC). It provides a mechanism for rapid evaluation and prototyping. The HSP50016-EV consists of a series of busses which provide input, output, and control to the DDC. These busses are brought out through dual 96 Pin connectors to support daisy chaining HSP50016-EVs with other Intersil evaluation boards for multichip prototyping and evaluation.

For added flexibility, the input and control busses can be driven by registers on-board the HSP50016-EV which have been down loaded with data via the parallel printer port of an IBM PC™ or compatible. In addition, the DDC output can be read into the PC via the status lines of the parallel port. Together, the I/O and Control Registers can be used to drive the target DDC with a PC based vector set while collecting output data on the PC's disk.

Jumper selectable clock sources provide three different methods of clocking the part under evaluation. In mode one, the clock signal is generated under PC based software control. In mode two, the HSP50016-EV's on-board oscillator may be selected as the clock source. In mode three, the user may provide an external clock through the 96 pin input connector.

The HSP50016-EV was built into a 3U Euro-Card form factor with dual 96 Pin Input/Output connectors. The I/O connectors conform to the VME J2/P2 Connector Standard.

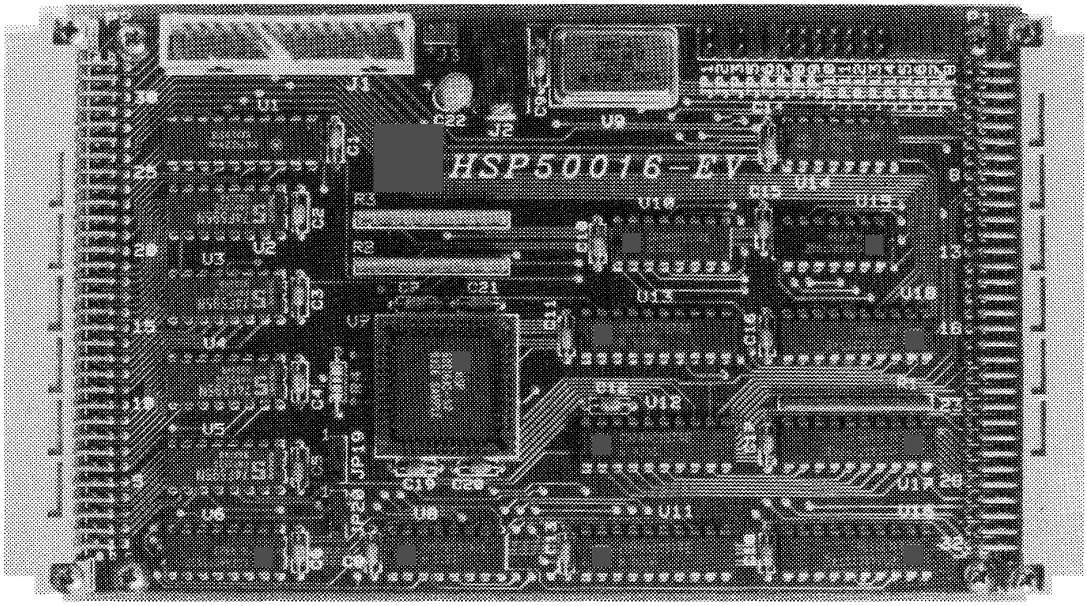
Features

- Single HSP50016-EV May be Used to Evaluate the HSP50016
- May be Daisy Chained to Support Evaluation of Multi-Chip Solutions
- Parallel Port Interface to Support IBM PC™ Based Evaluation and Control
- Three Clocking Modes for Flexibility in Performance Analysis and Prototyping
- Dual 96-Pin Input/Output Connectors Conforming to the VME J2/P2 Connector Standard

Applications

- PC Based Performance Analysis of HSP50016
- Rapid Prototyping

HSP50016 Evaluation Platform



Getting Started

This section describes the initial evaluation system setup for the HSP50016-EV evaluation board. The system setup consists of the evaluation board, software installation, and system test to verify proper operation of the board.

Assembly

As part of the initial assembly, the HSP50016-EV must be provided with the default jumper configuration to ensure proper operation with the system test software. Each board leaving the factory is supplied with the default configuration as shown in Figure 1.

Before using the board with the supplied software, power must be supplied to the board, and the HSP50016-EV must be connected to the parallel port of the PC.

- Power is provided to the board by connecting the wall mount power supply provided to connector J2. As an alternative, power may be supplied by a standard 5V ±5% supply through the J3 header or the HSP50016-EV's 96 Pin DIN connectors P1 or P2.
- The HSP50016-EV is connected to the target PC by connecting the HSP50016-EV's 26 Pin connector J1 to the PC's parallel port using the supplied ribbon cable.

System Requirements for the Evaluation Board Software

The PC system targeted to run the HSP50016-EV software (DDC-SOFT) and interface with the evaluation board must meet the following requirements:

- IBM PC/XT/AT, PS/2, or 100% compatible with a minimum of 640K of random access memory (RAM) (DDC-SOFT does not require extended memory)
- At least 250kB of free disk space on the hard disk
- DOS Version 3.0 or higher
- One parallel port with 27 Pin D-Sub connector

Software Installation

The distribution diskette contains a program called INSTALL.EXE which installs the DDC-SOFT software onto the target hard disk. Note: The steps in this section assume you are installing DDC-SOFT from a diskette in drive A: onto a hard drive C:. If a different configuration is used, substitute the letter of the drive where the diskette is located for drive A: Substitute the letter for the hard drive for drive C:.

To start the installation program:

Make sure computer is on and the DOS prompt is displayed.

- Type: C:<Enter>

Create a subdirectory to contain the DDC-SOFT Programs by typing:

- MD \DDCSOFT <Enter>

Change current directory to the DDCSOFT directory

- CD \DDCSOFT <Enter>

Start the installation process by typing:

- A:INSTALL <Enter>

The INSTALL program downloads the DDC-SOFT programs, DDCCTRL and DDCCMD, to the DDCSOFT subdirectory on the target hard drive. In addition, a subdirectory called DDC_CHK is created into which files used to perform functional verification are downloaded.

Modifications to AUTOEXEC.BAT

To run the DDC-SOFT programs, DOS must be able to find the executable files. To ensure that DOS can always find the DDC-SOFT executables, modify the search path to include the location of the DDC-SOFT directory. For example, if the DDC-SOFT programs are installed on drive C: in a subdirectory called\DDCSOFT, add the following line to the end of the existing Path command in the AUTOEXEC.BAT file:

- ;C:\DDCSOFT

If your AUTOEXEC.BAT file does not contain a PATH command, add the following command to the file:

PATH=C:\DDCSOFT

- Reboot the PC so that the search path changes will take effect.

System Test

Test software is provided to verify operation of the HSP50016-EV Board. Prior to performing the system test, it is assumed that the evaluation board has been assembled and configured as described above, power has been applied to the board, and the 26 Pin Connector J1 on board the HSP50016-EV has been connected to the parallel port of the target PC via the supplied cable. The system test is initiated by the following:

Change the current directory to that which contains the software required for the system test by typing:

- CD C:\DDCSOFT\DDC_CHK <Enter>

Run the system test software by typing:

- DDCCHK <Enter>

The DDCCHK.EXE batch file makes use of the Command Line Interface (see Command Line Interface Section) to initialize the evaluation board, clock a data vector through the HSP50016-EV, and store the output to a file. The output file is then compared, using the DOS command COMP, to a file containing a set of vectors generated by a properly functioning board. If the TEST_IN.DAT and TEST.OUT.DAT files match, the assembled board passes operational verification.

When a successful compare has been done, the software message returned is:

- Comparing files TEST_OUT.DAT and CMPRFILE.DAT
- FC: No differences encountered

The most common causes of test failures are incorrect board jumper settings, incorrect comm port selection, or a corrupted eval.cfg file. It is helpful to delete the file TEST_OUT.DAT, prior to the test, to ensure that DDC.CHK runs properly and that a new TEST_OUT.DAT file was created.

NOTE: if the operating system precedes DOS 6.0, the user should answer NO to the COMP command prompt to compare additional files. DOS Version 6.0 and above use a different file compare command, so this step is not necessary. DDCCHK checks the version automatically and executes the proper compare routine.

The DDCCHK system test assumes that the LPT1 printer port is being used for communication with the HSP50016-EV. If another printer port is used, the Command Line Interface, DDCCMD, must be used to configure the software for using the correct port (see DDCCMD's PPC and PP# command).

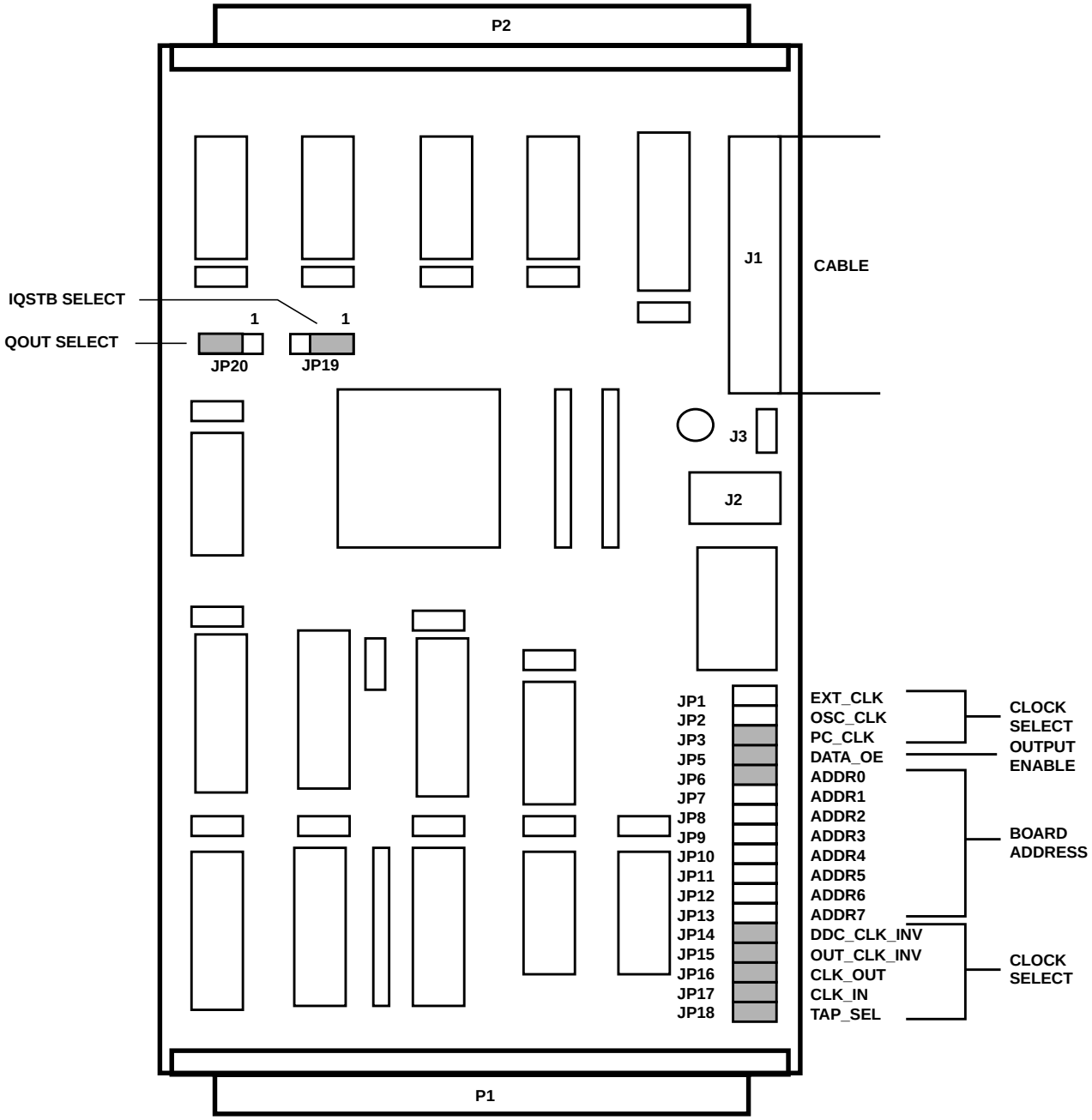


FIGURE 1. LAYOUT OF HSP50016-EV SHOWING DEFAULT JUMPER CONFIGURATION

HSP50016-EV Control Panel Software

The HSP50016-EV Control Panel is a graphical user interface for controlling the operation of the HSP50016-EV Board via an IBM PC or compatible. The control panel, shown in Figure 3, supports loading the HSP50016's control words; setting the state of control inputs; and specifying files which serve as the sources and destinations for the HSP50016's data and TAP inputs and outputs. Operation of the control panel software is dependent on the clock source provided to the HSP50016-EV as specified in the clock select portion of the control panel. The HSP50016-EV Control Panel is invoked by typing:

DDCCTRL <Enter>

Port Configuration

Communication between the Control Panel software and the evaluation board requires that the software knows which one of the PC's parallel ports is being used for communication with the HSP50016-EV and which board address the HSP50016-EV has been configured for. The default configuration assumes that LPT1 is being used and that the HSP50016-EV has been configured for a board address of 0. The Port Configuration can be inspected by opening up the port configuration window using the F9 function key. As shown in Figure 4, the window displays the available parallel ports and their addresses. Also displayed are the current port and HSP50016-EV board address being used by the Control Panel software.

The current port and HSP50016-EV address are changed by opening up the Port Configuration Window, using the up/down arrow keys to select the desired parameter, and toggling the space bar to change the selection. Proper operation of the control panel software requires that the HSP50016-EV board address specified in the port configuration window matches the address jumpered in the Address Selection Section of the HSP50016-EV's headers JP6-13.

Clock Select

The Clock Select portion of the control panel is used to tell the Control Panel software which of four different clock sources is being supplied to the HSP50016-EV. The choices include one of two different software generated clocks (Manual CLK or Port CLK), an oscillator clock provided by the HSP50016-EV (Oscillator CLK), or an externally supplied clock (External CLK). The clock mode selected must be consistent with the Clock Select jumper position in the HSP50016-EV's headers JP1-3. If either Manual CLK or Port CLK are specified in the Control Panel, the clock select jumper must be inserted in JP3. If either Oscillator CLK or External CLK is specified, the jumper must be inserted in JP2 or JP1 respectively.

In Manual CLK mode, single clock pulses are sent to the HSP50016 by depressing the F2 function key. The clock pulse is software generated by setting and clearing the PCCLK bit of the Control Register U16 on the HSP50016-EV. After each clock the HSP50016-EV's data outputs are inspected to see if they are ready to be read. If so, the data is read into the PC for display in the Control Panel. In this mode, file input and output are supported (See File I/O Select Section).

In Port CLK mode, a free running clock is sent to the HSP50016. The clock is started and stopped by depressing the F2 function key. The clock pulses are software generated by continually setting and clearing the PCCLK bit of Control Register U16. After each clock the HSP50016-EV's data outputs are inspected to see if they are ready to be read. If so, the data is read into the PC for display in the Control Panel. In this mode, file input and output are supported (see File I/O Select Section).

In Oscillator CLK mode, the HSP50016 is supplied with a clock by the oscillator on board the HSP50016-EV. In this mode, the Control Panel can be used for modifying $\overline{\text{RESET}}$ and $\overline{\text{IQSTRT}}$, the control words, and the data and TAP inputs to the DDC. However, the software is unable to provide file based I/O to the evaluation board since the data rate provided by the oscillator is much greater than that possible through the parallel port of the PC. As a result, the Control Panel disables file based I/O and the display of DDC output in this mode.

Operation in External CLK mode is identical to that in Oscillator CLK mode, except that the HSP50016 is supplied with a clock through the 96 Pin DIN connector P1 on the HSP50016-EV. Because this clock is asynchronous to the PC, file based I/O and the DDC output displays are disabled.

The clocking mode used by the control panel is indicated by the position of the "check mark" symbol within the Clock Select portion of the Control Panel. A different clocking mode may be selected by positioning the "check mark" symbol in front of the desired clocking mode. The position of the "check mark" is changed by using the cursor keys to move the active window to the desired position and then toggling the space bar to move the "check mark".

File I/O Select

The File I/O Select portion of the Control Panel allows the user to specify files which can be used as an input data source or an output data destination for the HSP50016-EV. The input data is loaded on to the input bus prior to the software generated clock and the output data is read from the output bus following the software generated clock.

If file based input is selected, the Control Panel software down loads data from the specified file to registers on the HSP50016-EV and clocks the data into the DATA0-15 inputs of the DDC. The Loop Count allows the user to simulate long data streams by repeatedly sending the same input file.

If file based output is specified, the software reads the data on the I and Q outputs of the HSP50016 and stores the data in the specified file. The software automatically reads the

output data and writes it into the output file as two's complement complex or real data. The configuration of the I, Q, IQCLK and IQSTB pins is transparent to the user, provided that none of the pins are three-stated and the DDC Control Word fields Real Output, HDF Decimation Rate, Number of Output Bits, I followed by Q and IQCLK rate are compatible with each other. All valid output modes are supported.

File based I/O is activated by using the space bar to toggle the "check mark" symbol in the window proceeding the input and output file identifiers in the control panel's file I/O Section. If either file input or output is activated, the respective file name must be entered in the window to the right of the file identifier. File input or output may be disabled at any time by toggling the respective "check mark".

Note: File I/O is only valid when either the 'Manual CLK' or 'Port CLK' clocking modes are selected and it is disabled if other clocking modes are specified.

Input and output data files are ASCII files whose format is described in Appendix A. There is no limitation to the input and output file size. Care must be taken if file output is specified since data is collected in the file until file output is deactivated or the DDCCTRL Program is exited.

TAP I/O files are similar, except that the TAP is available regardless of the CLK setting. The format for the TAP input and output files is given in Appendix B.

HSP50016 Data Inputs

The data window to the left of the HSP50016 icon is used to specify hexadecimal values which drive the DDC's data inputs DATA0-15. Data is entered into this window in hexadecimal format starting with the most significant digit. The contents of a particular data window may be edited by following the window editing instructions in Appendix C.

If file input is selected, the data input is driven with data from the specified file. On each clock the data window is updated with the data sample down loaded from the file. In this mode the data input window may not be manually updated.

HSP50016 Data I&Q Outputs

There are 32 bits available at P2. The control software for the evaluation board performs a serial read via the PC Port.

Control Signals

The control signal portion of the control panel is used to define the state of the DDC control signals $\overline{\text{RESET}}$ and $\overline{\text{IQSTRT}}$. The logical state of a control signal is set by using the space bar to toggle the signal state in the window preceding the specified control signal. When the evaluation board is in Port CLK mode and $\overline{\text{RESET}}$ is set either low or high, the DDC is automatically clocked five times. See the HSP50016 Data Sheet for a complete description of the control signals. **$\overline{\text{RESET}}$ must be toggled low and high once after power up. The software DOES NOT do this automatically.**

Control Words

In the lower left hand corner of the control panel is a data window which contains the hexadecimal values loaded into the HSP50016's eight control words. The contents of a particular control word may be updated by moving the cursor to the data window which is to be modified, selecting the control word by pressing the space bar (which moves the check mark to the desired control word) and depressing the F4 key. A submenu pops up which parses that control word into its various fields so that they may be examined or modified individually.

The value entered into the data window is down loaded to the HSP50016 and the submenu disappears when the user depresses the F2 key. Leaving the window via the <Esc> key ignores any changes made and returns to the main control panel screen. If the update bit has been set, the new values will update the configuration of the DDC and this will be reflected in the submenu screen.

Note that all values displayed in this window are the last values written to the control words, as opposed to having been read from the DDC itself.

Help

Help windows are provided as a source of information for control panel usage. The help window is activated by the F1 function key, and contains information based on the window which is currently active.

Command Line Interface

As an alternative to the control panel, a command line interface is provided which allows the user to control the HSP50016-EV by issuing commands from the DOS prompt. The commands perform basic I/O and configuration functions by up or down loading data to the HSP50016 through the HSP50016-EV. The Command Line Program has the following usage:

DDCCMD [Command] [ARG 1] [ARG 2] [ARG 3]

The Command specifies the action to be taken, and the Arguments (ARG1, ARG2) represent additional data required by the command. For example, to load Control Word 1 with a value of 200000005(HEX) and set the update bit, the user would type:

DDCCMD WCW 1 1 200000005 <Enter>

A summary of the command set is given in Table 2.

When several commands are to be entered consecutively, the user may initiate the interactive command mode by entering:

DDCCMD <Enter>

All commands are then entered as before, except that control does not return to DOS between commands, and it is not necessary to enter DDCCMD for each command. Note

that the software automatically updates the control words from the EVAL.CFG file upon entering the interactive mode. Leaving the interactive mode is accomplished by typing “quit” or “exit.”

DDCCMD gives the user the ability to control the evaluation board via DOS batch files or system calls from a programming language. The DDC_CHK6.BAT file discussed in the System Test Section is an example of how the Command Line Program might be used in a DOS batch file.

Configuration Jumpers

The Configuration Jumpers consists of the jumper headers JP1-3 and JP5-20 as shown in Figure 1 and Table 1. Refer to the evaluation board schematic found in the Appendices. Most of these are self-explanatory, but the following bear further discussion.

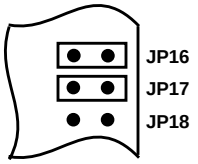


FIGURE 2. JUMPER CONFIGURATION IF CLOCK IS SUPPLIED THROUGH P1 INPUT HEADER

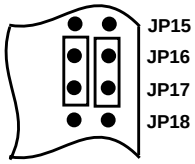


FIGURE 3. JUMPER CONFIGURATION IF CLOCK IS SUPPLIED THROUGH P2 OUTPUT HEADER

The jumpers JP16 and JP17 are used to select whether the HSP50016's clock source is provided through the P1 connector or the P2 connector. If jumpers are inserted as shown in Figure 2, a clock signal supplied through the CLK_IN pin of the P1 input header drives a buffer whose output clocks the HSP50016. The jumper inserted on JP16 feeds the buffered clock signal to the CLK_OUT pin of the P2 connector. If jumpers are inserted as shown in Figure 3, the CLK_OUT pin of the P2 connector drives the clock buffer which in turn drives the clock input of the HSP50016. The jumper inserted between JP16 pin 2 and JP17 pin 2 allows the CLKIN pin to be driven by the buffer output. NOTE: The jumper placement shown in Figure 2 is the standard configuration.

It is possible to configure the DDC so that the I, Q, IQCLK and IQSTB outputs are in a high impedance state. Except for IQSTB, these pins are pulled up on the evaluation board so that they will not float under these conditions. Since IQSTB can be either active high or low, it must be capable of being pulled either way. JP19 determines whether IQSTB is pulled up or down when it is three-stated. This jumper should be installed such that IQSTB is pulled to its inactive state.

Note: The position of JP20 comes into play only when parallel output from P2 is desired.

The jumper should be placed between pins 1 and 2 when the DDC is configured for I followed by Q mode; the jumper should be from JP20-2 to JP20-3 when I and Q are output separately. The HSP50016-EV is shipped from the factory with the default jumper configuration shown in Figure 1 and Table 1. For the supplied software to properly control operation of the HSP50016, it is assumed that the jumpers are as specified in the default configuration; of course, once the user is familiar with the operation of the board, this configuration may be modified as required. The system test software, DDCCHK, must be run using the default configuration.

TABLE 1. DESCRIPTION OF JUMPER CONNECTIONS

JP	DESCRIPTION		DEFAULT
1	DDC CLK driven from external source when this jumper is installed.	Only one of JP1, JP2 and JP3 selected at a time.	-
2	DDC CLK driven from on board oscillator when this jumper is installed.		-
3	DDC CLK driven from PC software when this jumper is installed.		Installed
5	DDC DATA0-15 driven from PC software when installed, otherwise data is from external source. **Must be installed or DATA0-15 lines must be driven to avoid damage to DDC.**		Installed
6-13	Selects evaluation board address. Only one of these jumpers should be installed at a time.		JP6 Installed
14	Selects input clock as inverted. Installed = non-inverted.		Installed
15	Selects output clock as inverted. Installed = non-inverted.		Installed
16	Direct flow of input and output clocks. JP16-1 is shorted to JP16-2 and JP17-1 is shorted to JP17-2 for the DDC CLK to be driven by the PC, on board oscillator, or connector pin P1C-20. To drive CLK from P2C-20, jumper JP16-1 to JP17-1 and JP16-2 to JP17-2. JP1 must be installed in this configuration.		JP16-1 to JP16-2, JP17-1 to JP17-2
17			
18	TAP inputs driven by PC (installed) or from P2 (not installed).		Installed
19	IQSTB pulled up (JP19-1 shorted to JP19-2) or pulled down (JP19-2 to JP19-3). **Must be installed (in either position) to avoid damage to evaluation board.**		JP19-1 to JP19-2
20	Serial to parallel converters configured for up to 32-bit, I followed by Q (JP20-1 to JP20-2) or 16 bit, I and Q output separately (JP20-2 to JP20-3).		JP20-2 to JP20-3

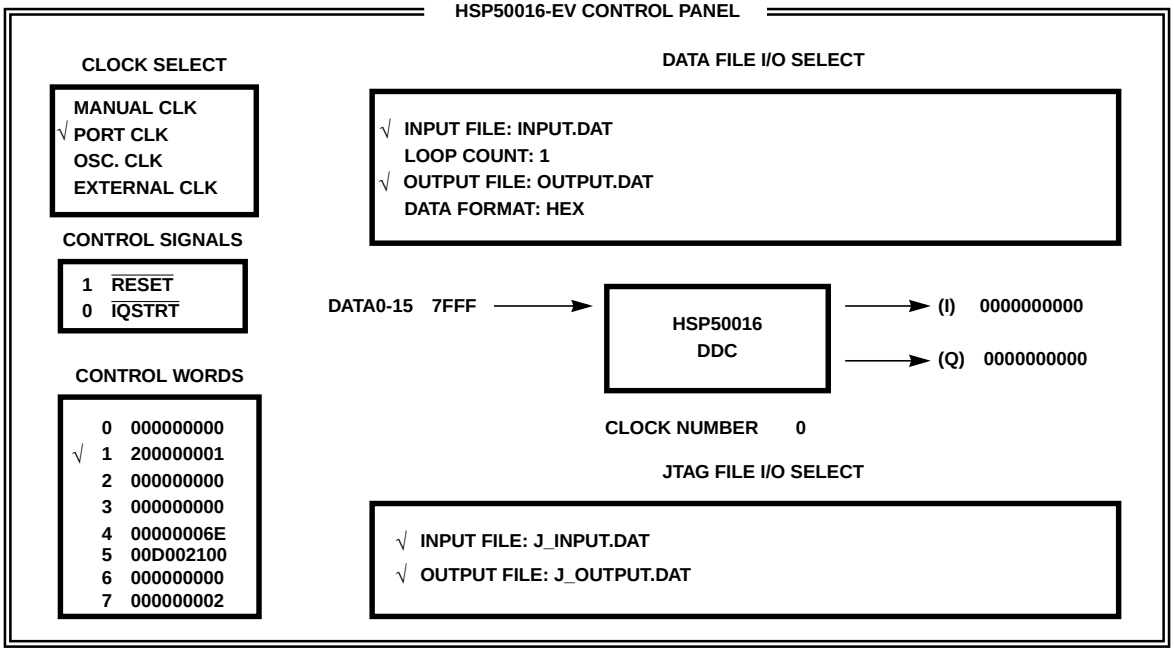


FIGURE 4. CONTROL PANEL SCREEN AS DISPLAYED ON PC

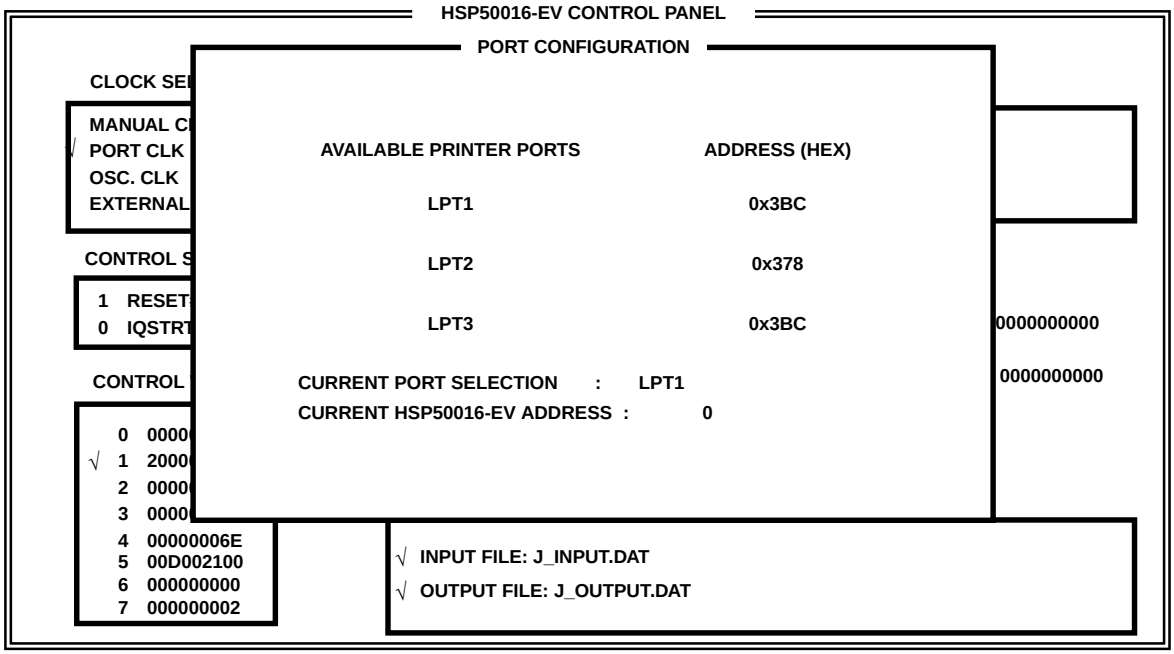


FIGURE 5. PORT CONFIGURATION WINDOW AS DISPLAYED ON PC

TABLE 2. COMMAND LIST FOR COMMAND LINE INTERFACE SOFTWARE

COMMAND	ARGUMENT #1	ARGUMENT #2	ARGUMENT #3	COMMAND DESCRIPTION
WCW	WORD NUMBER	UPDATE BIT	CONTROL WORD	Loads the specified control word of the HSP50016 with the 36-bit hexadecimal value specified in Argument #3. Setting the update bit = 1 updates the configuration of the DDC; update bit = 0 only modifies the control word.
RCW	WORD NUMBER			Reads one of the HSP50016's control words to the screen. If Argument #1 is omitted, all control words are displayed.
WCS	CONTROL REGISTER CONTENTS			Loads the evaluation board's control register with a 16-bit hexadecimal value.
RCS				Displays the last value loaded into the evaluation board's control register. Does not read the current contents of the register.
DIN	INPUT DATA			Loads the HSP50016's DATA0-15 input with the 16-bit value specified in Argument #1.
CLK	COUNT			Toggles PCCLK, the software clock to the DDC, the specified number of times. If Argument #1 is omitted, COUNT = 1.
RES				Resets the DDC and cycles CLK five times.
IQS	0/1			Sets the state of the $\overline{\text{IQSTRT}}$ line.
RDO				Reads the output I and Q data of the DDC to the screen.
PDF	INPUT FILE NAME	OUTPUT FILE NAME	COUNT	Process Data File: Read one sample from input file, write it to DATA0-15, repeat until output data becomes available, then read outputs, write to output file. Repeat until all samples in the data input file have been read. Perform this entire process for the number of times specified by Argument #3. If Argument #3 is omitted, input file is read one time.
ODF	0/1			Output data file format: 0 = hexadecimal, 1 = floating point.
TCK				Toggle TCLK one cycle.
TRS				Write $\overline{\text{TRST}}$ low, then high.
TMS	0/1			Write one bit to TMS pin.
TDI	0/1			Write one bit to TDI pin.
TDO				Read one bit from TDO pin.
PTF	INPUT FILE NAME	OUTPUT FILE NAME		Process Test File: Write bit patterns specified in input file to TAP; read TAP output and store in output file. See Appendix B for TAP file format.
$\overline{\text{PP}}$	PORT NUMBER (1 - 3)	BOARD ADDRESS (0 - 7)		Change the printer port and HSP50016-EV board address that the DDCCMD program is using for communication between the PC and the evaluation board to those specified in arguments 1 and 2. The board address is set by inserting a jumper one of the headers JP6-13.
PPC		S		Display the printer port and HSP50016-EV board address that the DDCCMD Program is using for communication to the PC.
ERR				Display the state of the error bit: 0 =...No error. 1 =...Software unable to execute command; e.g., a syntax error was detected in the command line, an RDO command was executed while DDC was executing a data output cycle, and so on. A correctly executed command clears the bit, except for ERR, BYE, EXIT and QUIT, which have no effect on the error bit.
?				List available commands together with a brief description.
BYE, EXIT, QUIT				Any one of these terminates interactive mode.

Hardware Overview

The HSP50016-EV was designed to facilitate prototyping with the HSP50016 Digital Down Converter. It can be used in a stand alone mode, in conjunction with other Intersil evaluation boards, or be inserted into a card cage and operate as a part of a larger system. The following description of the board references both the Block Diagram in Figure 6 and the Schematic Diagrams, which are included at the back of this manual.

Bus Structure

The HSP50016-EV utilizes a set of busses for DDC input, output and control as shown in Figure 6. The input and output busses connect the DDC to the outside world through 96 Pin DIN connectors conforming to the VME J2/P2 Connector Standard. DDC control information is provided either by control registers down loaded via the parallel port of a PC or from the 96 Pin DIN connectors

The DDC's input data bus, DIN0-15, is driven from the 96 Pin DIN connector P1 (Pinout shown in Table 3). DIN0-15 may be driven by Registers U12 and U13 which have been down loaded with data through the Parallel Port Bus. The source of the input data is selected by jumper JP5. Installing the shorting jumper on JP5 selects the PC as the data source. Removing the jumper puts the registers driving the DIN0-15 bus in a high impedance state so that the input data can be driven from P1.

The control lines of the DDC and the board are driven by the outputs of the Control Registers (U11, U16). These registers are down loaded with data via the Parallel Port Bus or through the PCD0-7 lines on P1 or P2. when the board is controlled through the 96 Pin DIN connectors, the user must emulate the operation of the PC interface. A description of this operation is given below in the section describing the Parallel Port Bus.

The DDC output is available through three different paths: It is connected to the Select line of the PC Parallel Port through the eight to one multiplexer U6; it is connected to the 96 Pin DIN connector P2 through the buffer U1; finally, it is converted to parallel data by the Shift Registers U2-5 and driven out on P2. The mapping for P2 is given in Table 4.

Parallel Port Bus

The Parallel Port Bus carries the write only parallel data and signals required to support bidirectional data transfers between the HSP50016-EV and the parallel port of the PC. This bus contains eight data lines, PCD0-7, two control lines, PCWR0-1, and the serial output line PCRD1. The control and data lines are used to down load data into the on board registers of the HSP50016-EV. The serial output line carries the DDC output data back to the PC.

The Parallel Port Bus is attached to the PC by connecting the ribbon cable provided to the PC's parallel port and to the 26 pin connector J1 on the DDC Evaluation Board. The ribbon cable maps the Parallel Port Bus signals to the PC's parallel port as shown in Table 5.

The Parallel Port Bus is brought out through each of the 96 Pin DIN connectors (P1, P2) so that multiple Intersil evaluation boards can be daisy chained. This allows all of the evaluation boards in the chain to be controlled through a single board which has been connected to a host PC.

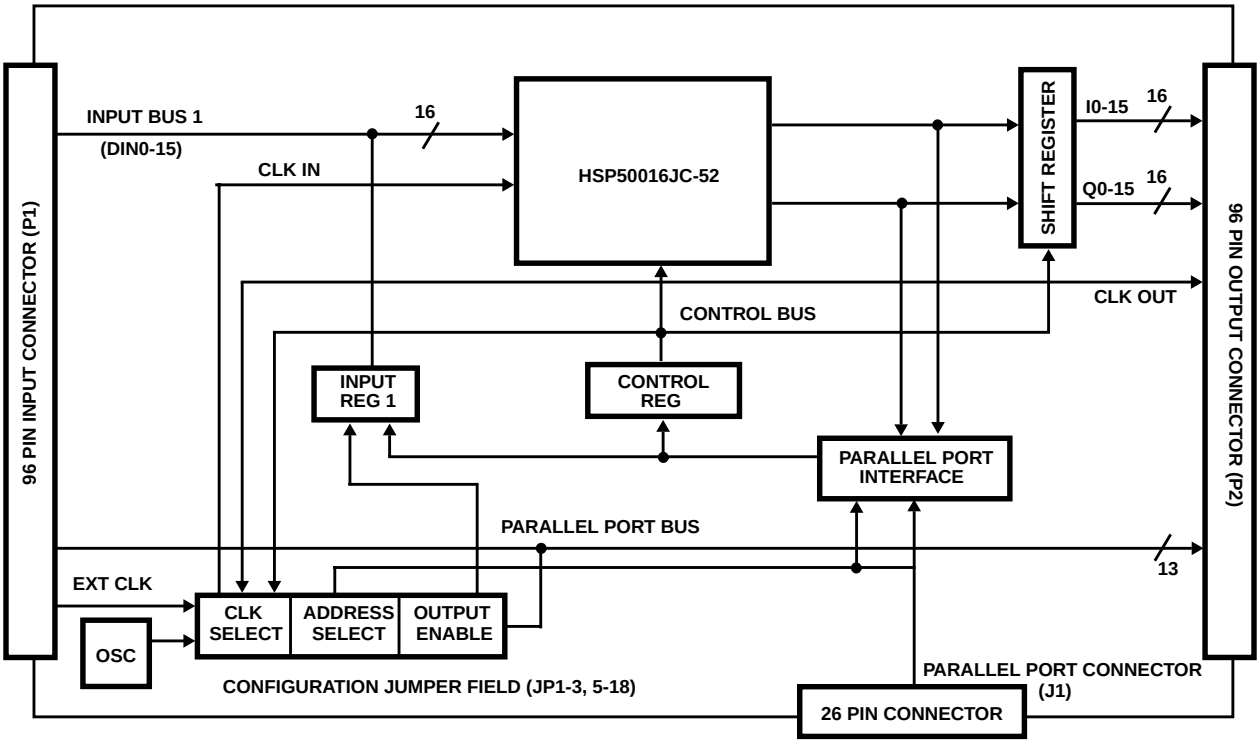


FIGURE 6. BLOCK DIAGRAM OF HSP50016-EV

TABLE 3. PIN ASSIGNMENTS FOR 96 PIN INPUT CONNECTOR P1

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	N.C.	V_{CC}	GND
2	DIN0	GND	DIN1
3	DIN2	N.C.	DIN3
4	DIN4	N.C.	DIN5
5	DIN6	N.C.	DIN7
6	GND	N.C.	DIN8
7	DIN9	N.C.	DIN10
8	DIN11	N.C.	DIN12
9	DIN13	N.C.	DIN14
10	DIN15	N.C.	GND
11	N.C.	N.C.	N.C.
12	N.C.	GND	N.C.
13	N.C.	V_{CC}	N.C.
14	N.C.	N.C.	N.C.
15	N.C.	N.C.	GND
16	N.C.	N.C.	N.C.
17	N.C.	N.C.	N.C.
18	N.C.	N.C.	N.C.
19	N.C.	N.C.	N.C.
20	GND	N.C.	CLKIN
21	GND	N.C.	N.C.
22	GND	GND	N.C.
23	GND	N.C.	N.C.
24	GND	N.C.	N.C.
25	GND	N.C.	N.C.
26	PCD0	N.C.	PCD1
27	PCD2	N.C.	PCD3
28	PCD4	N.C.	PCD5
29	PCD6	N.C.	PCD7
30	PCWR0	N.C.	GND
31	PCWR1	GND	PCRD0
32	PCRD1	V_{CC}	PCRD2

TABLE 4. PIN ASSIGNMENTS FOR 96 PIN OUTPUT CONNECTOR P2

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	N.C.	V_{CC}	GND
2	QO0	GND	QO1
3	QO2	N.C.	QO3
4	QO4	N.C.	QO5
5	QO6	N.C.	QO7
6	GND	N.C.	QO8
7	QO9	N.C.	QO10
8	QO11	N.C.	QO12
9	QO13	N.C.	QO14
10	QO15	N.C.	GND
11	N.C.	N.C.	IO0
12	IO1	GND	IO2
13	IO3	V_{CC}	IO4
14	IO5	N.C.	IO6
15	IO7	N.C.	GND
16	IO8	N.C.	IO9
17	IO10	N.C.	IO11
18	IO12	N.C.	IO13
19	IO14	N.C.	IO15
20	TCK.E	N.C.	CLKOUT
21	TMS.E	N.C.	IQSTB.B
22	TRST.E	GND	IQCLK.B
23	TDI.E	N.C.	IOUT.B
24	TDO.B	N.C.	QOUT.B
25	GND	N.C.	GND
26	PCD0	N.C.	PCD1
27	PCD2	N.C.	PCD3
28	PCD4	N.C.	PCD5
29	PCD6	N.C.	PCD7
30	PCWR0	N.C.	GND
31	PCWR1	GND	PCRD0
32	PCRD1	V_{CC}	PCRD2

TABLE 5. SIGNAL MAPPING FOR CONNECTOR J1

PIN NUMBER	J1A SIGNAL MNEMONIC	J1B SIGNAL MNEMONIC
1	N.C.	N.C.
2	PCD0 (D0)	N.C.
3	PCD1 (D1)	PCWR0 (INIT PRINTER)
4	PCD2 (D2)	PCWR1 (SELECT IN)
5	PCD3 (D3)	GND
6	PCD4 (D4)	GND
7	PCD5 (D5)	GND
8	PCD6 (D6)	GND
9	PCD7 (D7)	GND
10	N.C.	GND
11	PCRD0 (BUSY)	GND
12	PCRD2 (PAPER END)	GND
13	PCRD1 (SELECT)	GND

PCRD = PC Read; PCD = PC Data

TABLE 6. REGISTER TO INPUT/CONTROL BUS MAPPINGS

REGISTER ADDRESS	DESTINATION REGISTER	REGISTER FUNCTION
0	U16	Clock and control
1	U11	DDC Control, TAP
2	U13	DDC Data input LS Byte
3	U12	DDC Data Input MS Byte
4-7	Not Used	N.C.

TABLE 7. ADDRESS REGISTER BIT MAP

NOT USED	LOAD ADDRESS RANGE	BOARD ADDRESS	REGISTER ADDRESS
D7	D6	D5-3	D2-0

Register Structure

The HSP50016-EV provides a set of registers which may be used as a source for DDC input and control. They can be loaded from either the parallel port or from the P1 connector.

Down Loading Data via Parallel Port Interface

The control and input registers are down loaded from the PC by a series of single byte writes to the to the Parallel Port Interface. The Parallel Port Interface consists of two decoders, an 8-bit address register, and an 8-bit holding register. The On-Board Registers are down loaded by first writing data to the Parallel Port Interface's Holding Register U17 followed by two writes to the Address Register U18. By writing the address register, data in the holding register is loaded into one of the Registers U11, 12, 13, 16. The address register specifies the particular register for loading as well as the board address of the HSP50016-EV targeted for the data download. The HSP50016-EV board address is selected by placing a shorting jumper on one of the headers JP6-13 (see Configuration Jumper Field Section), and the memory map for the 8 data registers is shown in Table 6. The bit map for the Parallel Port Interface's Address Register is given in Table 7.

The Parallel Port Interface's Address and Holding Registers are loaded with data from the PCD0-7 data lines of the parallel port bus by a “low” to “high” transition on the appropriate bus control line. Specifically, the address register is loaded with data when a “low” to “high” transition occurs on the PCWR0 line of the Parallel Port Bus, and the holding register is loaded by a like transition on the PCWR1 line. The mapping of the parallel port bus signals to the PC's parallel port is given in Table 5.

As an example, consider the loading of the least significant byte of the data input, Register U13, as shown by the Timing Diagram in Figure 7. First, data is down loaded to the Parallel Port Interface's Holding Register. Next, the address register is written with a value which contains the address of U13 (see Table 6 for memory map), the HSP50016-EV board address (assumed to be zero in this example), and a “high” in the LD bit position (see Table 7 for Address Register Bit Map). Finally, data is latched into the targeted register by rewriting the address register with the same board and register address but with a “low” in the LD bit position. The “high/low” transition of the LD bit loads the data in the holding register into the target data register on the specified HSP50016-EV.

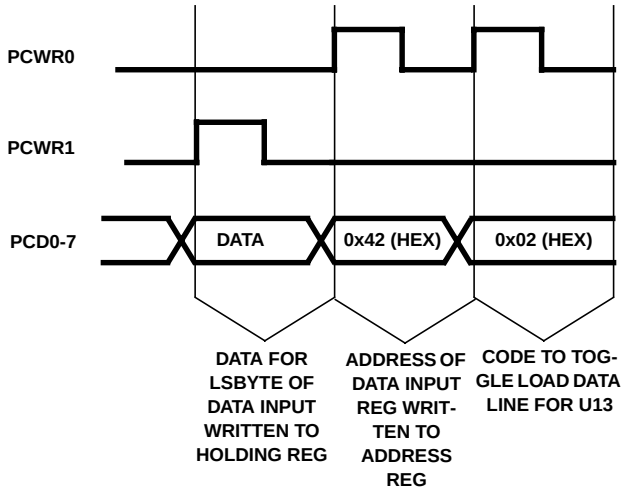


FIGURE 7. TIMING DIAGRAM FOR LOADING DATA INTO LSBYTE OF DATA INPUT REGISTER

Up Loading Data via PC's Parallel Port

Data is up loaded to the host PC through the “Select” serial status line of the PC's parallel port. The PC up loads data by monitoring the state of the PCRD1 serial output line on the HSP50016-EV's Parallel Port Bus. The mapping of the evaluation board signals to the PC’s parallel port is given in Table 5.

DDC Data and Control via P1 Connector

When it is desired to use P1 connector for data input, the registers driving the data bus are three-stated by removing the jumper JP5 (see Configuration Jumper Field Section). The DIN0-15 pins on P1 are then used to drive the input pins of the HSP50016. If all 16 pins are not used, then the DIN bus should be loaded starting from bit 15 down. **When JP5 is not installed, all data input pins must either be driven by an external data source or grounded to avoid damage to the board.**

To control the DDC from the P1 or P2 connector, the PCD0-7 bus is exercised via the connector. In this case, the user must operate this bus in the same manner as the PC exercises it from the parallel port as described above. No jumper selection is necessary in this case; it is only necessary to leave the parallel port connector J1 unconnected.

To operate the Test Access Port from P2, the shorting jumper on JP18 is removed. The TAP pins are then controlled directly from P2 according to the TAP Specification. In this case, the SEL0-2 lines should be set to 0, 0, and 1 respectively.

DDC Clocking Modes

The HSP50016-EV provides the DDC with one of three jumper selectable clock sources. The three clock choices consist of an on-board oscillator, a user provided external clock, and a clock generated by toggling the LSB of the Control Register U16. The clock source is select by placing a jumper on either JP1, 2 or 3. To support applications in which multiple evaluation boards are daisy chained together, a clock output line is routed to the HSP50016-EV's output connector P2.

An external clock may be selected by inserting a jumper on the header JP1. In this mode, an external clock supplied to the CLKIN pin of the 96 pin Input Connector is provided to the DDC. This configuration supports the use of a common clock between daisy-chained evaluation boards by wiring CLKOUT from the P2 Output Connector of one board to the CLKIN pin of another board's P1 Input Connector. Since there is no synchronization between the externally provided clock and data transfers to the HSP50016-EV's I/O Registers, the PC would typically provide the DDC with asynchronous control in this mode.

The on-board oscillator is selected as a clock source by JP2. In this mode, the oscillator on board the HSP50016-EV is supplied as a clock to the DDC. Since data transfers to the DDC via the HSP50016-EV’s I/O Registers are much slower than the DDC’s data rate using the oscillator clock, the PC can only be used to provide the DDC with asynchronous control in this mode.

The LSB of the Control Register U16 is selected as the clock source if a jumper is inserted in the header JP3. In this mode, the clock signal is generated by using register writes to toggle the PCCLK bit. Since the clock may be controlled by software, input and control register writes and the output shift register reads can be performed synchronously with the clock. Consequently, the HSP50016-EV can be used as a hardware modeler where input and output data vectors are transferred via the PC's parallel port.

Configuration Jumper Field

The HSP50016-EV is configured for operation by placing jumpers in the headers JP1-3 and JP5-18. As shown in Table 1, the jumper field has areas dedicated for clock selection, register output enables and board address selection. The default jumper placement is shown in Figure 1 and Table 1. Each HSP50016-EV leaves the factory jumpered with the default configuration.

The Clock Select jumpers are used to specify one of the three available DDC clocking modes. These include EXT_CLK for selection of an external clock source, OSC_CLK for selection of the on board oscillator clock, and PC_CLK for selection of a register driven clock using the LSB of the CTL Control Register. The clocking modes are described in the DDC Clocking Modes Section of this manual. Note: Normally, only one clock source may be selected at a time. In any mode, the input and output clocks may be negated independently by removing the jumpers on JP14 and JP15.

The output of the Input Registers U12 and U13 are enabled by placing a jumper on JP5 (see Bus and Register Structure Sections) If a jumper is removed, the output of the respective register is three stated.

The Board Address Jumpers are used to specify the HSP50016-EV board address used for data transfers via the Parallel Port Bus. An address from 0 to 7 may be selected by inserting a jumper in positions ADDR0 thru ADDR7 respectively. Only one jumper may be inserted in this field.

The jumper JP18 is used to select the source of data for the IEEE 1149.1 Test Access Port (TAP) bus. Inserting this jumper enables the PC to drive this bus, while removing it enables control from the P1 connector.

JP19 selects whether the IQSTB line is pulled up or down. Placing the jumper between header pins 1 and 2 pulls IQSTB up, while shorting pins 2 and 3 pulls IQSTB down. The position of the jumper is only meaningful when IQSTB is

three stated, which can be programmed by setting the proper control bits of the DDC. Even if the user has no intention of operating in this mode, it is recommended that JP19 be put in one position or the other to avoid the possibility of this line floating after power up or due to being inadvertently placed in the high impedance state. **If the shorting jumper is not installed on JP19, the IQSTB line may oscillate and cause damage to U6.**

When parallel output is desired from the P2 connector, JP20 controls the flow of data to the Shift Registers U4 and U5. The user may read the I and Q outputs separately with 16 bits of precision by configuring the DDC to output data separately over the I and Q pins, setting the output precision to 16 bits and inserting a shorting jumper on header pins 2 and 3. The parallel outputs can be read with any precision by setting the DDC for I followed by Q and setting the jumper on header pins 1 and 2. For this circuit to operate correctly, the DDC must also be set for IQCLK Rate > 1, and data stable on the falling edge of IQCLK. Note that in the schematic, the parallel output lines are numbered assuming that the DDC output is MSB first, although the circuit will work just as well in LSB first mode.

HSP50016-EV Limited Warranty

Intersil warrants the HSP50016-EV to be free of defects in material and workmanship under normal use for a period of ninety (90) days. Intersil also warrants that the HSP50016-EV User's Manual is substantially complete and contains all the information which Intersil considers necessary to use the HSP50016-EV, and that the HSP50016-EV functions substantially as described in the HSP50016-EV User's Manual. Intersil will replace the HSP50016-EV as Intersil's sole duty under this warranty only if you ship it, postage prepaid, to Intersil within 90 days of such acquisition and provide proof of date of acquisition.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse, or as a result of service or modification by anyone other than Intersil or Intersil's authorized representatives.

Intersil makes no other express or implied warranty with respect to the HSP50016-EV other than the limited warranty set forth above. Intersil disclaims all implied warranties of merchantability and/or fitness for a particular purpose. In any event, all implied warranties shall be limited to the duration of this warranty. **The liability of Intersil, if any, shall under any tort, contract or other legal theory be limited to the actual price paid for such product and shall in no event include incidental, consequential, special or indirect damages of any kind, even if Intersil is aware of the possibility of such damages.**

Intersil reserves the right to revise and make changes to this manual and the HSP50016-EV from time to time without obligation to notify any person of, or to provide any person with, such revisions or changes.

HSP50016-EV Software License Agreement

In return for the purchase price of the HSP50016-EV product, the Purchaser receives from Intersil Corporation (“Intersil”) a non-exclusive nontransferable (except as set forth below) license under Intersil copyrights to use the software subject to the following terms and conditions:

[1] The Software is protected by both United States Copyright Law and International Treaty Provisions. Therefore, you must treat the Software like any other copyrighted material (e.g., a book) and may not copy, distribute or make derivatives of any part thereof except that the you may either a) make one copy of the Software solely for archival purposes, or b) transfer the Software to a single hard disk provided you keep the original solely for backup or archival purposes.

[2] The Software may be transferred to a third party on a permanent basis, provided you retain no copies and the recipient agrees, in writing to Intersil, to the terms of this Agreement.

[3] If the software package contains both 3.5" and 5.25" disks, then you may use only the disks appropriate for your single-user computer. You may not use the other disks on another computer or loan, rent, lease, or transfer them to another user except as part of the permanent transfer (as provided above) of all Software.

Appendix A

Data File Structures

The Input/Output data files used by the HSP50016-EV Control Panel and Command Line Interface Software contain data samples. The data files consist of a seven line header followed by the data itself. The Header Section must follow this format:

Line 1:	Comment #1
Line 2:	Comment #2
Line 3:	Comment #3
Line 4:	Comment #4
Line 5:	Comment #6
Line 7:	r 1 n
(Data sample)	•
	•
	•

The ‘n’ on the 7th line of the header should be replaced by the number of data samples in the file. Following the header, the data samples are listed one per row. The data sample is represented as a two’s complement floating point value bounded by +1.0 and -1.0.

The output file format is similar, except that the data samples are usually complex, with the real part in the first column and the imaginary part in the second column. In this case, the “r” int line 7 of the file header is replaced with a “c”. The exception to this is when the DDC is in real output mode, in which case the output file consists of one column of real data as shown above. The file CMPRFILE.DAT installed in the DDC_CHK subdirectory is an example of the output data file structure.

Appendix B: TAP File Format

The input test vector file is read line by line; each set of inputs is supplied to the part simultaneously. On the falling edges of TCK, the output pins are read and their states are stored in the output file. Input and output files are ASCII text. The input file has no header or trailer, but for purposes of clarity, it is recommended that the user include a header such as the one shown in the example below. The first column of bits is applied to the TDI pin, the next to TRST, and so on as shown.

Input file example:

Comment lines denoted by # in column 1

```
# T   T   T   T
# D   R   M   C
# I   S   S   K
#     T
    1   1   1   0
    1   0   1   1
    1   0   1   0
    1   1   1   1
    1   1   1   0
```

The output file is similar in format, with each column corresponding to an output pin and each row representing the state of the pins on each falling edge of TCK.

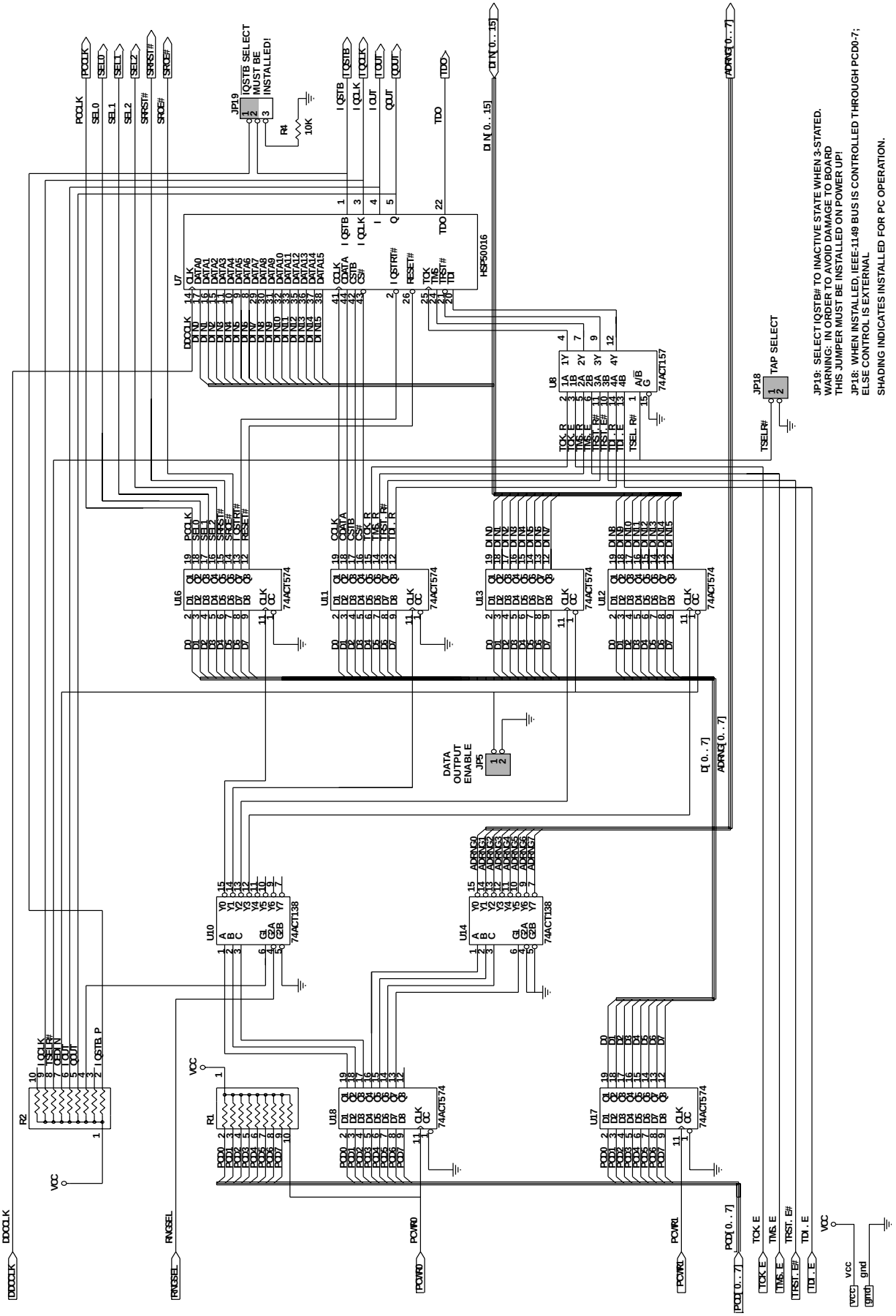
Output file example:

```
                I   I
                Q   Q
T               S   C
D               T   L
O   I   Q   B   K
1   1   1   0   0
1   0   1   1   0
1   0   1   0   0
```

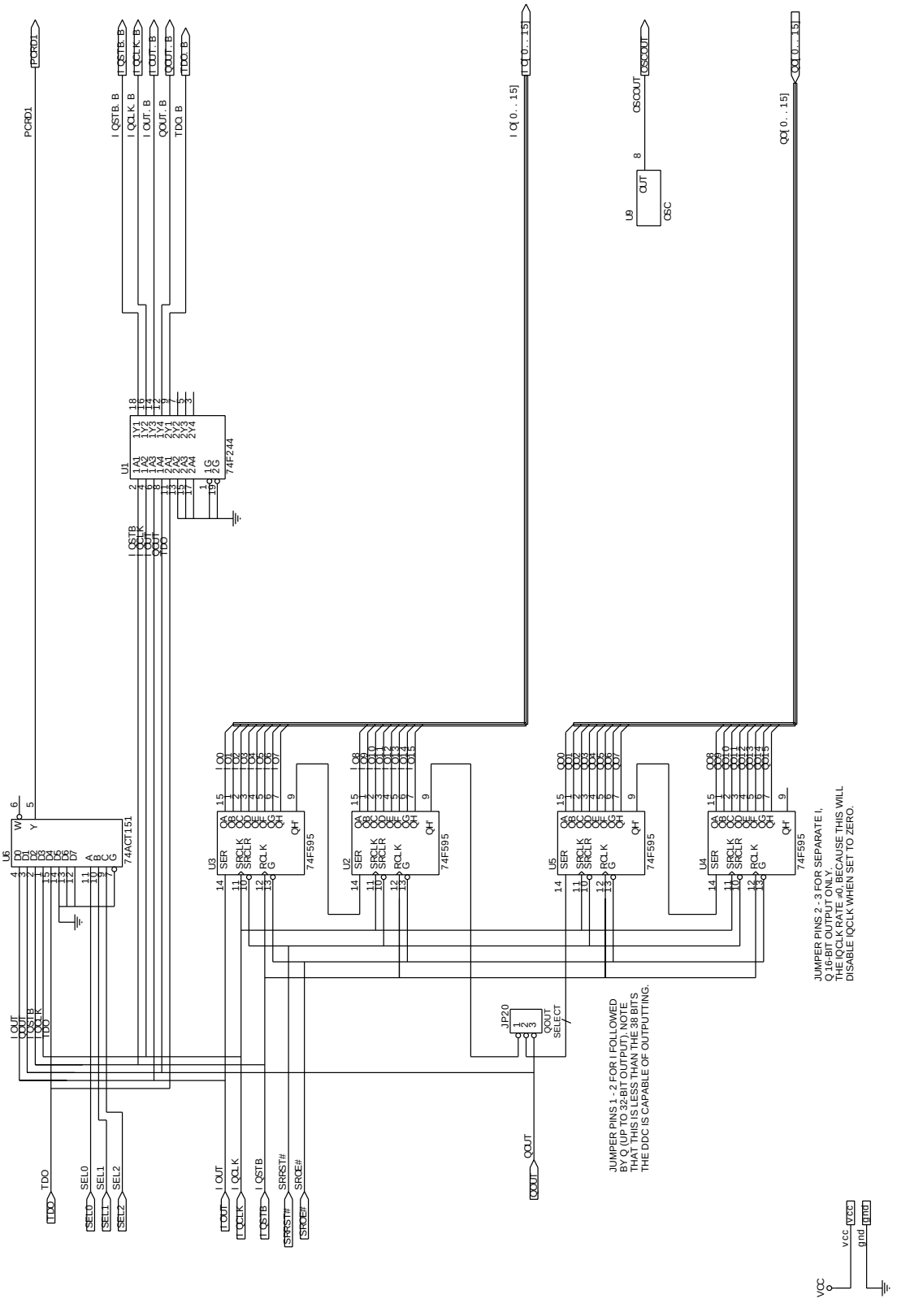
Appendix C: Window Editing

KEY	FUNCTION
Control-Y	Deletes contents of field.
Insert	Toggles insert/overwrite editing modes.
Any Character	Inserts or replaces character at current cursor location.
Delete	Deletes character at current cursor location.
Backspace	Deletes character to the left of the cursor.
Right/Left Arrow	Moves cursor right or left.
Home	Positions cursor at the beginning of the current line.
End	Positions cursor at the end of the current line.
Enter/Up/Down Arrow Keys	Enter edited data and exit window. DDCCTRL does not accept changes until window is exited.
Space Bar	Toggles control signals

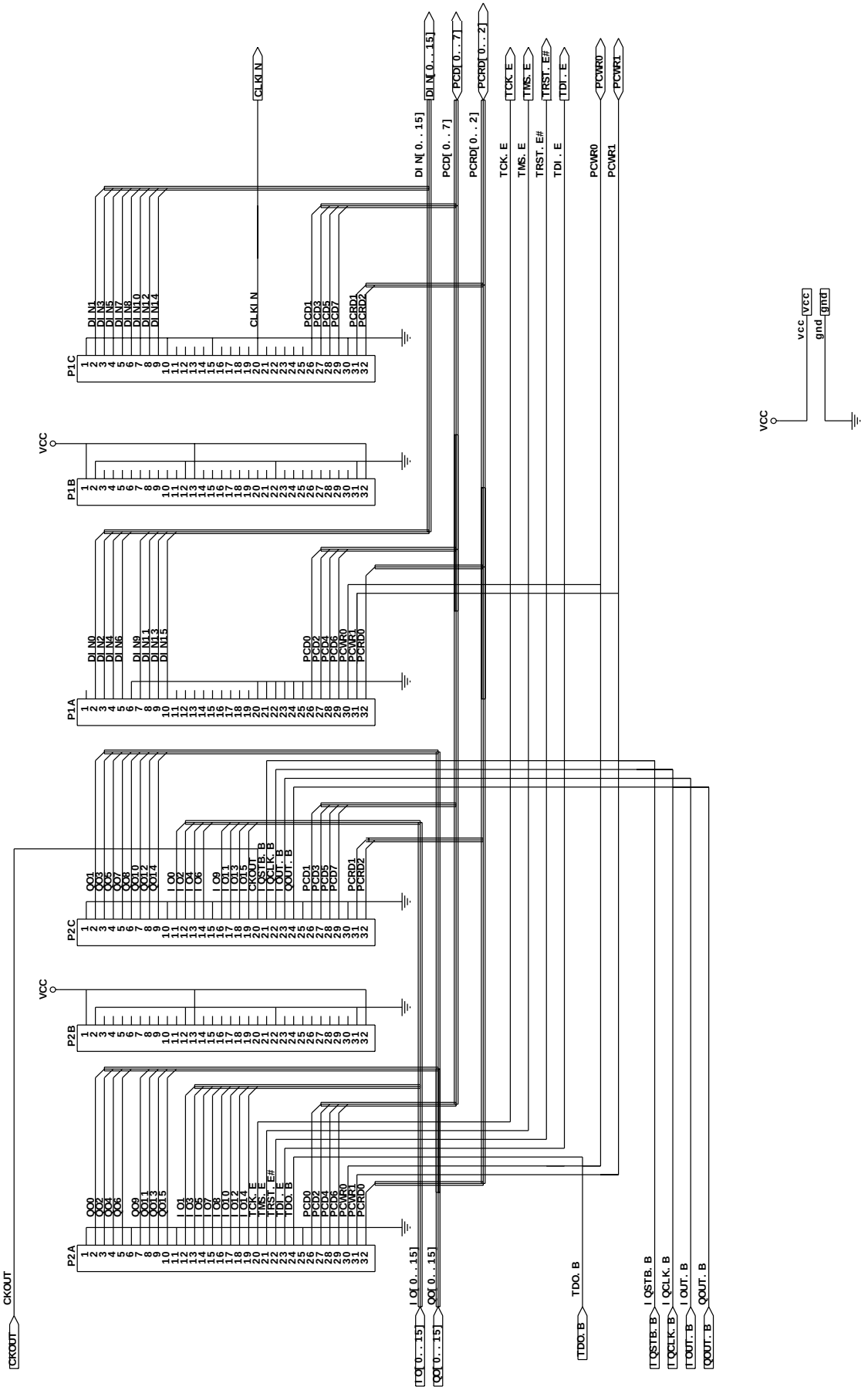
Schematic


JP19: SELECT IQSTB# TO INACTIVE STATE WHEN 3-STATED.
WARNING: IN ORDER TO AVOID DAMAGE TO BOARD
THIS JUMPER MUST BE INSTALLED ON POWER UP!
JP18: WHEN INSTALLED, IEEE-1149 BUS IS CONTROLLED THROUGH PCD0-7;
ELSE CONTROL IS EXTERNAL
SHADING INDICATES INSTALLED FOR PC OPERATION.
HSP50016
74ACT574
74ACT138
74ACT157
DATA OUTPUT ENABLE
TAP SELECT
IQSTB SELECT MUST BE INSTALLED!

Schematic (Continued)



Schematic (Continued)



Schematic (Continued)