HIP7038A8

PRELIMINARY

April 1994

J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version

Features

- **Direct Replacement for HIP7030A2/A8 Microcontrollers**
  - **All Hardware and Software Features**
  - **Equivalent Timing and Performance**
- **Memory**
  - **176 Bytes of RAM**
  - **7744 Bytes of Programmable EEPROM**
  - **242 Bytes of Bootstrap Program**
- **Single 5V Supply**
- **10MHz Operating Frequency (5.0MHz Internal Bus Frequency) at 5V.**
- **28 Lead Small Outline Ceramic Package**
  - **Same Terminal Assignment as HIP7030A2 and HIP7030A8**

Description

The HIP7038A8 HCMOS Microcomputer is an EEPROM version of the HIP7030A family of low-cost single-chip J1850 microcontrollers. These microcontrollers provide the system designer with a complete set of building blocks for implementing a “Class B” VPW multiplexed communications network interface, which fully complies with SAE Recommended Practice J1850. The HIP7038A8 contains all hardware and software features of the HIP7030A2/A8 microcontrollers with equivalent timing, performance characteristics, and an identical footprint.

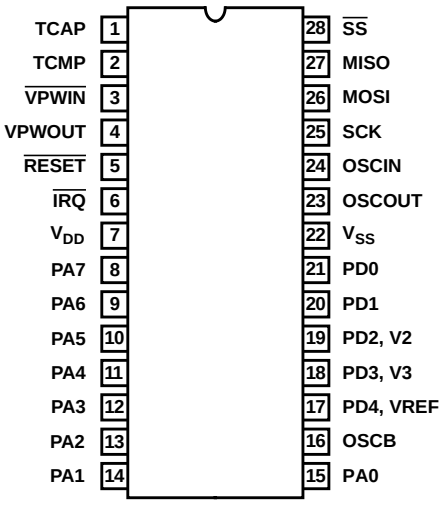
The device can be programmed using the HIP7038A8 EEPROM Programmer available from Intersil. In-circuit Emulation Tools are also provided for system development.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7038A8F	-40^{o}C to +85^{o}C	28 Lead Ceramic SOIC

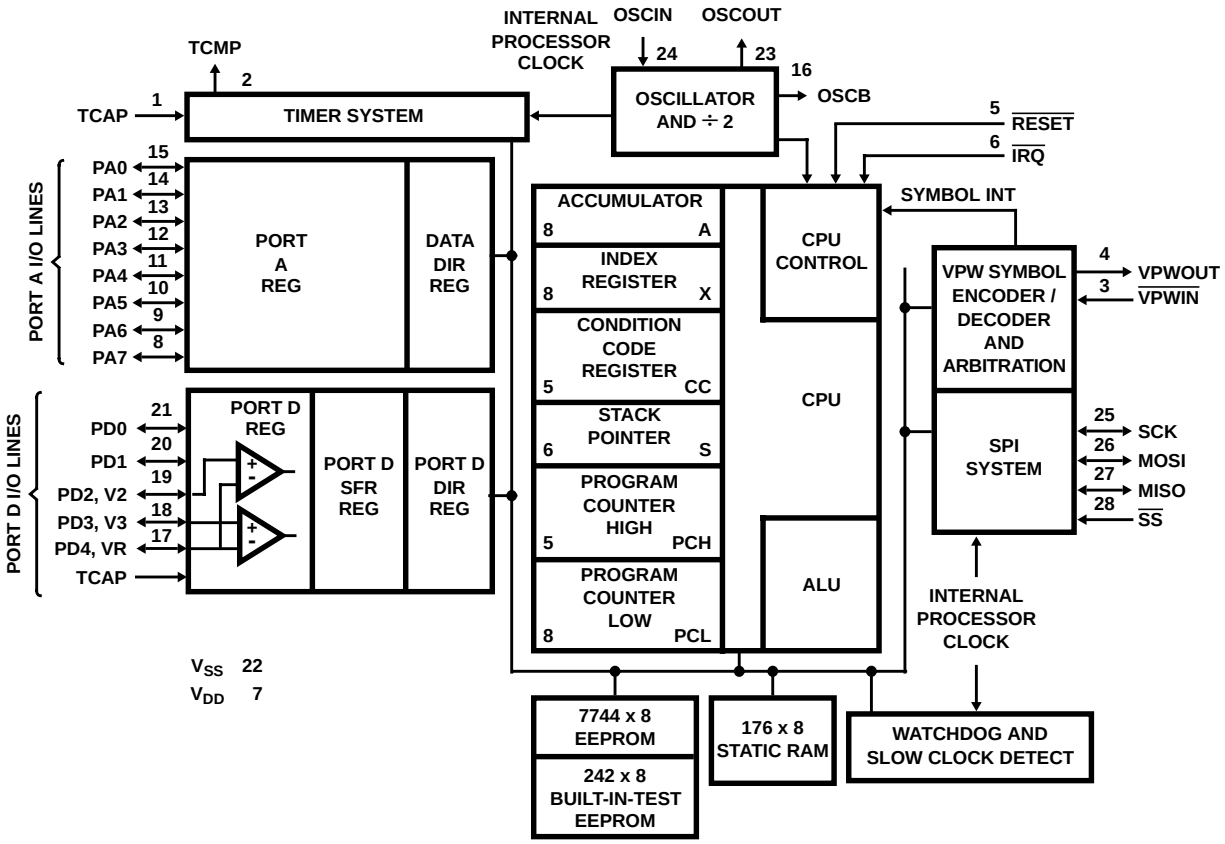
Pinout

HIP7038A8 (SOIC FLATPACK)
TOP VIEW



File Number **3647.1**

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.3V to +6.0V
Input or Output Voltage
  Pins with V_{DD} Diode . . . . . -0.3V to V_{DD} +0.3V
  Pins without V_{DD} Diode. . . . . -0.3V to +10.0V
Current Drain Per Pin, I (Excluding V_{DD} and V_{SS}) 25mA
ESD Classification . . . . . Class 2
Gate Count . . . . . 21000 Gates

Thermal Information

Operating Temperature Range (T_A) . . . . . -40^oC to $+125^oC$
Storage Temperature Range (T_{STG}) . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
  1/16in. ± 1/32in. (1.59 ± 0.79mm) from case for 10s Max.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -40^oC to $+85^oC$
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . $(0.8 \bullet V_{DD})$ to V_{DD}
Input Rise and Fall Time
  CMOS Inputs . . . . . 100ns Max.
  CMOS Schmitt Inputs . . . . . Unlimited

DC Electrical Specifications

$V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40^oC$ to $+85^oC$ Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
RUN	I_{RUN}		-	50	-	mA
WAIT	I_{WAIT}		-	4	-	mA
STOP	I_{STOP}	$T_A = +25^oC$	-	100	-	µA
		$T_A = -40^oC$ to $+85^oC$	-	100	-	µA
Powerdown Input Voltage: $\overline{RESET}$, $\overline{IRQ}$, $\overline{VPWIN}$, OSCIN	V_{INPD}	$V_{DD} = 0$	-0.3	-	9	V

NOTE:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Functional Description

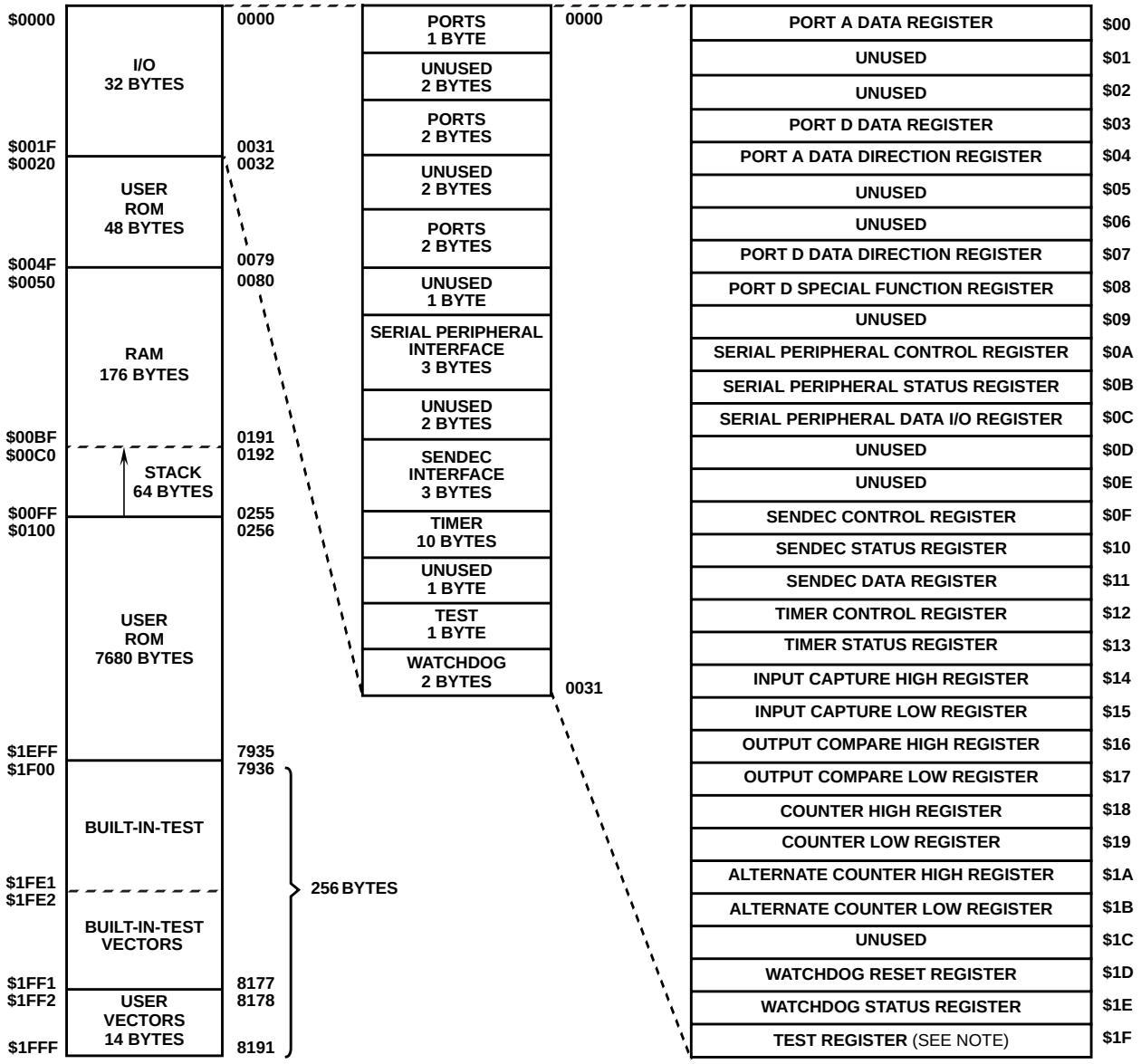
The HIP7038A8 MCU is functionally identical to the HIP7030A2 and HIP7030A8 microcontrollers. The device differs only in that the on-board masked ROM has been replaced with EEPROM, which allows the device to be rapidly programmed by the user. For detailed information about the functions included on the HIP7038A8 refer to File Number 3646, the technical specification of the HIP7030A2 Microcontroller. Only differences are presented here.

The availability of the HIP7038A8 dramatically reduces the time-to-market of new products by providing the development engineer rapid feedback during the design phase of a HIP7030A2/8 project.

The EEPROM is reusable and can be reprogrammed up to 10^4 times.

Memory Organization

The HIP7038A8 MCU addresses 8192 bytes of memory and I/O registers with its program counter. Of these locations, 8184 have been implemented as shown in Figure 1. The first 256 bytes of memory (page zero) include: 24 bytes of I/O features such as data ports, the port DDRs, Timer, serial peripheral interface (SPI), and J1850 VPW Registers; 48 bytes of user ROM, and 176 bytes of RAM. The next 7680 bytes complete the user ROM. The Built-In-Test ROM (242 bytes) is contained in memory locations $1F00 through $1FF1. The 14 highest address bytes contain the user defined reset and the interrupt vectors. Eight bytes of the lowest 32 memory locations are unused and the 176 bytes of user RAM include up to 64 bytes for the stack. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.



NOTE: Accessable in test mode only.

FIGURE 1. MEMORY MAP OF THE HIP7038A8

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