HA5022/883

Dual 125MHz Video Current Feedback Amplifier with Disable

January 1995

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Dual Version of HA-5020**
- **Individual Output Enable/Disable**
- **Wide Unity Gain Bandwidth 125MHz**
- **Slew Rate 475V/μs**
- **Differential Gain 0.03%**
- **Differential Phase. . . . . 0.03 Deg.**
- **Supply Current (per Amplifier) 7.5mA**
- **Crosstalk Rejection at 10MHz. . . . . -60dB**
- **ESD Protection. 2000V**
- **Guaranteed Specifications at ±5V Supplies**

Applications

- **Video Multiplexers; Video Switching and Routing**
- **Video Gain Block**
- **Video Distribution Amplifier/RGB Amplifier**
- **Flash A/D Driver**
- **Current to Voltage Converter**
- **Radar and Imaging Systems**
- **Medical Imaging**

Description

The HA5022/883 is a dual version of the popular Intersil HA-5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5022/883 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 video multiplexers to be implemented with a single IC.

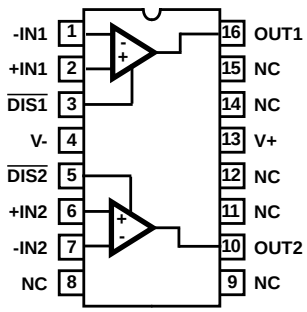
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5022MJ/883	-55°C to +125°C	16 Lead CerDIP

Pinout

HA5022/883
(CERDIP)
TOP VIEW



Spec Number **511107-883**
File Number **3729.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 36V
Differential Input Voltage 10V
Voltage at Either Input Terminal . . . . . V+ to V-
Output Current . . . . . Full Short Circuit Protected
Junction Temperature . . . . . +175^{o}C
ESD Rating . . . . . < 2000V
Storage Temperature Range . . . . . -65^{o}C ≤ T_A ≤ +150^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	75^{o}C/W	20^{o}C/W

Maximum Package Power Dissipation at +75^{o}C
CerDIP Package 1.33W
Package Power Dissipation Derating Factor above +75^{o}C
CerDIP Package . . . . . 13.3mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage ($\pm V_S$) . . . . . ±5V to ±15V
Operating Temperature Range . . . . . -55^{o}C ≤ T_A ≤ +125^{o}C

$V_{INCM} \leq 1/2(V+ - V-)$ $R_L \geq 50\Omega$
$V_{\overline{DISABLE}} = V+$ or 0V $R_F = 1k\Omega$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_{SOURCE} = 0\Omega$, $R_L = 400\Omega$, $V_{OUT} = 0V$, $V_{\overline{DISABLE}} = V+$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25^{o}C	-3	3	mV
			2, 3	+125^{o}C, -55^{o}C	-5	5	mV
Common Mode Rejection Ratio	CMRR	$\Delta V_{CM} = \pm 2.5V$ V+ = 2.5V, V- = -7.5V V+ = 7.5V, V- = -2.5V	1	+25^{o}C	53	-	dB
			2	+125^{o}C	38	-	dB
		$\Delta V_{CM} = \pm 2.25V$ V+ = 2.75V, V- = -7.25V V+ = 7.25V, V- = -2.75V	3	-55^{o}C	38	-	dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{SUP} = \pm 1.5V$ V+ = 6.5V, V- = -5V V+ = 3.5V, V- = -5V	1	+25^{o}C	60	-	dB
			2, 3	+125^{o}C, -55^{o}C	55	-	dB
Delta Input Offset Voltage Between Channels	ΔV_{IO}	$V_{CM} = 0$	1	+25^{o}C	-	3.5	mV
			2,3	+125^{o}C, -55^{o}C	-	3.5	mV
Non-Inverting Input (+IN) Current	I_{BSP}	$V_{CM} = 0V$	1	+25^{o}C	-8	8	µA
			2, 3	+125^{o}C, -55^{o}C	-20	20	µA
+IN Current Common Mode Sensitivity	CMS_{IBP}	$\Delta V_{CM} = \pm 2.5V$ V+ = 2.5V, V- = -7.5V V+ = 7.5V, V- = -2.5V	1	+25^{o}C	-	0.15	µA/V
			2	+125^{o}C	-	2.0	µA/V
		$\Delta V_{CM} = \pm 2.25V$ V+ = 2.75V, V- = -7.25V V+ = 7.25V, V- = -2.75V	3	-55^{o}C	-	2.0	µA/V
ΔInverting Input (-IN) Current Between Channels	ΔI_{BSN}	$V_{CM} = 0$	1	+25^{o}C	-15	15	µA
			2, 3	+125^{o}C	-30	30	µA
Inverting Input (-IN) Current	I_{BSN}	$V_{CM} = 0V$	1	+25^{o}C	-12	12	µA
			2, 3	+125^{o}C, -55^{o}C	-30	30	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_{SOURCE} = 0Ω, R_L = 400Ω, V_{OUT} = 0V, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
-IN Current Common Mode Sensitivity	CMS_{IBN}	ΔV_{CM} = ±2.5V V+ = 2.5V, V- = -7.5V V+ = 7.5V, V- = -2.5V	1	+25°C	-	0.4	µA/V
			2	+125°C	-	5	µA/V
		ΔV_{CM} = ±2.25V V+ = 2.75V, V- = -7.25V V+ = 7.25V, V- = -2.75V	3	-55°C	-	5	µA/V
-IN Current Power Supply Sensitivity	PSS_{IBN}	ΔV_{SUP} = ±1.5V V+ = 6.5V, V- = -5V V+ = 3.5V, V- = -5V	1	+25°C	-	0.2	µA/V
			2, 3	+125°C, -55°C	-	0.5	µA/V
+IN Current Power Supply Sensitivity	PSS_{IBP}	ΔV_{SUP} = ±1.5V V+ = 6.5V, V- = -5V V+ = 3.5V, V- = -5V	1	+25°C	-	0.1	µA/V
			2, 3	+125°C, -55°C	-	0.3	µA/V
Output Voltage Swing	V_{OP}	A_V = +1, R_L = 150Ω, V_{IN} = -3V	1	+25°C	2.5	-	V
		V_{IN} = -3V	2, 3	+125°C, -55°C	2.5	-	V
	V_{ON}	A_V = +1, R_L = 150Ω, V_{IN} = +3V	1	+25°C	-	-2.5	V
		V_{IN} = +3V	2, 3	+125°C, -55°C	-	-2.5	V
Short Circuit Output Current	$+I_{SC}$	V_{IN} = ±2.5V V_{OUT} = 0V	1	+25°C	50	-	mA
			2, 3	+125°C, -55°C	50	-	mA
	$-I_{SC}$	V_{IN} = ±2.5V V_{OUT} = 0V	1	+25°C	-	-40	mA
			2, 3	+125°C, -55°C	-	-40	mA
Output Current	$+I_{OUT}$	Note 1	1	+25°C	20	-	mA
			2, 3	+125°C, -55°C	16.6	-	mA
	$-I_{OUT}$	Note 1	1	+25°C	-	-20	mA
			2, 3	+125°C, -55°C	-	-16.6	mA
Quiescent Power Supply Current	I_{CC}	R_L = 400Ω	1	+25°C	-	10	mA/Op Amp
			2, 3	+125°C, -55°C	-	10	mA/Op Amp
	I_{EE}	R_L = 400Ω	1	+25°C	-10	-	mA/Op Amp
			2, 3	+125°C, -55°C	-10	-	mA/Op Amp
Transimpedance	$+A_{ZOL1}$	R_L = 400Ω V_{OUT} = ±2.5V	1	+25°C	1	-	MΩ
			2	+125°C	0.5	-	MΩ
		V_{OUT} = ±2.25V	3	-55°C	0.5	-	MΩ
	$-A_{ZOL1}$	R_L = 400Ω V_{OUT} = ±2.5V	1	+25°C	1	-	MΩ
			2	+125°C	0.5	-	MΩ
		V_{OUT} = ±2.25V	3	-55°C	0.5	-	MΩ

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_{SOURCE} = 0Ω, R_L = 400Ω, V_{OUT} = 0V, $V_{\overline{DISABLE}}$ = V+, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Disabled Output Current	$+I_{LEAK}$	V_{IN} = 0V, V_{OUT} = +2.5V R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	-	1	µA
			2, 3	+125°C, -55°C	-	2	µA
	$-I_{LEAK}$	V_{IN} = 0V, V_{OUT} = -2.5V R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	-	1	µA
			2, 3	+125°C, -55°C	-	2	µA
Disable Pin Input Current	I_{LOGIC}	$V_{\overline{DIS}}$ = 0V	1	+25°C	-1.0	-	mA
			2, 3	+125°C, -55°C	-1.5	-	mA
Minimum $\overline{DISABLE}$ Pin Current to Disable	I_{DIS}	Note 2	1	+25°C	-	350	µA
			2, 3	+125°C, -55°C	-	350	µA
Maximum $\overline{DISABLE}$ Pin Current to Enable	I_{EN}	Note 3	1	+25°C	20	-	µA
			2, 3	+125°C, -55°C	20	-	µA
Disabled Power Supply Current	I_{CCDIS}	R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	-	7.5	mA/Op Amp
			2, 3	+125°C, -55°C	-	7.5	mA/Op Amp
	I_{EEDIS}	R_L = Open, $V_{\overline{DIS}}$ = 0V	1	+25°C	7.5	-	mA/Op Amp

NOTES:

1. Guaranteed from V_{OUT} Test with R_L = 150Ω, by: $I_{OUT} = V_{OUT}/150Ω$.
2. R_L = 100Ω, V_{IN} = 2.5V. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when -10mV ≤ V_{OUT} ≤ +10mV.
3. V_{IN} = 0V. This is the maximum current that can be pulled out of the $\overline{Disable}$ pin with the HA5022/883 remaining enabled. The HA5022/883 is considered disabled when the supply current has decreased by at least 0.5mA.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±5V, A_V = +2, R_F = 681Ω, R_L = 400Ω, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
-3dB Bandwidth	BW(+1)	A_V = +1, R_F = 1K V_{OUT} = 100mV_{RMS}	1	+125°C, -55°C	70	-	MHz
	BW(+2)	A_V = +2, V_{OUT} = 100mV_{RMS}	1	+125°C, -55°C	70	-	MHz
Gain Flatness	GF5	A_V = +2, f ≤5MHz V_{OUT} = 100mV_{RMS}	1	+125°C, -55°C	-	±0.045	dB
	GF10	A_V = +2, f ≤10MHz V_{OUT} = 100mV_{RMS}	1	+125°C, -55°C	-	±0.085	dB
	GF20	A_V = +2, f ≤20MHz V_{OUT} = 100mV_{RMS}	1	+125°C, -55°C	-	±0.65	dB

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V_{SUPPLY} = ±5V, A_V = +2, R_F = 681Ω, R_L = 400Ω, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR(+1)	A_V = +1, R_F = 1K V_{OUT} = -2V to +2V	1, 4	+125°C, -55°C	300	-	V/µs
	-SR(+1)	A_V = +1, R_F = 1K V_{OUT} = +2V to -2V	1, 4	+125°C, -55°C	270	-	V/µs
	+SR(+2)	A_V = +2, V_{OUT} = -2V to +2V	1, 4	+125°C, -55°C	465	-	V/µs
	-SR(+2)	A_V = +2, V_{OUT} = +2V to -2V	1, 4	+125°C, -55°C	350	-	V/µs
Rise and Fall Time	T_R	A_V = +2, V_{OUT} = -0.5V to -0.5V	1, 2	+125°C, -55°C	-	5.5	ns
	T_F	A_V = +2, V_{OUT} = +0.5V to +0.5V	1, 2	+125°C, -55°C	-	6.0	ns
Overshoot	+OS	A_V = +2, V_{OUT} = -0.5V to +0.5V	1, 3	+125°C, -55°C	-	35	%
	-OS	A_V = +2, V_{OUT} = +0.5V to -0.5V	1, 3	+125°C, -55°C	-	27	%
Propagation Delay	$+T_P$	A_V = +2, R_F = 681Ω V_{OUT} = 0V to 1V	1, 2	+125°C, -55°C	-	10	ns
	$-T_P$	A_V = +2, R_F = 681Ω V_{OUT} = 1V to 0V	1, 2	+125°C, -55°C	-	9.5	ns

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot-to-lot and within lot variation.
2. Measured between 10% and 90% points.
3. For 200ps input transition times. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Performance Curves.
4. Measured between 25% and 75% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4
Group A Test Requirements	1, 2, 3, 4
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Test Circuits and Waveforms

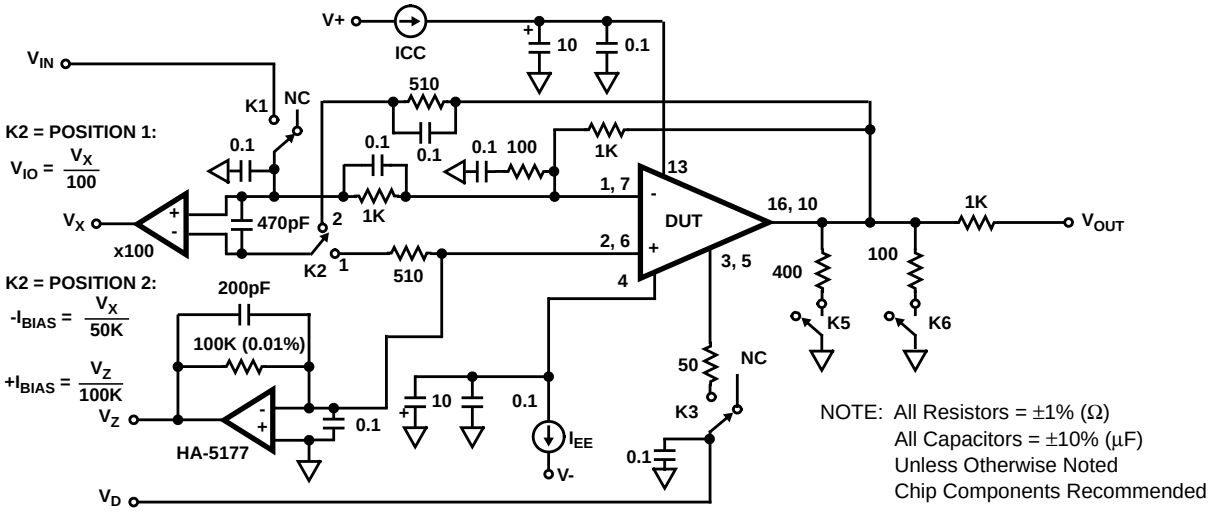


FIGURE 1. TEST CIRCUIT (Applies to Table 1)

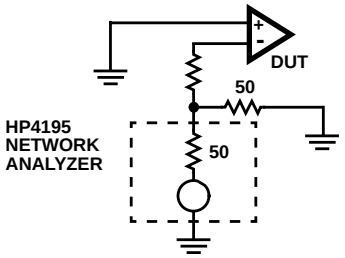


FIGURE 2. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

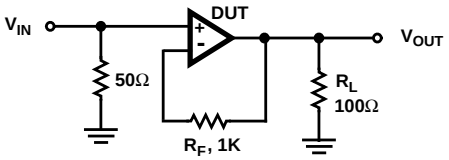


FIGURE 3. SMALL SIGNAL PULSE RESPONSE CIRCUIT

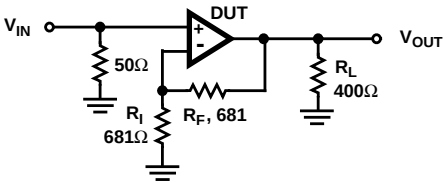


FIGURE 4. LARGE SIGNAL PULSE RESPONSE CIRCUIT

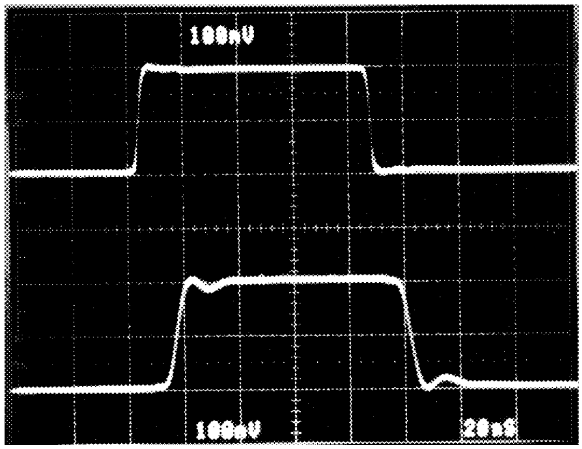


FIGURE 5. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

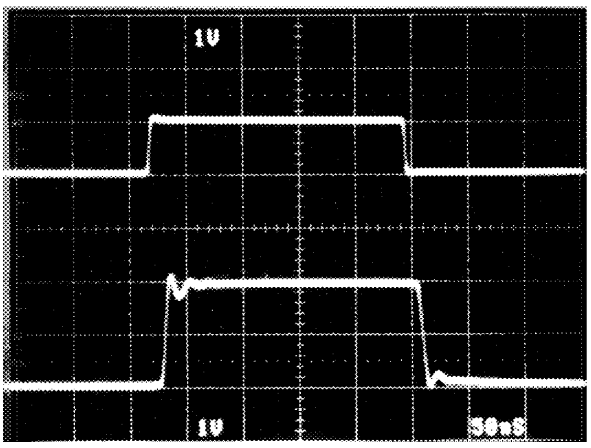
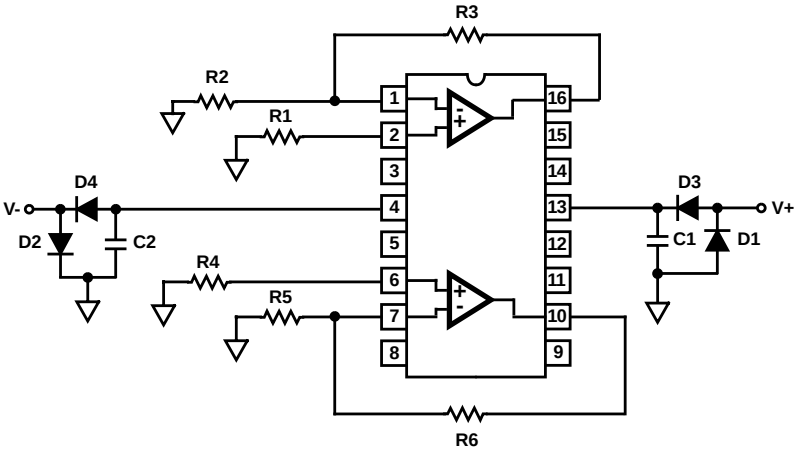


FIGURE 6. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Burn-In Circuit

HA5022MJ/883 CERAMIC DIP



NOTES:

R1 = R2 = R4 = R5 = 1kΩ, ±5% (Per Socket)
R3 = R6 = 10kΩ, ±5% (Per Socket)
C1 = C2 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
D1 = D2 = 1N4002 or Equivalent (Per Board)
D3 = D4 = 1N4002 or Equivalent (Per Socket)
V+ = +5.5V ± 0.5V
V- = -5.5V ± 0.5V

Die Characteristics

DIE DIMENSIONS:
65 x 100 x 19 mils ± 1 mils
1650 x 2540 x 483µm ± 25.4µm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ± 0.4kÅ, Metal 2: 16kÅ ± 0.8kÅ

WORST CASE CURRENT DENSITY:
1.62 x 10^5 A/cm^2 at 35mA

SUBSTRATE POTENTIAL (Powered Up): V-

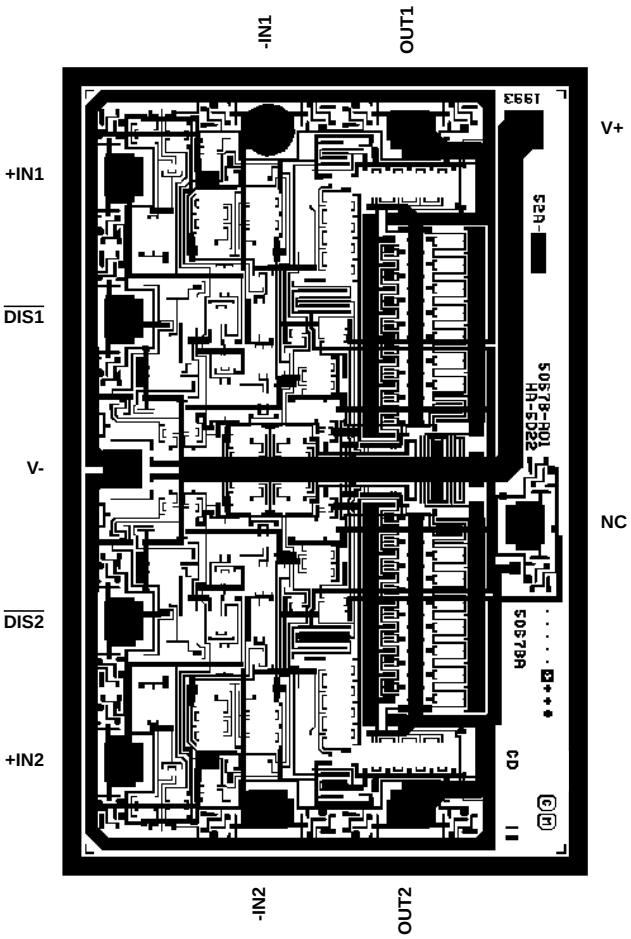
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.4kÅ

TRANSISTOR COUNT: 124

PROCESS: Bipolar Dielectric Isolation

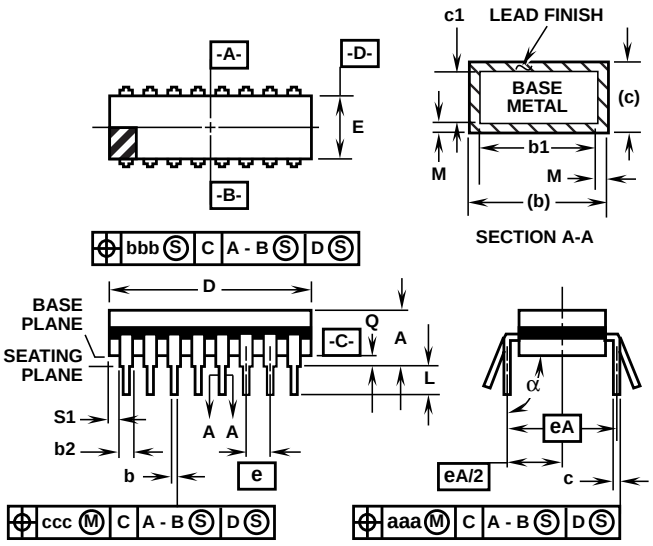
Metallization Mask Layout

HA5022/883



Spec Number **511107-883**

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

DESIGN INFORMATION

Dual 125MHz Video Current Feedback Amplifier with Disable

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified.

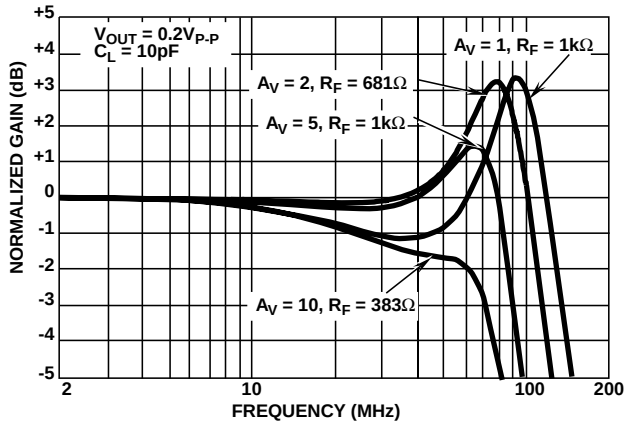

FIGURE 1. NON-INVERTING FREQUENCY RESPONSE

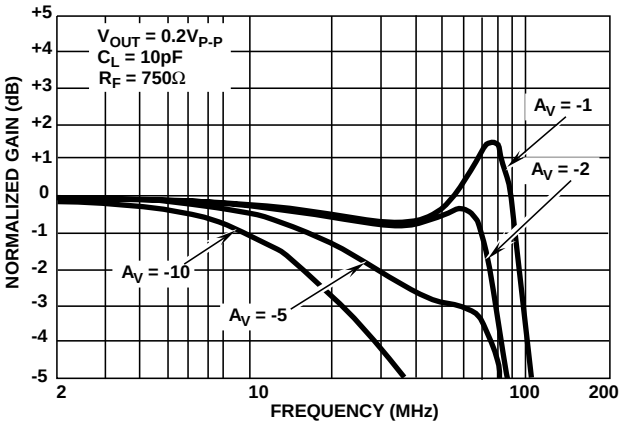

FIGURE 2. INVERTING FREQUENCY RESPONSE

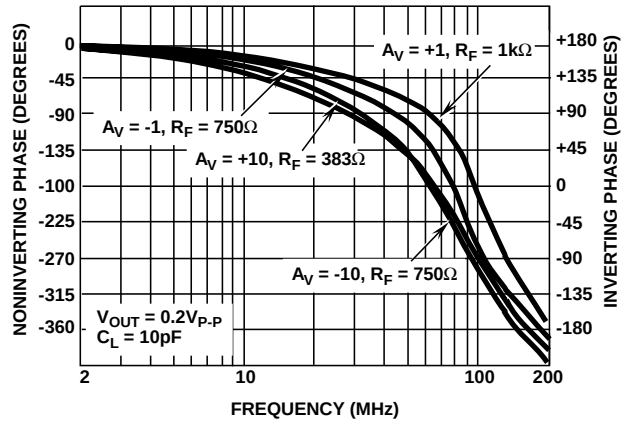

FIGURE 3. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

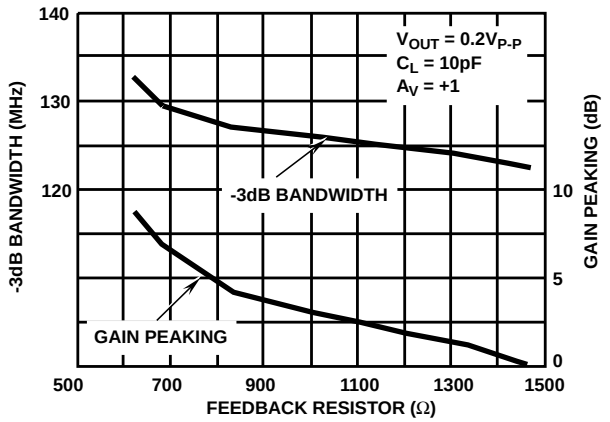

FIGURE 4. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

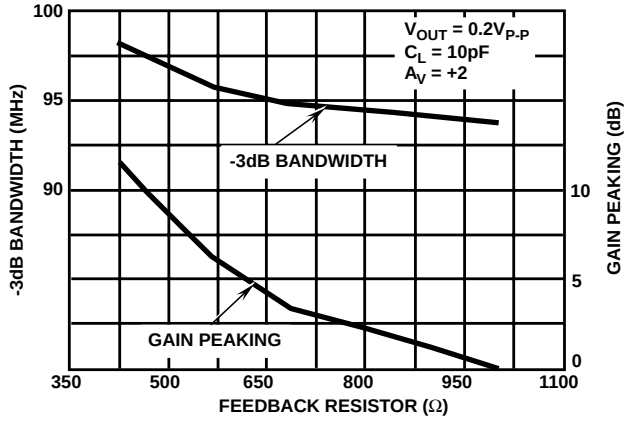

FIGURE 5. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

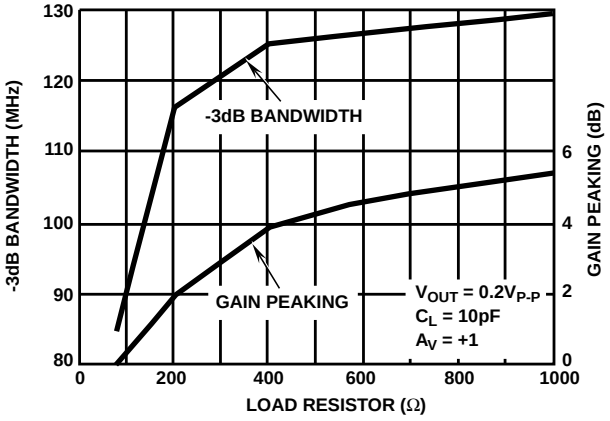

FIGURE 6. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified. (Continued)

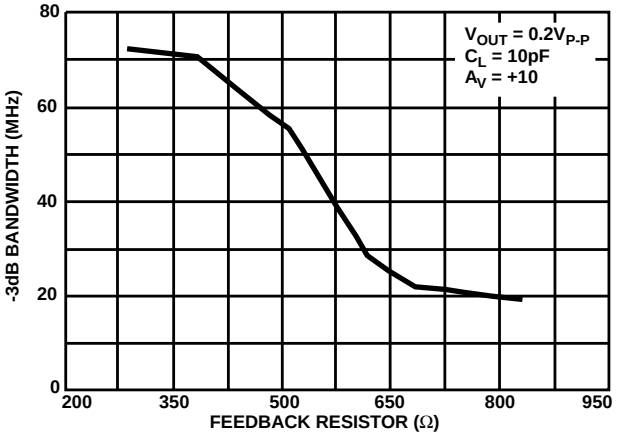

FIGURE 7. BANDWIDTH vs FEEDBACK RESISTANCE

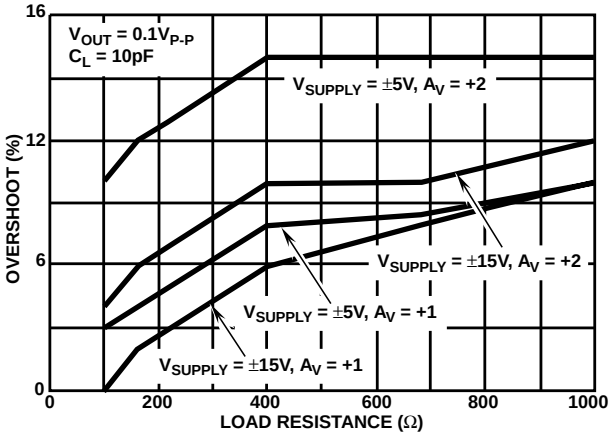

FIGURE 8. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

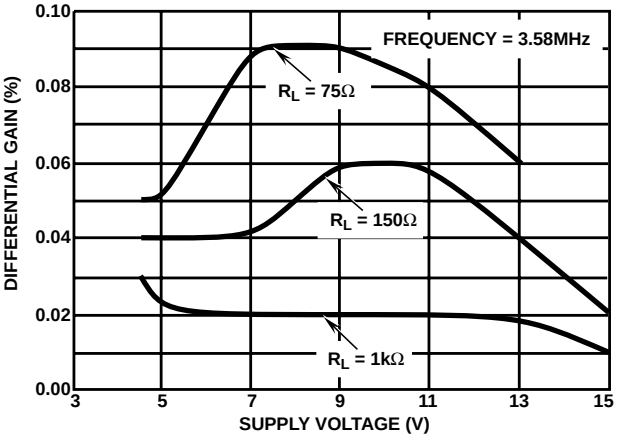

FIGURE 9. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

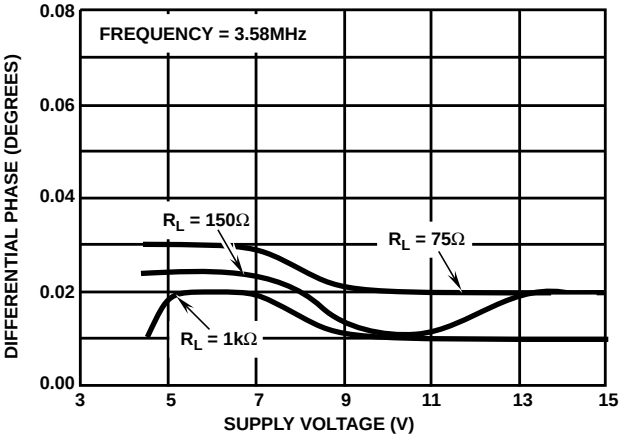

FIGURE 10. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

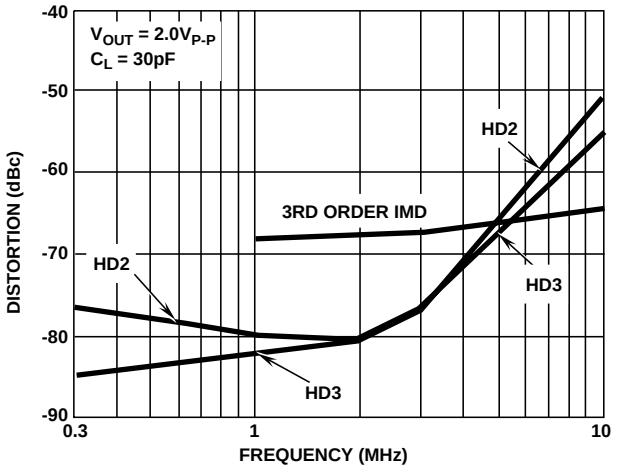

FIGURE 11. DISTORTION vs FREQUENCY

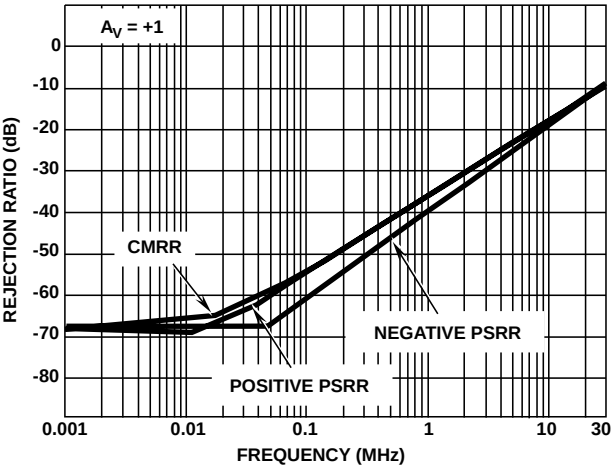

FIGURE 12. REJECTION RATIOS vs FREQUENCY

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified. (Continued)

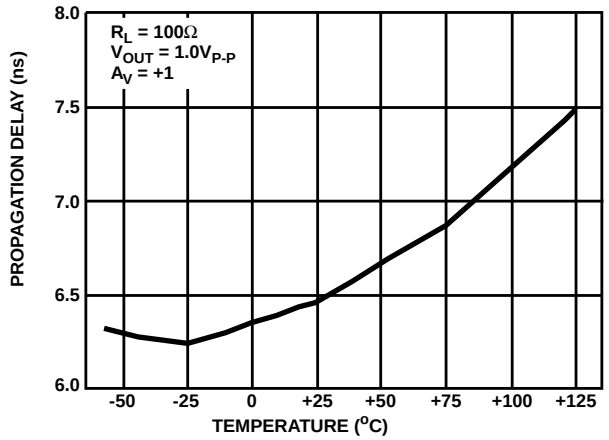

FIGURE 13. PROPAGATION DELAY vs TEMPERATURE

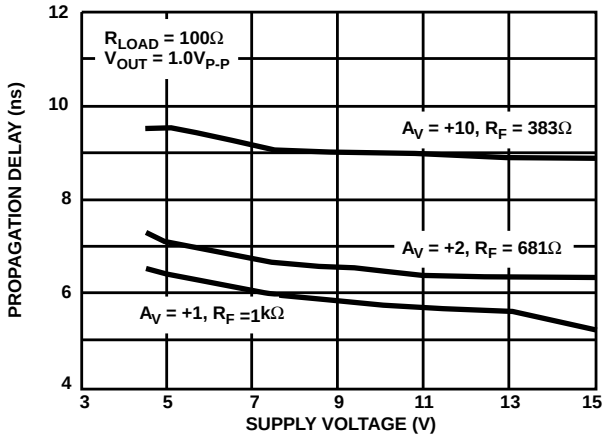

FIGURE 14. PROPAGATION DELAY vs SUPPLY VOLTAGE

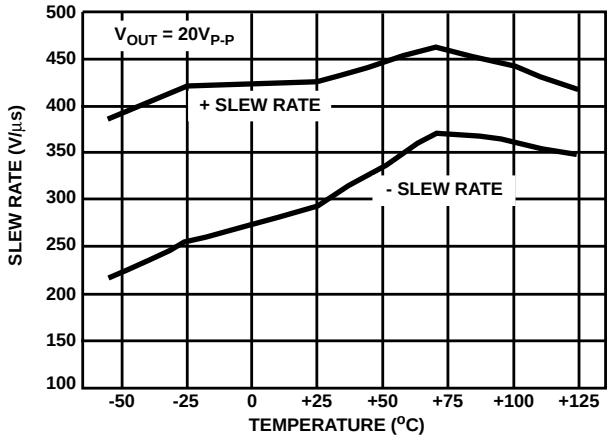

FIGURE 15. SLEW RATE vs TEMPERATURE

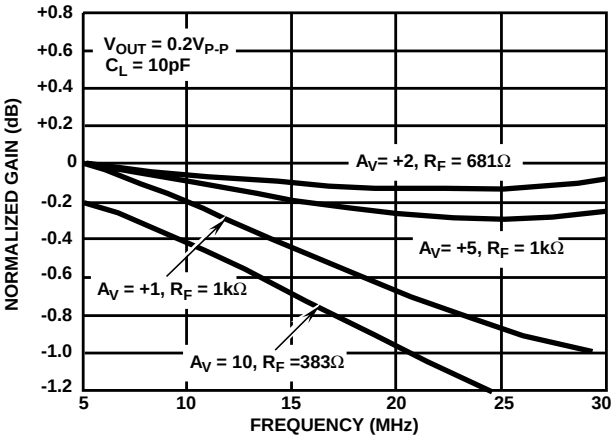

FIGURE 16. NON-INVERTING GAIN FLATNESS vs FREQUENCY

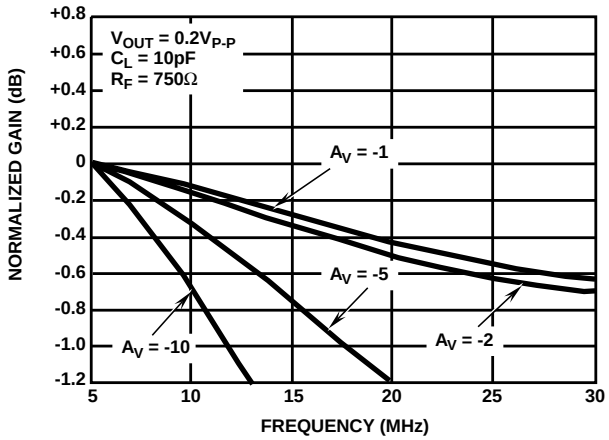

FIGURE 17. INVERTING GAIN FLATNESS vs FREQUENCY

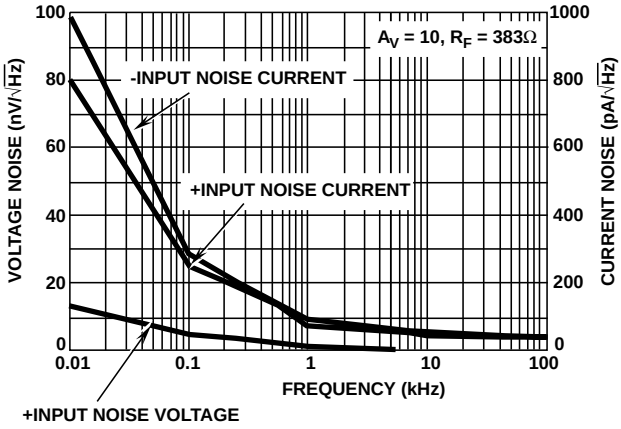

FIGURE 18. INPUT NOISE CHARACTERISTICS

DESIGN INFORMATION (Continued)

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Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified. (Continued)

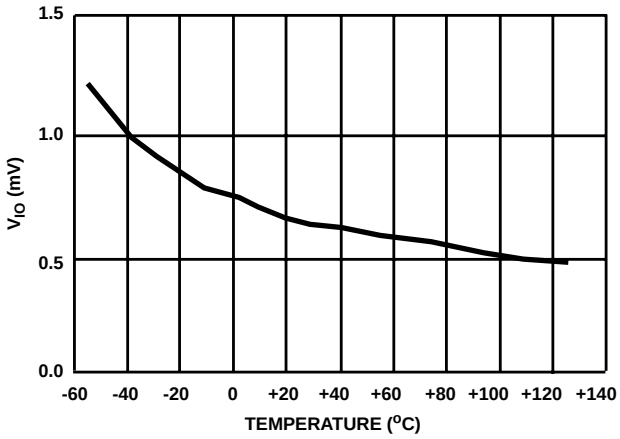

FIGURE 19. INPUT OFFSET VOLTAGE vs TEMPERATURE

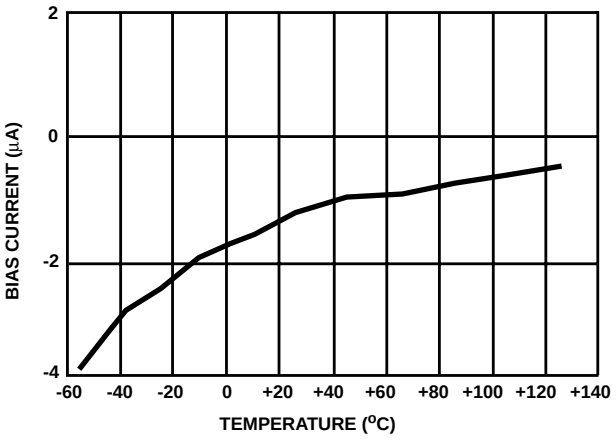

FIGURE 20. +INPUT BIAS CURRENT vs TEMPERATURE

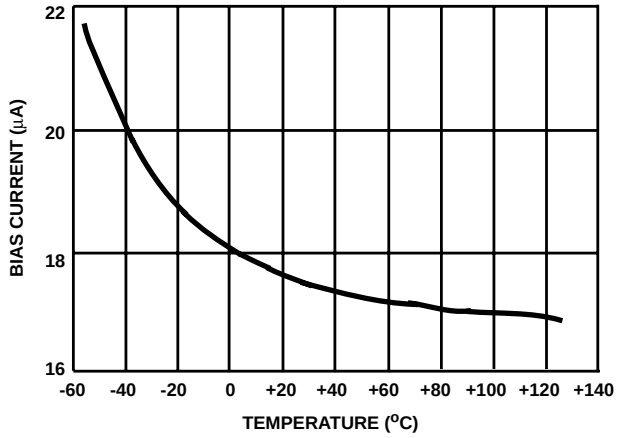

FIGURE 21. -INPUT BIAS CURRENT vs TEMPERATURE

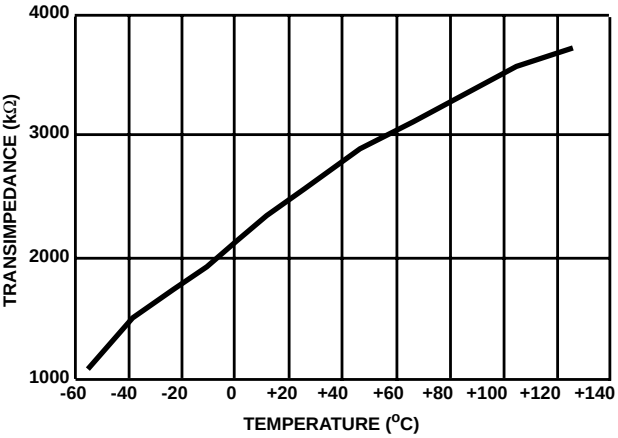

FIGURE 22. TRANSIMPEDANCE vs TEMPERATURE

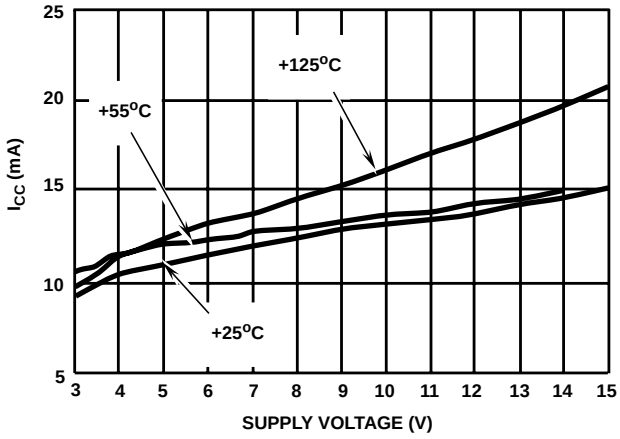

FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

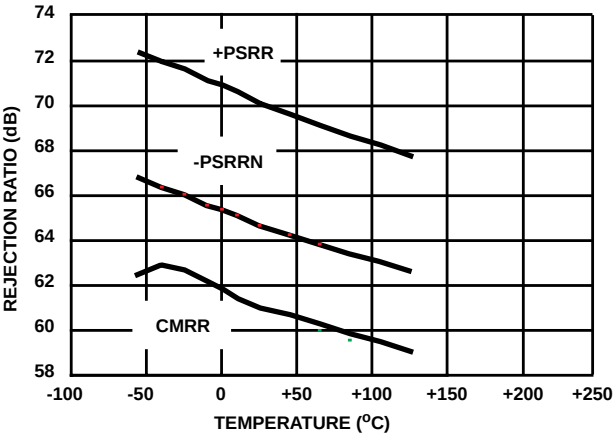

FIGURE 24. REJECTION RATIO vs TEMPERATURE

DESIGN INFORMATION (Continued)

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Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified. (Continued)

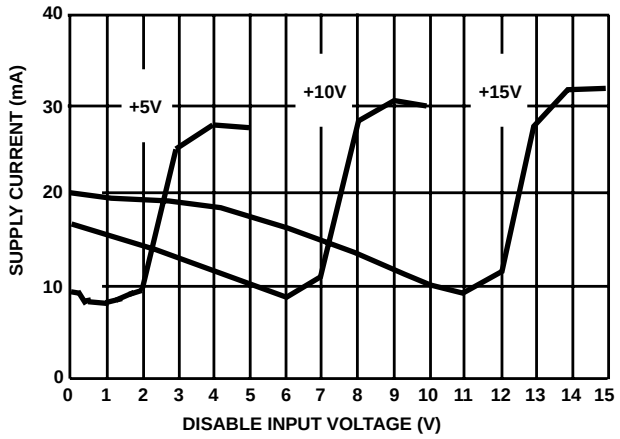

FIGURE 25. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

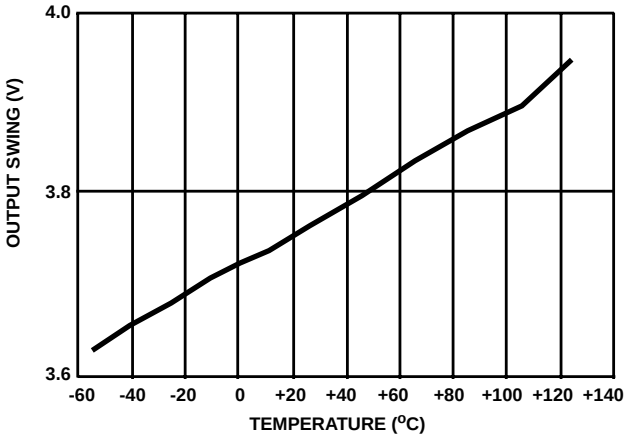

FIGURE 26. OUTPUT SWING vs TEMPERATURE

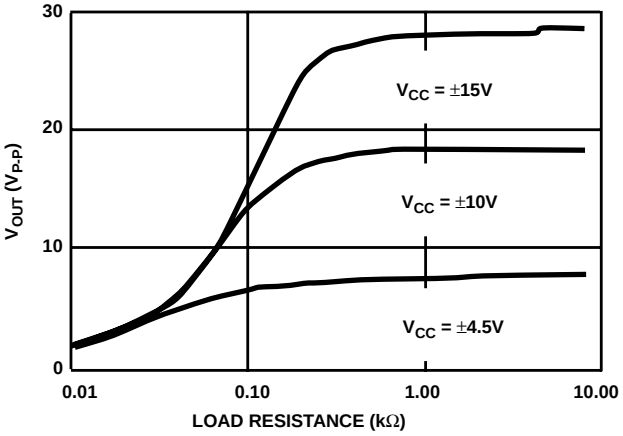

FIGURE 27. OUTPUT SWING vs LOAD RESISTANCE

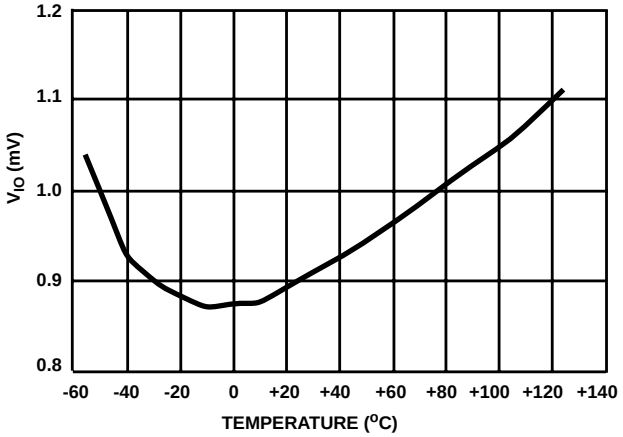

FIGURE 28. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

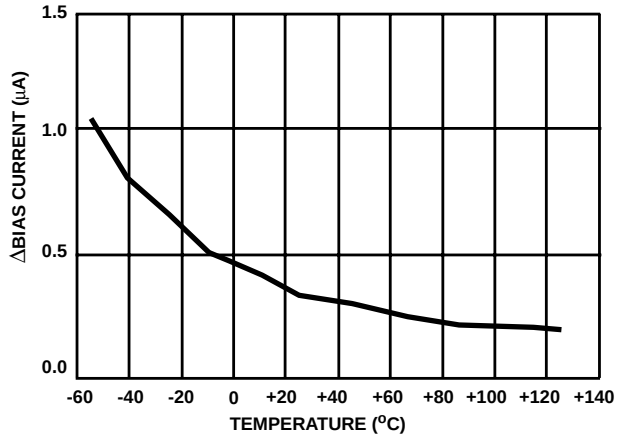

FIGURE 29. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

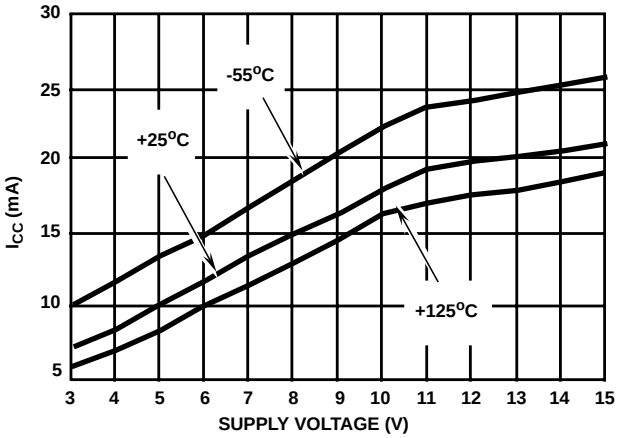

FIGURE 30. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

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Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified. (Continued)

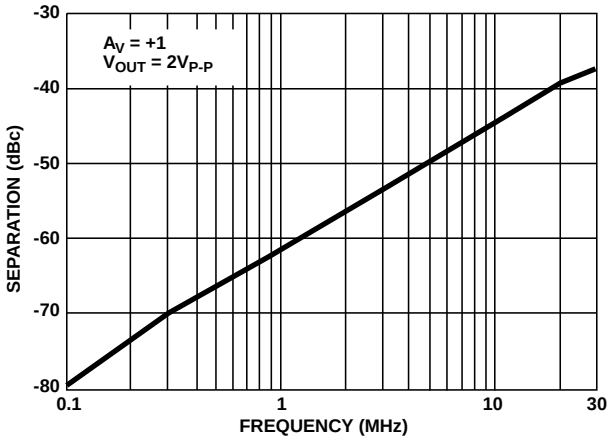

FIGURE 31. CHANNEL SEPARATION vs FREQUENCY

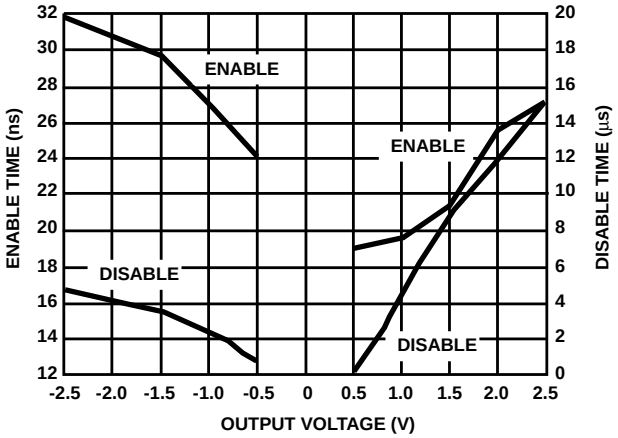

FIGURE 32. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

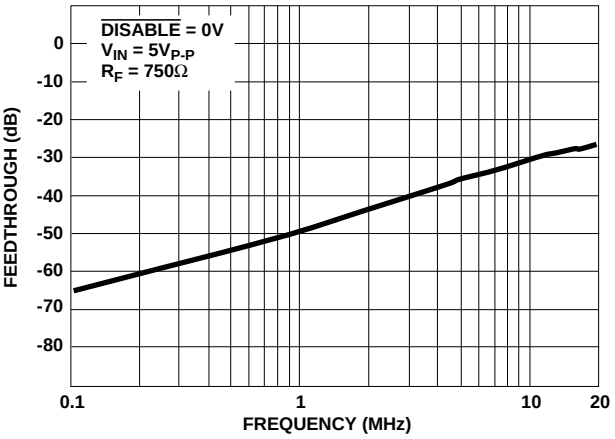

FIGURE 33. DISABLE FEEDTHROUGH vs FREQUENCY

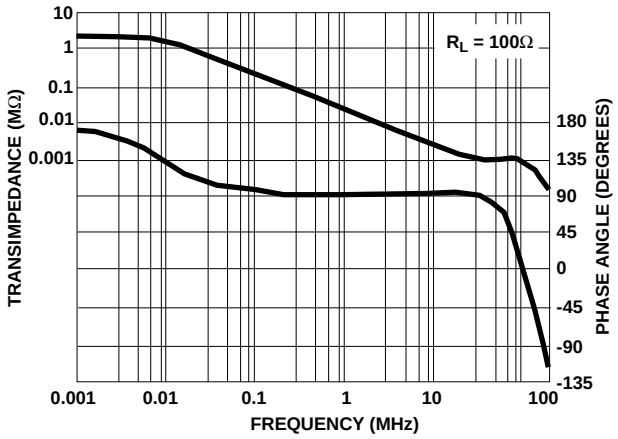

FIGURE 34. TRANSIMPEDANCE vs FREQUENCY

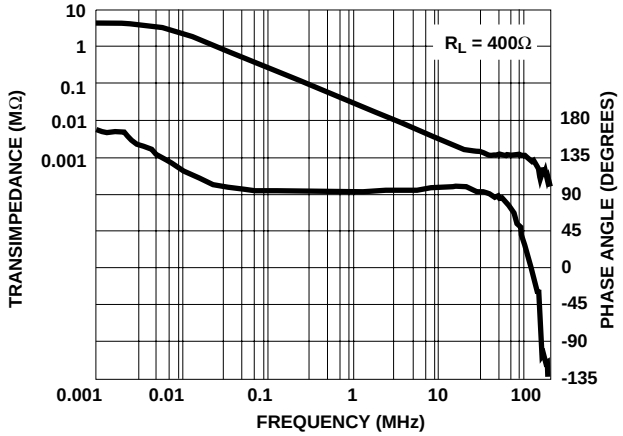

FIGURE 35. TRANSIMPEDANCE vs FREQUENCY

DESIGN INFORMATION (Continued)

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Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 1 and Figure 2 in the Typical Performance Curves section, illustrate the performance of the HA5022 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5022 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 36.

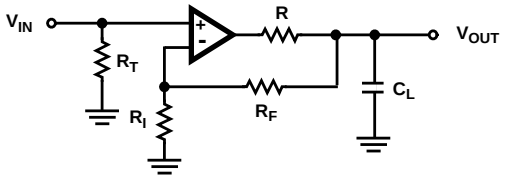

FIGURE 36. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in dual amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 37 shows the maximum ambient temperature versus supply voltage for the available package styles. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

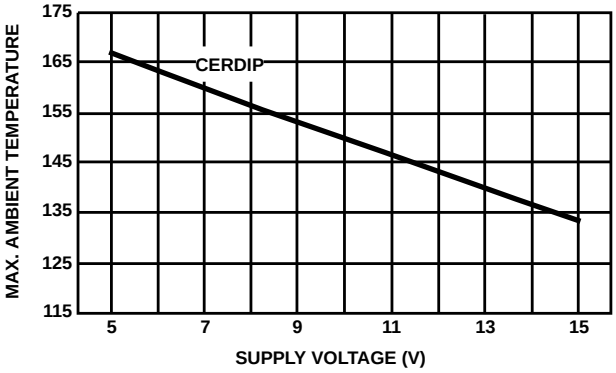

FIGURE 37. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 38 is a simplified schematic of

DESIGN INFORMATION (Continued)

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the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350µA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

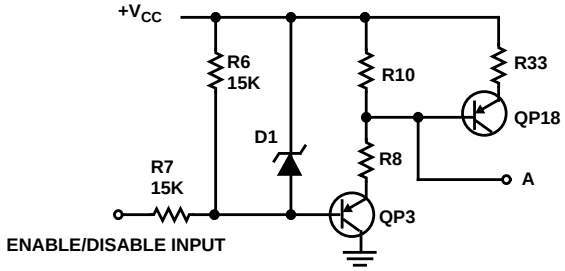

FIGURE 38. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5 volts the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20µA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Two Channel Video Multiplexer

Referring to the amplifier U1A in Figure 39, R1 terminates the cable in its characteristic impedance of 75Ω, and R4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R3 can be changed if a different network gain is desired. R5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other circuit, U1b, operates in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5022 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5022, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5022 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 40, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R2 and R3 determine the amplifier gain, and if a different gain is desired R2 should be changed according to the equation G = (1 + R3/R2). R3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing it's value. R5, C1 and D1 are an asymmetrical charge/discharge time circuit which configures U1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 40 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved. The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

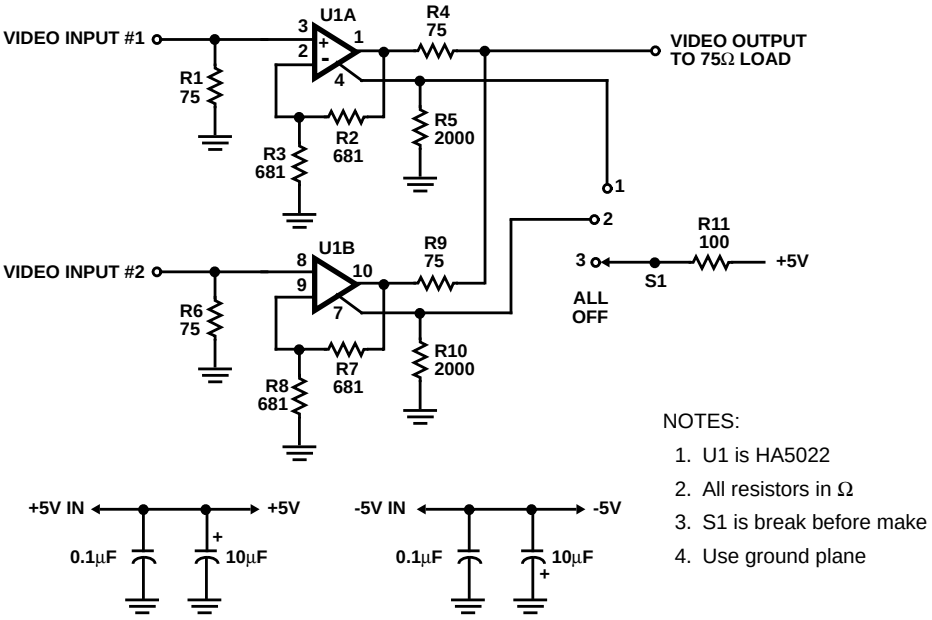

FIGURE 39. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER

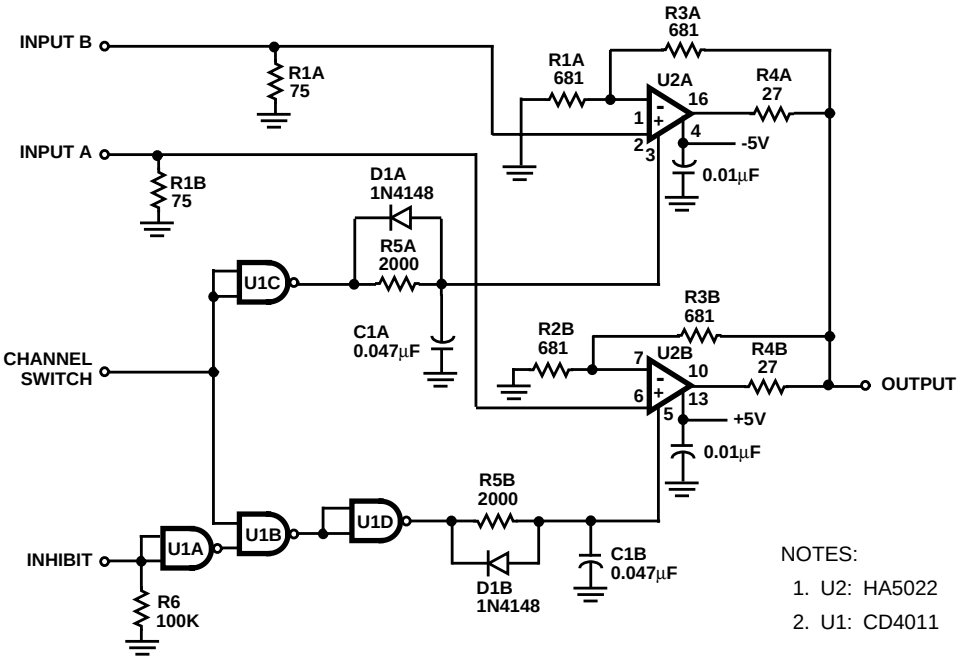

FIGURE 40. LOW IMPEDANCE MULTIPLEXER

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	µA
	A	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3) (+ $I_{BCMR} = \frac{1}{R_{IN}}$)	A	+25°C	-	-	0.15	µA/V
	A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	µA/V
	A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current	A	+25°C, +85°C	-	4	12	µA
	A	-40°C	-	10	30	µA
Delta -IN BIAS Current Between Channels	A	+25°C, +85°C	-	6	15	µA
	A	-40°C	-	10	30	µA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	µA/V
	A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	µA/V
	A	Full	-	-	0.5	µA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	nV/√Hz
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	pA/√Hz
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	pA/√Hz

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I			UNITS
			MIN	TYP	MAX	
TRANSFER CHARACTERISTICS						
Transimpedance (Note 21)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain R_L = 400Ω, V_{OUT} = ±2.5V	A	+25°C	70	-	-	dB
	A	Full	65	-	-	dB
Open Loop DC Voltage Gain R_L = 100Ω, V_{OUT} = ±2.5V	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 20)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 20)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note 13)	A	Full	±40	±60	-	mA
Output Current (Disabled, Notes 5, 14)	A	Full	-	-	2	µA
Output Disable Time (Note 15)	B	+25°C	-	40	-	µs
Output Enable Time (Note 16)	B	+25°C	-	40	-	ns
Output Capacitance (Disabled, Notes 5, 17)	B	+25°C	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled (Note 5)	A	Full	-	5	7.5	mA/Op Amp
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 6)	A	Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 7)	A	Full	-	-	20	µA
AC CHARACTERISTICS (A_V = +1)						
Slew Rate (Note 8)	B	+25°C	275	400	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	22	28	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I			UNITS
			MIN	TYP	MAX	
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)						
Slew Rate (Note 8)	B	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	-	26	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	100	-	ns
Gain Flatness 5MHz	B	+25°C	-	0.02	-	dB
Gain Flatness 20MHz	B	+25°C	-	0.07	-	dB
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)						
Slew Rate (Note 8)	B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	28	38	-	MHz
Rise Time (Note 10)	B	+25°C	-	8	-	ns
Fall Time (Note 10)	B	+25°C	-	9	-	ns
Propagation Delay (Note 10)	B	+25°C	-	9	-	ns
Overshoot	B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step	B	+25°C	-	130	-	ns

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I			UNITS
			MIN	TYP	MAX	
VIDEO CHARACTERISTICS						
Differential Gain (Notes 18, 20)	B	+25°C	-	0.03	-	%
Differential Phase (Notes 18, 20)	B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. V_{CM} = ±2.5V. At -40°C Product is tested at V_{CM} = ±2.25V because short test duration does not allow self heating.
4. ±3.5V ≤ V_S ≤ ±6.5V.
5. $\overline{\text{Disable}}$ = 0V.
6. R_L = 100Ω, V_{IN} = 2.5V. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when -10mV ≤ V_{OUT} ≤ +10mV.
7. V_{IN} = 0V. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5024 remaining enabled. The HA5024 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_{PEAK} = 2V
10. R_L = 100Ω, V_{OUT} = 1V. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. R_L = 400Ω, V_{OUT} = 100mV.
12. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
13. V_{IN} = ±2.5V, V_{OUT} = 0V.
14. V_{OUT} = ±2.5V, V_{IN} = OV.
15. V_{IN} = +2V, $\overline{\text{Disable}}$ = +5V to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to V_{OUT} = 0V.
16. V_{IN} = +2V, $\overline{\text{Disable}}$ = 0V to +5V. Measured from the 50% point of $\overline{\text{Disable}}$ to V_{OUT} = 2V.
17. V_{IN} = 0V, Force V_{OUT} from 0V to ±2.5V, t_R = t_F = 50ns.
18. Measured with a VM700A video tester using an NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
20. R_L = 150Ω .
21. V_{OUT} = ± 2.5V. At -40°C Product is tested at V_{OUT} = ±2.25V because short test duration does not allow self heating.
22. ESD Protection is for human body model tested per MIL-STD-883, Method 3015.7.