Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to +6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current, Per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or GND Current, I_{CC} or I_{GND}
For Up to 4 Outputs Per Device, Add ±25mA For Each Additional Output . . . . . ±100mA

Power Dissipation Per Package, P_D
T_A = -55°C to +100°C (Package F) 500mW
T_A = +100°C to +125°C (Package F) . . . . . Derate Linearly at 8mW/°C to 300mW
Operating Temperature Range, T_A
Package Type F . . . . . -55°C to +125°C
Storage Temperature, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case For 10s Max . . . . . +265°C
Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)
With Solder Contacting Lead Tips Only . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}
Unless Otherwise Specified, All Voltages Referenced to GND
T_A = Full Package Temperature Range
CD54AC Types . . . . . 1.5V to 5.5V
CD54ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}

Operating Temperature, T_A . . . . . -55°C to +125°C
Input Rise and Fall Slew Rate, dt/dv
at 1.5V to 3V (AC Types) . . . . . 0ns/V to 50ns/V
at 3.6V to 5.5V (AC Types) . . . . . 0ns/V to 20ns/V
at 4.5V to 5.5V (AC Types) . . . . . 0ns/V to 10ns/V

HARRIS SEMICONDUCTOR

CD54AC299/3A
CD54ACT299/3A

8-Input Universal Shift/Storage Registers with Common Parallel I/O Pins

June 1997

COMPLETE DATA SHEET COMING SOON!

Description

The CD54AC299/3A and CD54ACT299/3A are three-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices utilize the Harris Advanced CMOS Logic technology. These registers have four synchronous operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DS0, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-to-HIGH transition of the clock pulse (CP). S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

The Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When $\overline{MR}$ is LOW, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The three-state input/output (I/O) port has three modes of operation

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW, the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a three-state output and a CMOS buffer input.

The CD54AC299/3A and CD54ACT299/3A are supplied in 20 lead dual-in-line ceramic packages (F suffix).

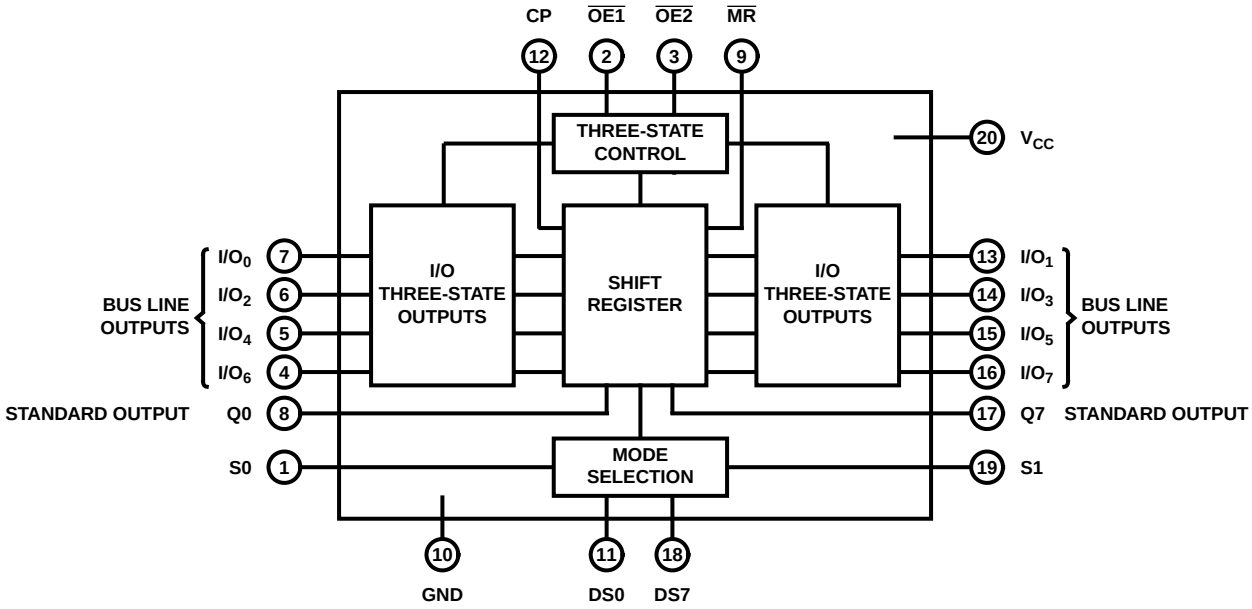
ACT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
S1, S2, $\overline{OE1}$, $\overline{OE2}$	0.83
SL, CP	0.67
$\overline{MR}$	1.33

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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