

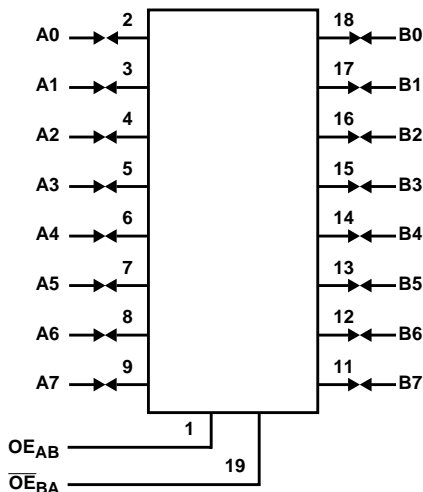
Octal Bus Transceiver Three-State, Non-Inverting

July 1998

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- Meets JEDEC Standard No. 20
- SCR - Latch-Up-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST/A/S with Significantly Reduced Power Consumption
- Functionally and Pin-Compatible with Industry 54 Bipolar Types in the FAST, AS and S Series
- Balanced Propagation Delays
- Military Operating Temperature Range
 - Ceramic (CERDIP) 54 Series: -55 to 125°C
- $\pm 24\text{mA}$ Output Drive Current, Drives 75Ω Lines without Need for Terminations
- Fan Out (Over Temperature)
 - ACL Loads 2400
 - FAST Loads..... 15
 - AS Loads..... 48
- Operation Voltage 4.5V to 5.5V

Functional Diagram



Description

The CD54ACT623F3A is an octal bus transceiver that utilizes Harris Advanced CMOS Logic technology. It is a non-inverting three-state bidirectional transceiver-buffer that allows for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus depending on the logic levels of the Output Enable (OE_{AB} , \overline{OE}_{BA}) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling OE_{AB} and \overline{OE}_{BA} . Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high-impedance, both sets of bus lines will remain in their last states.

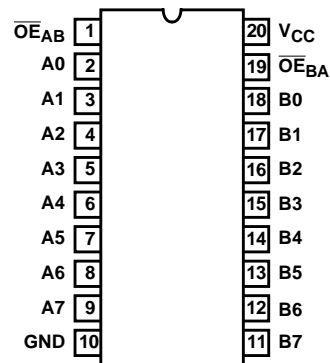
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54ACT623F3A	-55 to 125	20 Ld CERDIP	F20.3

NOTE:

1. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout



CD54ACT623F3A

ACT Input Load Table

INPUT	UNIT LOAD
An, Bn	0.83
\overline{OE}_{BA}	0.64
OE_{AB}	0.15

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r , $t_f = 3ns$, $C_L = 50pF$ (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-55°C TO 125°C			UNITS
			MIN	TYP	MAX	
Propagation Delay, Data to Output	t_{PLH} , t_{PHL}	5 (Note 10)	1.8	-	10.6 (Note 8)	ns
Propagation Delay, Output Disable to Output	t_{PLZ} , t_{PHZ}	5	2.5	-	14.4 (Note 8)	ns
Propagation Delay, Output Enable to Output	t_{PZL} , t_{PZH}	5	2.5	-	14.4 (Note 8)	ns
Minimum (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Figure 1	5	-	4 at 25°C	-	V
Maximum (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Figure 1	5	-	1 at 25°C	-	V
Three-State Output Capacitance	C_O	-	-	-	15	pF
Input Capacitance	C_I	-	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	79	-	pF

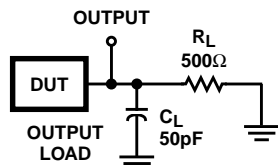
NOTES:

8. Limits tested 100%.
9. 3.3V Min = 3.6V, Max = 3V.
10. 5V Min = 5.5V, Max = 4.5V
11. C_{PD} is used to determine the dynamic power consumption per gate.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Burn-In Test Circuit Connections (Use DC II for F3A Burn-In and AC for Life Test)

DC	DC BURN-IN I			DC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54ACT623	2-9	1, 10-19	20	11-18	10	1-9, 19, 20
AC	OPEN	GROUND	$1/2 V_{CC}$ (3V)	V_{CC} (6V)	OSCILLATOR	
					50kHz	25kHz
CD54ACT623	-	10	11-18	19, 20	2-9	1

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k Ω -47k Ω .



	CD54ACT
Input Level	3V
Input Switching Voltage, V_S	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}

FIGURE 1. PROPAGATION DELAY TIMES