

April 1995

8-Bit 500 MSPS Flash A/D Converter

Features

- Differential Linearity Error ± 0.5 LSB or Less
- Integral Linearity Error ± 0.7 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 500 MSPS (Min)
- Low Input Capacitance 20pF (Typ)
- Wide Analog Input Bandwidth 300MHz (Min. for Full-Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 2.8W (Typ)
- Low Error Rate
- Capable of Driving 50 Ω Loads

Applications

- Radar Systems
- Communication Systems
- Digital Oscilloscopes
- Direct RF Down-Conversion

Description

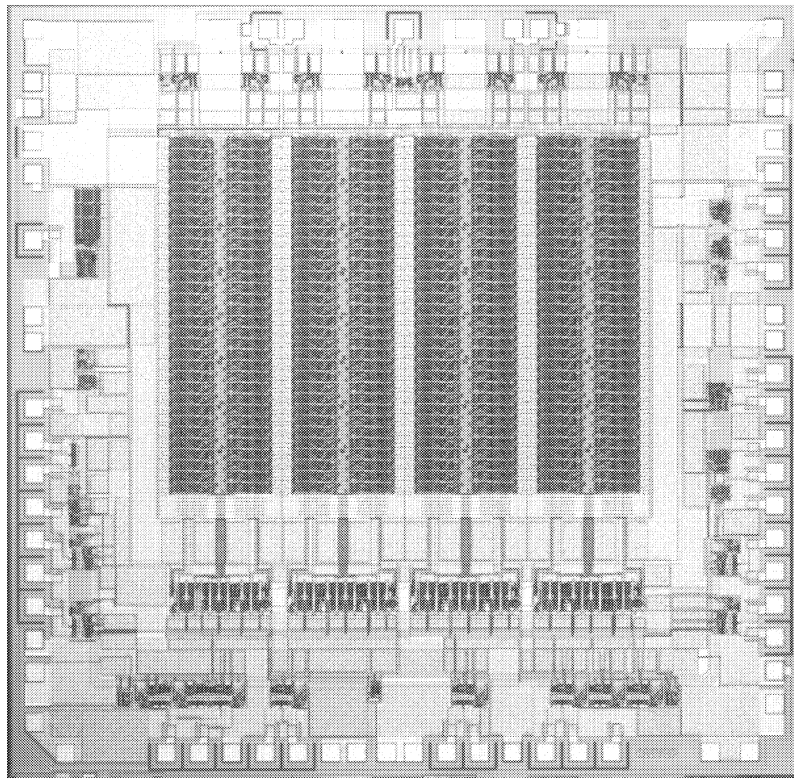
This is a specification that outlines the mechanical and electrical characteristics for the HI1276Y, 8-bit Flash A/D converter IC, in chip (die) form.

Ordering Information

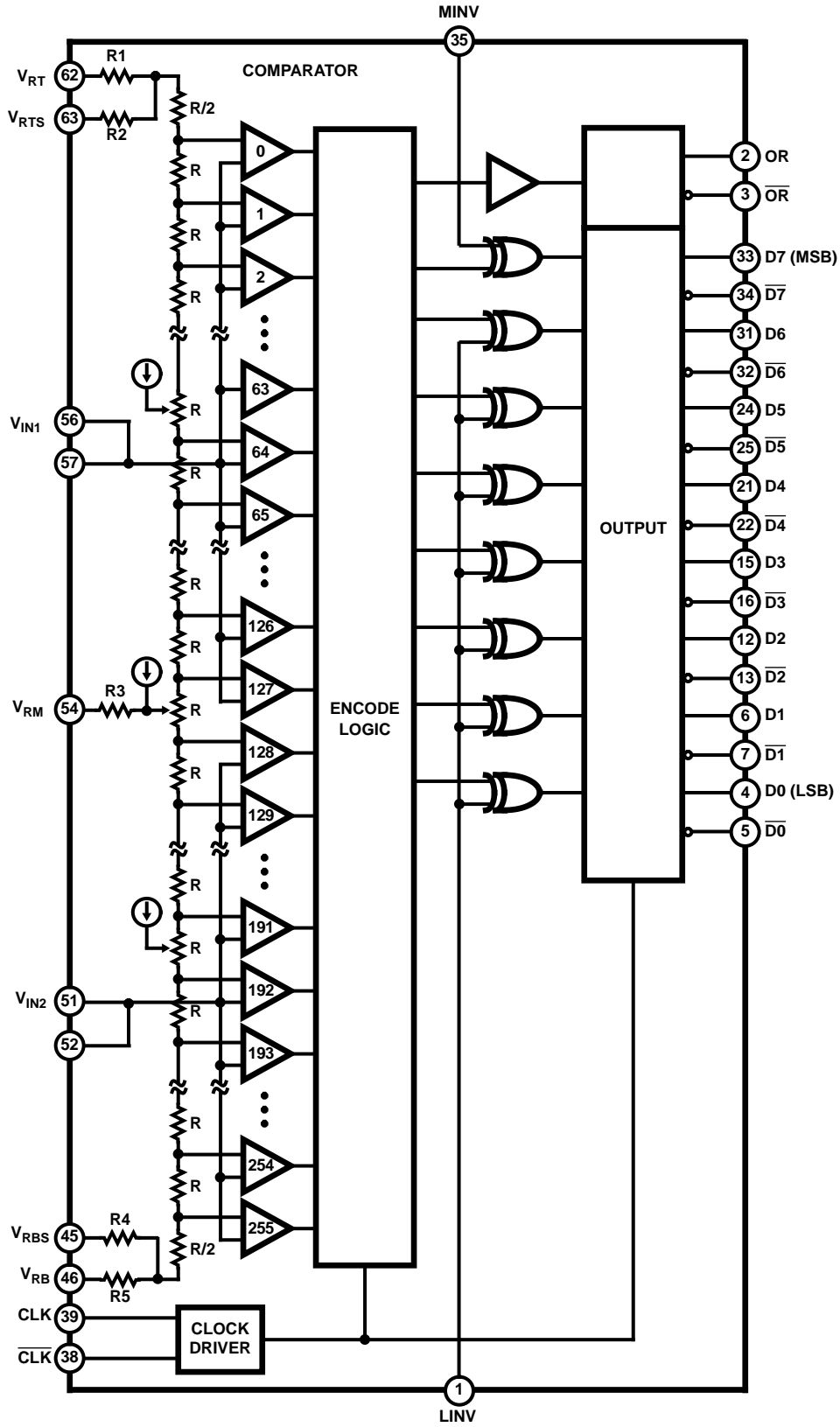
PART NUMBER	TEMPERATURE	PACKAGE
HI1276Y	+25°C	Die

• All performance parameters are for packaged devices when supplied by Harris.

Die Metallization Layer



Functional Block Diagram



Specifications HI1276Y

Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

Supply Voltage (V_{EE} , DV_{EE})	-7V to +0.5V	V_{RM} Pin Input Current (I_{VRM})	-3mA to +3mA
Analog Input Voltage (V_{IN})	-2.7 to +0.5V	Digital Output Current	(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, \overline{IOR})
Reference Input Voltage			-30mA to 0mA
V_{RT} , V_{RB} , V_{RM}	V_{EE} to +0.5V	Storage Temperature Range (T_{STG})	-65°C to +150°C
$ V_{RT} - V_{RB} $	2.5V		
Digital Input Voltage			
MINV, LINV	-4V to +0.5V		
CLK, \overline{CLK}	DV_{EE} to +0.5V		
$ CLK - \overline{CLK} $	2.7V		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage		Reference Input Voltage	
V_{EE} , DV_{EE}	-5.5V to -4.95V	V_{RT}	-0.1V to 0.1V
$V_{EE} - DV_{EE}$	-0.05V to 0.05V	V_{RB}	-2.2V to -1.8V
AGND - DGND	-0.05V to 0.05V	Analog Input Voltage, V_{IN}	V_{RB} to V_{RT}

Electrical Specifications $T_A = +25^\circ\text{C}$, DV_{EE} , $V_{EE} = -5.2\text{V}$, $V_{RT} = 0\text{V}$, $V_{RB} = -2\text{V}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Differential Linearity Error (DNL) (00000000 to 11111111)		-0.5	0.5	LSB
Integral Linearity Error (INL) (00000000 to 11111111)		-0.7	0.7	LSB
Resolution		8	-	Bits
Input Bias Current, I_{IN}	$V_{IN} = -1.0\text{V}$	50	830	μA
Analog Input Resistance, R_{IN}	$V_{IN} = -1.0\text{V}$	35	380	$\text{k}\Omega$
Resister-String Current, I_{REF}		-24	-16	mA
Reference Voltage, V_{RM}		-1.1	-0.9	V
Residual Resistance, R1		0.1	1.2	Ω
Residual Resistance, R5		0.1	1.2	Ω
Digital Input Current HI, I_{IH}	$H_i = -0.8\text{V}$	0	50	μA
Digital Input Current LO, I_{IL}	$L_o = -1.6\text{V}$	-30	30	μA
CLK Open Voltage, V_{OPN}	$\overline{CLK} = \text{Open}$	-1.45	-1.20	V
Leakage (1) D0 to D7, V_{LEAK}	$I = -10\mu\text{A}$	-1.0	-0.3	V
Leakage (2) D0 to D7, V_{IN} , LINV, MINV, CLK, \overline{CLK} , I_{LEAK}	$V = 0.3\text{V}$	-1.0	1.0	μA
Digital Output Voltage HI, V_{OH}	50Ω to -2V	-1	-0.6	V
Digital Output Voltage LO, V_{OL}	50Ω to -2V	-2	-1.6	V
Supply Current, I_{EE}		-640	-400	mA

Timing Diagram

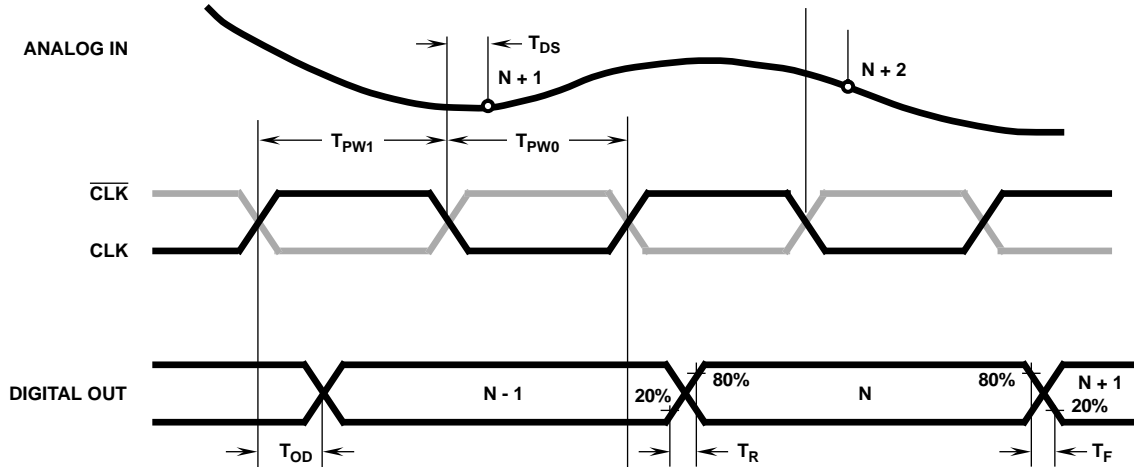


FIGURE 1.

Pad Descriptions

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	LINV	I	ECL		<p>Polarity selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.</p> <p>Polarity selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.</p>
35	MINV				
62	V _{RT}	I	0V		<p>Analog reference voltage (top) (0V typ.).</p>
63	V _{RTS}	O	0V		<p>Reference voltage sense (top).</p>
54	V _{RM}	I	V _{RB/2}		<p>Reference voltage mid point. Can be used for linearity compensation.</p>
45	V _{RBS}	O	-2V		<p>Reference voltage sense (bottom).</p>
46	V _{RB}	I	-2V		<p>Analog reference voltage (bottom).</p>

Pad Descriptions (Continued)

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
51, 52	V_{IN2}	I	V_{RTS} to V_{RBS}		Analog input. All of the pins must be wired externally.
39	CLK	I	ECL		CLK Input
38	$\overline{\text{CLK}}$				Complementary CLK input. Pulled down to -1.3V when left open.
33, 34	$D7, \overline{D7}$	O	ECL		MSB and complementary MSB data output.
31, 32	$D6, \overline{D6}$				D1 to D6: Data output D1 to D6: Complementary data output
24, 25	$D5, \overline{D5}$				
21, 22	$D4, \overline{D4}$				
15, 16	$D3, \overline{D3}$				
12, 13	$D2, \overline{D2}$				
6, 7	$D1, \overline{D1}$				LSB data complementary output LSB data output.
4, 5	$D0, \overline{D0}$				Overrange and complementary overrange output.
2, 3	OR, \overline{OR}				

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Pad Descriptions (Continued)

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
40, 41, 47, 48, 60, 61, 65, 66	AV _{EE}	-	-5.2V		Analog supply. Internally connected to DV _{EE} (resistance: 4Ω to 6Ω).
49, 50, 53, 55, 58, 59	AGND		0V		Analog ground.
8, 14, 23, 30	DV _{EE}		-5.2V		Digital supply. Internally connected to AV _{EE} (resistance: 4Ω to 6Ω).
9, 19, 20, 29	DGND1		0V		Digital ground.
10, 11, 17, 18, 27, 28	DGND2 (Note 1)		0V		Digital ground for output drive.
36, 37, 42, 43, 44, 64	NC				No connect pins. It is recommended to wire these pins to AGND.
45	NC			No connect pin. It is recommended to wire these pins to DGND.	

NOTE:

1. V_{RT} = V_{RTS} = 0V, V_{RM} = -1V or open, V_{RB} = V_{RBS} = -2V

A/D OUTPUT CODE TABLE

V _{IN} (NOTE 1)	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V	0	0	000 •••••00		0	100 •••••00		0	011 •••••11		0	111 •••••11	
		1	000 •••••00		1	100 •••••00		1	011 •••••11		1	111 •••••11	
		1	000 •••••01		1	100 •••••01		1	011 •••••10		1	111 •••••10	
			• • •			• • •			• • •			• • •	
-1V	127	1	011 •••••11		1	111 •••••11		1	000 •••••00		1	100 •••••00	
		128	100 •••••00		1	000 •••••00		1	111 •••••11		1	011 •••••11	
			• • •			• • •			• • •			• • •	
	254	1	111 •••••10		1	011 •••••10		1	100 •••••01		1	000 •••••01	
	255	1	111 •••••11		1	011 •••••11		1	100 •••••00		1	000 •••••00	
-2V	1	1	111 •••••11		1	011 •••••11		1	100 •••••00		1	000 •••••00	

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Pad Coordinates

PAD COORDINATE 1

PAD NO.	PAD NAME	X [μm]	Y [μm]
1	LINV	2198.40	4490.40
2	OR	2008.00	4490.40
3	$\overline{\text{OR}}$	1817.60	4490.40
4	D0	1627.20	4490.40
5	$\overline{\text{D0}}$	1436.80	4490.40
6	D1	1246.40	4490.40
7	$\overline{\text{D1}}$	1056.00	4490.40
8	DV _{EE}	865.60	4490.40
9	DGND1	675.20	4490.40
10	DGND2	388.80	4490.40
11	DGND2	209.60	4311.20
12	D2	209.60	3730.40
13	$\overline{\text{D2}}$	209.60	3540.00
14	DV _{EE}	209.60	3349.60
15	D3	209.60	3159.20
16	$\overline{\text{D3}}$	209.60	2968.80
17	DGND2	209.60	2778.40
18	DGND2	209.60	2629.60
19	DGND1	209.60	2458.40
20	DGND1	209.60	2301.60
21	D4	209.60	2111.20
22	$\overline{\text{D4}}$	209.60	1920.80

PAD NO.	PAD NAME	X [μm]	Y [μm]
23	DV _{EE}	209.60	1730.40
24	D5	209.60	1540.00
25	$\overline{\text{D5}}$	209.60	1349.60
26		209.60	1159.20
27	DGND2	209.60	588.00
28	DGND2	209.60	362.40
29	DGND1	484.80	215.20
30	DV _{EE}	675.20	215.20
31	D6	865.60	215.20
32	$\overline{\text{D6}}$	1056.00	215.20
33	D7	1246.40	215.20
34	$\overline{\text{D7}}$	1436.80	215.20
35	MINV	1627.20	215.20
36		1817.60	215.20
37		2008.00	215.20
38	$\overline{\text{CLK}}$	2198.40	215.20
39	CLK	2388.80	215.20
40	AV _{EE}	2579.20	215.20
41	AV _{EE}	2728.00	215.20
42		2974.40	215.20
43		3164.80	215.20
44		3355.20	215.20

PAD NO.	PAD NAME	X [μm]	Y [μm]
45	V _{RBS}	3545.60	215.20
46	V _{RB}	3736.00	215.20
47	AV _{EE}	3926.40	215.20
48	AV _{EE}	4075.20	215.20
49	AGND	4377.60	215.20
50	AGND	4377.60	1292.00
51	V _{IN2}	4377.60	1570.40
52	V _{IN2}	4377.60	1720.80
53	AGND	4377.60	1999.20
54	V _{RM}	4377.60	2352.80
55	AGND	4377.60	2698.40
56	V _{IN1}	4377.60	2984.80
57	V _{IN1}	4377.60	3135.20
58	AGND	4377.60	3413.60
59	AGND	4377.60	4490.40
60	AV _{EE}	4075.20	4490.40
61	AV _{EE}	3926.40	4490.40
62	V _{RT}	3736.00	4490.40
63	V _{RTS}	3545.60	4490.40
64		3164.80	4490.40
65	AV _{EE}	2728.00	4490.40
66	AV _{EE}	2579.20	4490.40

Pad Coordinates (Continued)

PAD COORDINATE 2

PAD NO.	PAD NAME	X [μm]	Y [μm]
1	LINV	2158.40	4450.40
2	OR	1968.00	4450.40
3	$\overline{\text{OR}}$	1777.60	4450.40
4	D0	1587.20	4450.40
5	$\overline{\text{D0}}$	1396.80	4450.40
6	D1	1206.40	4450.40
7	$\overline{\text{D1}}$	1016.00	4450.40
8	DV _{EE}	825.60	4450.40
9	DGND1	635.20	4450.40
10	DGND2	348.80	4450.40
11	DGND2	169.60	5271.20
12	D2	169.60	3690.40
13	$\overline{\text{D2}}$	169.60	3500.00
14	DV _{EE}	169.60	3309.60
15	D3	169.60	3119.20
16	$\overline{\text{D3}}$	169.60	2928.80
17	DGND2	169.60	2738.40
18	DGND2	169.60	2589.60
19	DGND1	169.60	2418.40
20	DGND1	169.60	2261.60
21	D4	169.60	2071.20
22	$\overline{\text{D4}}$	169.60	1880.80

PAD NO.	PAD NAME	X [μm]	Y [μm]
23	DV _{EE}	169.60	1690.40
24	D5	169.60	1500.00
25	$\overline{\text{D5}}$	169.60	1309.60
26		169.60	1119.20
27	DGND2	169.60	548.00
28	DGND2	169.60	322.40
29	DGND1	444.80	175.20
30	DV _{EE}	635.20	175.20
31	D6	825.60	175.20
32	$\overline{\text{D6}}$	1016.00	175.20
33	D7	1206.40	175.20
34	$\overline{\text{D7}}$	1396.80	175.20
35	MINV	1587.20	175.20
36		1777.60	175.20
37		1968.00	175.20
38	$\overline{\text{CLK}}$	2158.40	175.20
39	CLK	2348.80	175.20
40	AV _{EE}	2539.20	175.20
41	AV _{EE}	2688.00	175.20
42		2934.40	175.20
43		3124.80	175.20
44		3315.20	175.20

PAD NO.	PAD NAME	X [μm]	Y [μm]
45	V _{RBS}	3505.60	175.20
46	V _{RB}	3696.00	175.20
47	AV _{EE}	3886.40	175.20
48	AV _{EE}	4035.20	175.20
49	AGND	4337.60	175.20
50	AGND	4337.60	1252.00
51	V _{IN2}	4337.60	1530.40
52	V _{IN2}	4337.60	1680.80
53	AGND	4337.60	1959.20
54	V _{RM}	4337.60	2312.80
55	AGND	4337.60	2658.40
56	V _{IN1}	4337.60	2944.80
57	V _{IN1}	4337.60	3095.20
58	AGND	4337.60	3373.60
59	AGND	4337.60	4450.40
60	AV _{EE}	4035.20	4450.40
61	AV _{EE}	3886.40	4450.40
62	V _{RT}	3696.00	4450.40
63	V _{RTS}	3505.60	4450.40
64		3124.80	4450.40
65	AV _{EE}	2688.00	4450.40
66	AV _{EE}	2539.20	4450.40

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