HARRIS Semiconductor

NOT RECOMMENDED FOR NEW DESIGNS
See HI5805

HI5804

October 1998

12-Bit, 5 MSPS A/D Converter

Features

- **Sampling Rate . . . . . 5 MSPS**
- **Low Power**
- **Internal Sample and Hold**
- **Fully Differential Architecture**
- **Full Power Input Bandwidth 100MHz**
- **Low Distortion**
- **Internal Reference**
- **TTL/CMOS Compatible Digital I/O**
- **Digital Outputs . . . . . 3V to 5V**

Applications

- **High Speed Data Acquisition Systems**
- **Digital IF Communication Systems**
- **Document and Film Scanners**
- **Medical Imaging**
- **Radar Signal Analysis**
- **Vibration/Waveform Spectrum Analysis**
- **Digital Servo Loop Control**
- **Reference Literature**
  - **AN9214 Using Harris High Speed Converters**
  - **AN9647 Using the HI5804 Evaluation Board**

Description

The HI5804 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5804 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5804 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

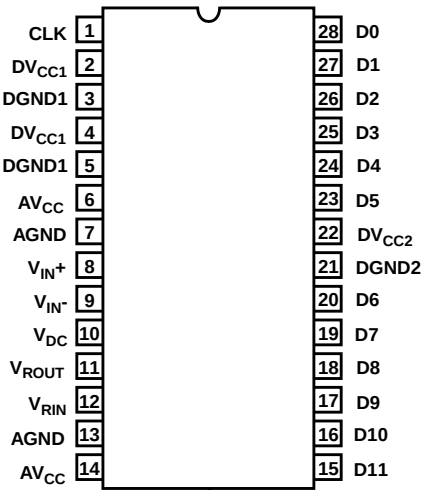
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI5804KCB	5 MSPS	0 to 70	28 Ld SOIC	M28.3
HI5804EVAL		25	Evaluation Board	

Pinout

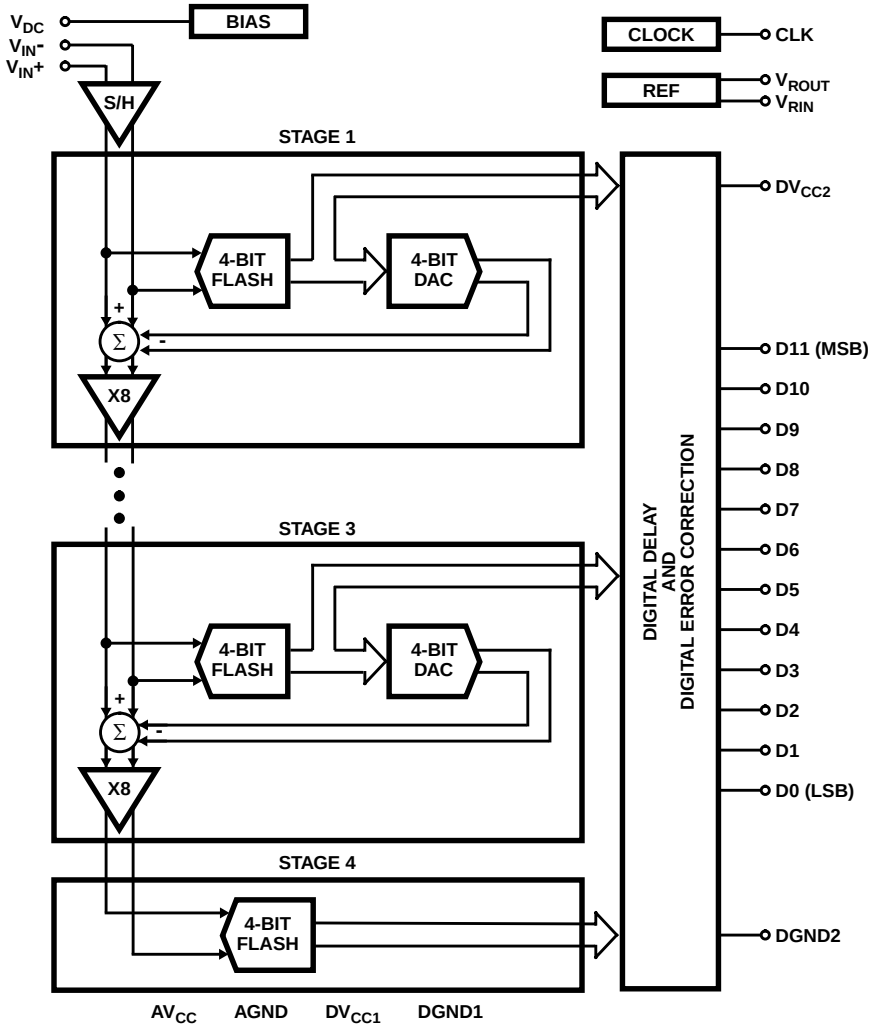
HI5804
(SOIC)
TOP VIEW



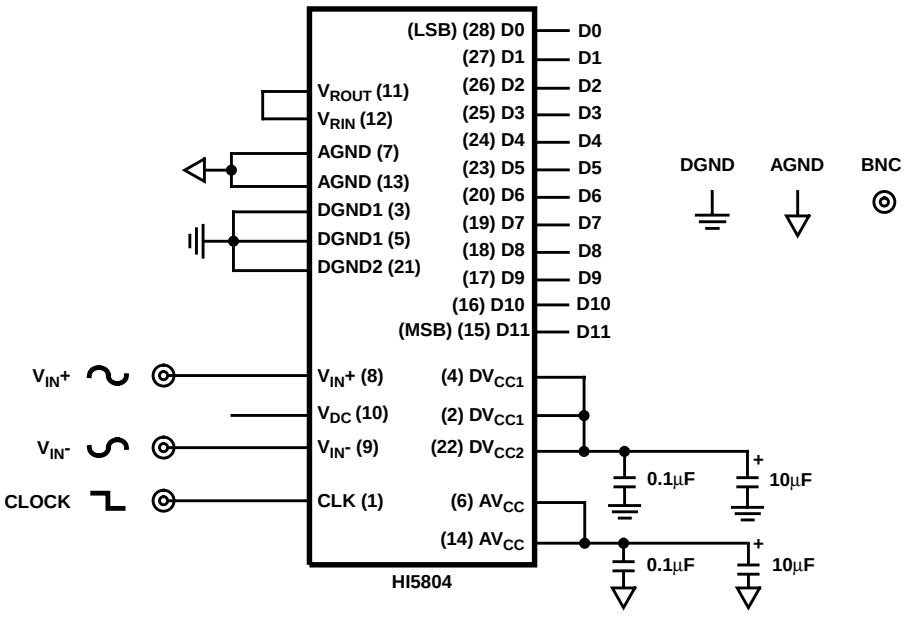
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4026.5**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . . D_{GND} to DV_{CC}
Analog I/O Pins. . . . . A_{GND} to AV_{CC}

Operating Conditions

Temperature Range, HI5804KCB . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
HI5804KCB	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±2	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	12	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	24	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes	-	5	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	10.3	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	64	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	65	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-70	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-73		dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-73	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	73	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-66	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±2.0	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	4.0	-	V
Analog Input Resistance, R_{IN}	(Notes 2, 3)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-		-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\ DIFF} = (I_B+ - I_B-)$		-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	100	-	MHz
Analog Input Common Mode Voltage ($V_{IN}+ + V_{IN}-$)/2	Differential Mode (Note 2)	1	2.3	4	V

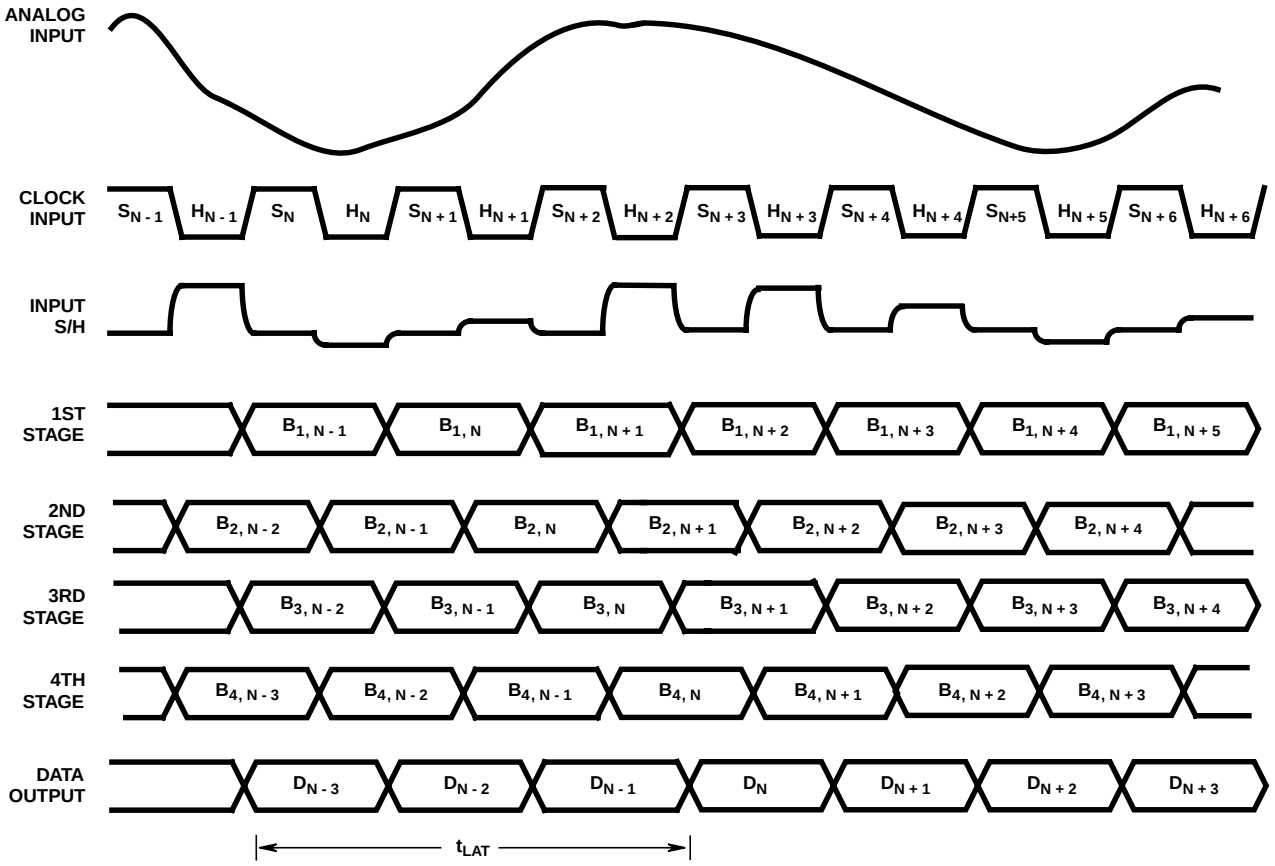
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT}		-	3.5	-	V
Reference Output Current		-	-	1	mA
REFERENCE INPUT					
Total Reference Resistance, R_L		-	7.8	-	kΩ
Reference Current		-	450	-	µA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current (Not to Exceed)		-	-	1	mA
DIGITAL INPUT, CLK					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{CLK} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{CLK} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS, D0-D11					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$ (Note 2)	1.6	-	-	mA
	$DV_{CC2} = 3.0V$, $V_O = 0.4V$	-	1.6	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$ (Note 2)	-0.2	-	-	mA
	$DV_{CC2} = 3.0V$, $V_O = 2.4V$	-	-0.2	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Hold, t_H		-	8	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	3	Cycle
Clock Pulse Width (Low)	5MHz Clock	90	100	110	ns
Clock Pulse width (High)	5MHz Clock	90	100	110	ns
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}		2.85	-	5.25	V
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	60	-	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	46	-	mA
Digital Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = 2V$	-	13	-	mA
Digital Output Supply Current, DI_{CC2}	$V_{IN}+ - V_{IN}- = 2V$	-	1	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = 2V$	-	300	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±16	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±16	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5804 INTERNAL CIRCUIT TIMING

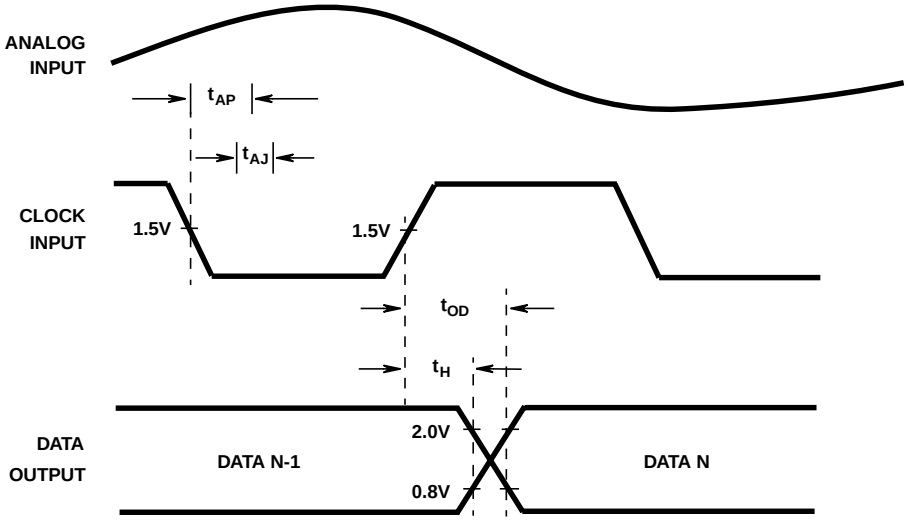


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

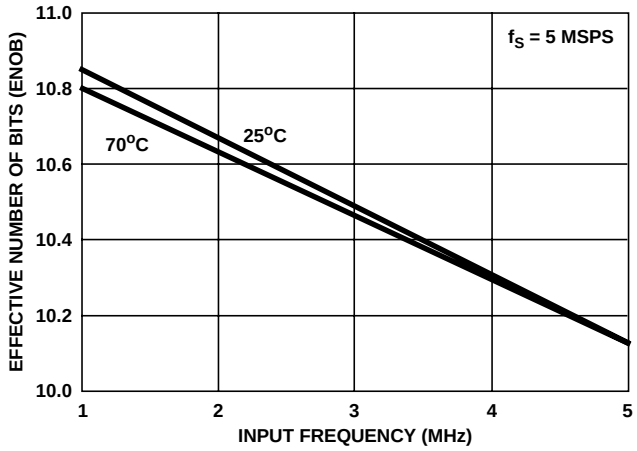


FIGURE 3. TYPICAL ENOB vs INPUT FREQUENCY

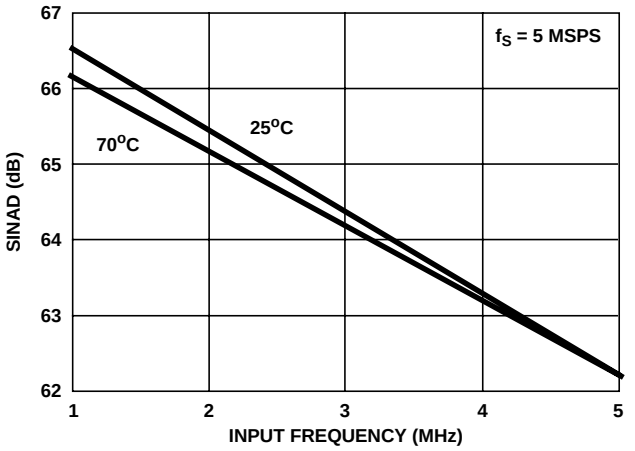


FIGURE 4. TYPICAL SINAD vs INPUT FREQUENCY

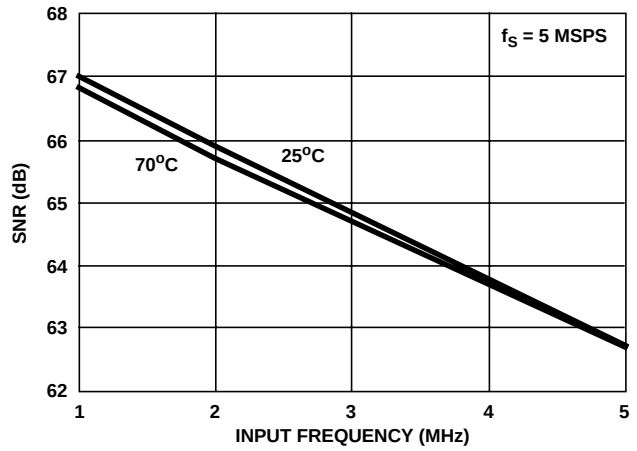


FIGURE 5. TYPICAL SNR vs INPUT FREQUENCY

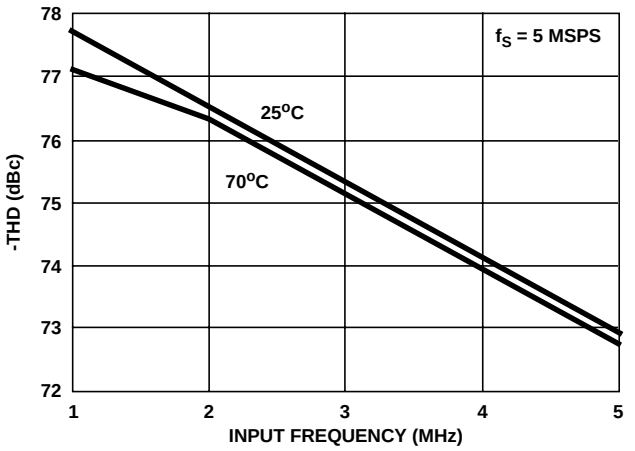


FIGURE 6. TYPICAL -THD vs INPUT FREQUENCY

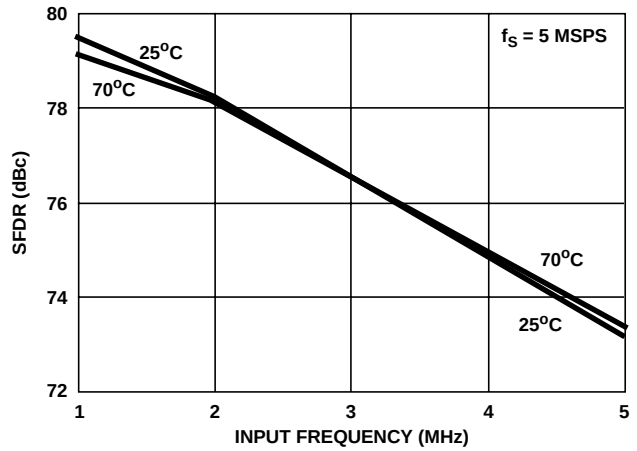


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

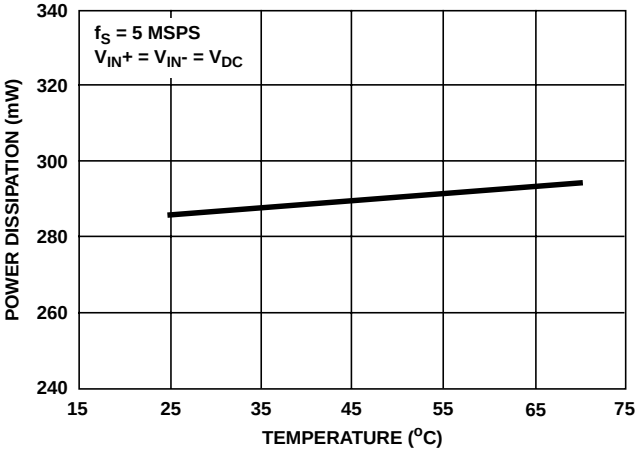


FIGURE 8. TYPICAL POWER DISSIPATION vs TEMPERATURE

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	CLK	Sample Clock Input.
2	DV_{CC1}	Digital Supply (+5.0V).
3	DGND1	Digital Ground.
4	DV_{CC1}	Digital Supply (+5.0V).
5	DGND1	Digital Ground.
6	AV_{CC}	Analog Supply (+5.0V).
7	AGND	Analog Ground.
8	V_{IN}+	Positive Analog Input.
9	V_{IN}-	Negative Analog Input.
10	V_{DC}	DC Bias Voltage Output.
11	V_{ROUT}	Reference Voltage Output.
12	V_{RIN}	Reference Voltage Input.
13	AGND	Analog Ground.
14	AV_{CC}	Analog Supply (+5.0V).
15	D11	Data Bit 11 Output (MSB).
16	D10	Data Bit 10 Output.
17	D9	Data Bit 9 Output.
18	D8	Data Bit 8 Output.
19	D7	Data Bit 7 Output.
20	D6	Data Bit 6 Output.
21	DGND2	Digital Output Ground.
22	DV_{CC2}	Digital Output Supply (+3.0V to +5.0V).
23	D5	Data Bit 5 Output.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5804 is a 12-bit, fully-differential, sampling pipeline A/D converter with digital error correction. Figure 9 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

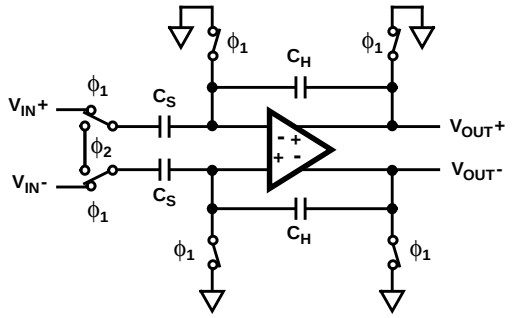


FIGURE 9. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a four bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal with the result that alternate stages in the pipeline will perform the same operation.

The 4-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final twelve bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 3rd cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a latch. The digital outputs are in offset binary format (See Table 1).

Internal Reference Generator, V_{ROUT} and V_{RIN}

The HI5804 has an internal reference voltage generator, therefore no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

The HI5804 can be used with an external reference voltage. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5804 is tested with V_{RIN} equal to 3.5V. Internal to the converter two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of ±2V.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input to the HI5804 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 10) will give the best performance for the converter.

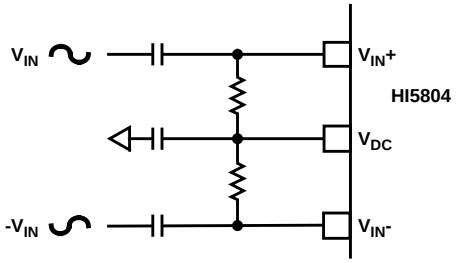


FIGURE 10. AC COUPLED DIFFERENTIAL INPUT

Since the HI5804 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature.

The difference between the converter's two internal voltage references is 2V. For the AC coupled differential input, (Figure 10), if V_{IN} is a $2V_{P-P}$ sinewave with $-V_{IN}$ being 180 degrees out of phase with V_{IN}, the converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 1V and the $V_{IN}-$ input is at V_{DC} - 1V ($V_{IN}+ - V_{IN}- = 2V$). Conversely, the ADC will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 1V and $V_{IN}-$ is at V_{DC} + 1V ($V_{IN}+ - V_{IN}- = -2V$).

Analog Input, Single-Ended Connection

The configuration shown in Figure 11 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND.

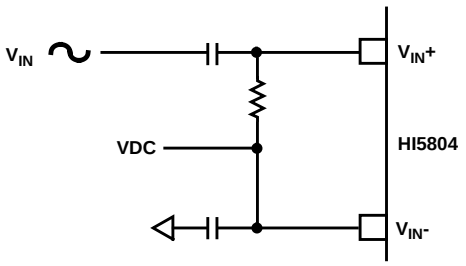


FIGURE 11. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave, then $V_{IN}+$ is a $4V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 2V ($V_{IN}+ - V_{IN}- = 2V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 2V ($V_{IN}+ - V_{IN}- = -2V$). In this case, VDC could range between 2V and 3V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} bias voltage output of the HI5804.

A single ended source will give better overall system performance if it is first converted to differential before driving the analog input of the HI5804.

Digital I/O and Clock Requirements

The HI5804 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5804 to be driven by CMOS logic.

The digital CMOS outputs have a separate digital supply. This allows the digital outputs to operate from a 3.0V to 5.0V supply. When driving CMOS logic, the digital outputs will swing to the rails. When driving standard TTL loads, the digital outputs will meet standard TTL level requirements even with a 3.0V supply.

In order to ensure rated performance of the HI5804, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5804 will only be guaranteed at conversion rates above 0.5 MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5804 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5804 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to Application Note AN9214, "Using Harris High Speed A/D Converters" for additional considerations when using high speed converters.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE† (USING INTERNAL REFERENCE)	OFFSET BINARY OUTPUT CODE											
		MSB											LSB
		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	+1.99976V	1	1	1	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	1.99878V	1	1	1	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.4µV	1	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.1µV	0	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-1.99829V	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-1.99927V	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each offset binary output code.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5804. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02$$

where: $V_{CORR} = 0.5dB$

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured distortion terms to the signal is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Overvoltage Recovery

Overvoltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the difference between the two internal voltage references. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture Jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

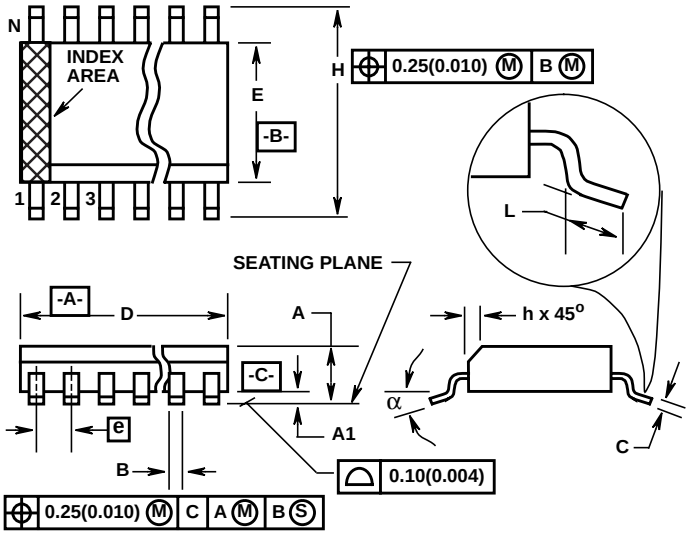
Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus after the third cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 3 clock cycles.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.