HI3086

August 1997

6-Bit, 140 MSPS, Flash A/D Converter

Features

- **Differential Linearity Error . . . . . ±0.2 LSB**
- **Integral Linearity Error . . . . . ±0.2 LSB**
- **Single +5V Power Supply Operation Available**
- **Low Input Capacitance 7pF**
- **Wide Analog Input Bandwidth 200MHz**
- **Low Power Consumption 360mW**
- **CLK/2 Clock Output Pin**
- **Excellent Temperature Characteristics**
- **1:2 Demultiplexed Output**
- **Internal $^1/_2$ Frequency Divider Circuit (With Reset Function)**
- **Compatible with ECL, PECL and TTL Digital Input Levels**
- **Direct Replacement for Sony CXA3086**

Applications

- **RGB Graphics Processing (LCD, PDP)**
- **Digital Communications (QPSK, QAM)**
- **Magnetic Recording (PRML)**

Description

The HI3086 is a 6-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 140 MSPS encode rate capability and full-power analog bandwidth of 200MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3086's clock input interfaces directly to TTL, ECL, or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single-channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at $^1/_2$ the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 140 MSPS conversion rate.

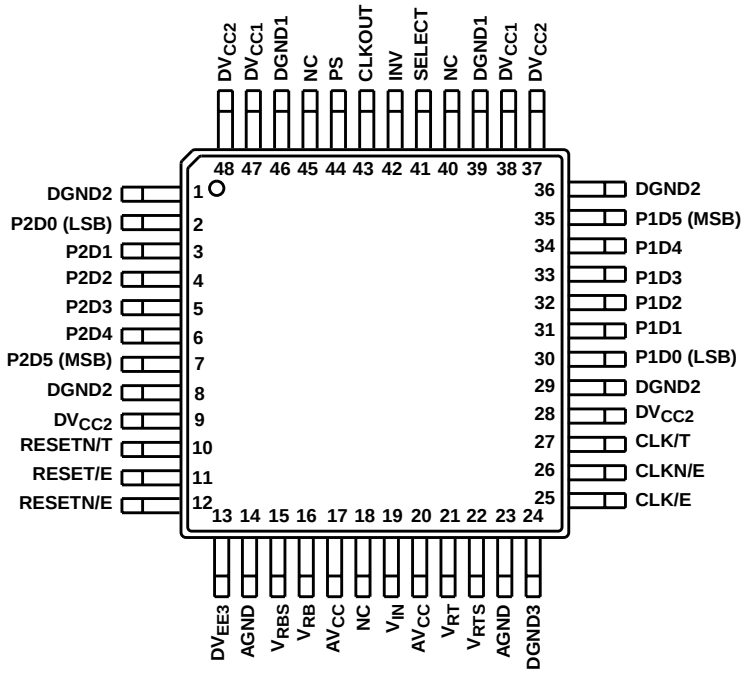
Fabricated with an advanced bipolar process, the HI3086 is provided in a space-saving 48-lead MQFP surface mount plastic package and is specified over the -20^{o}C to 75^{o}C temperature range.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3086JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S
HI3086EVAL	25	Evaluation Board	

Pinout

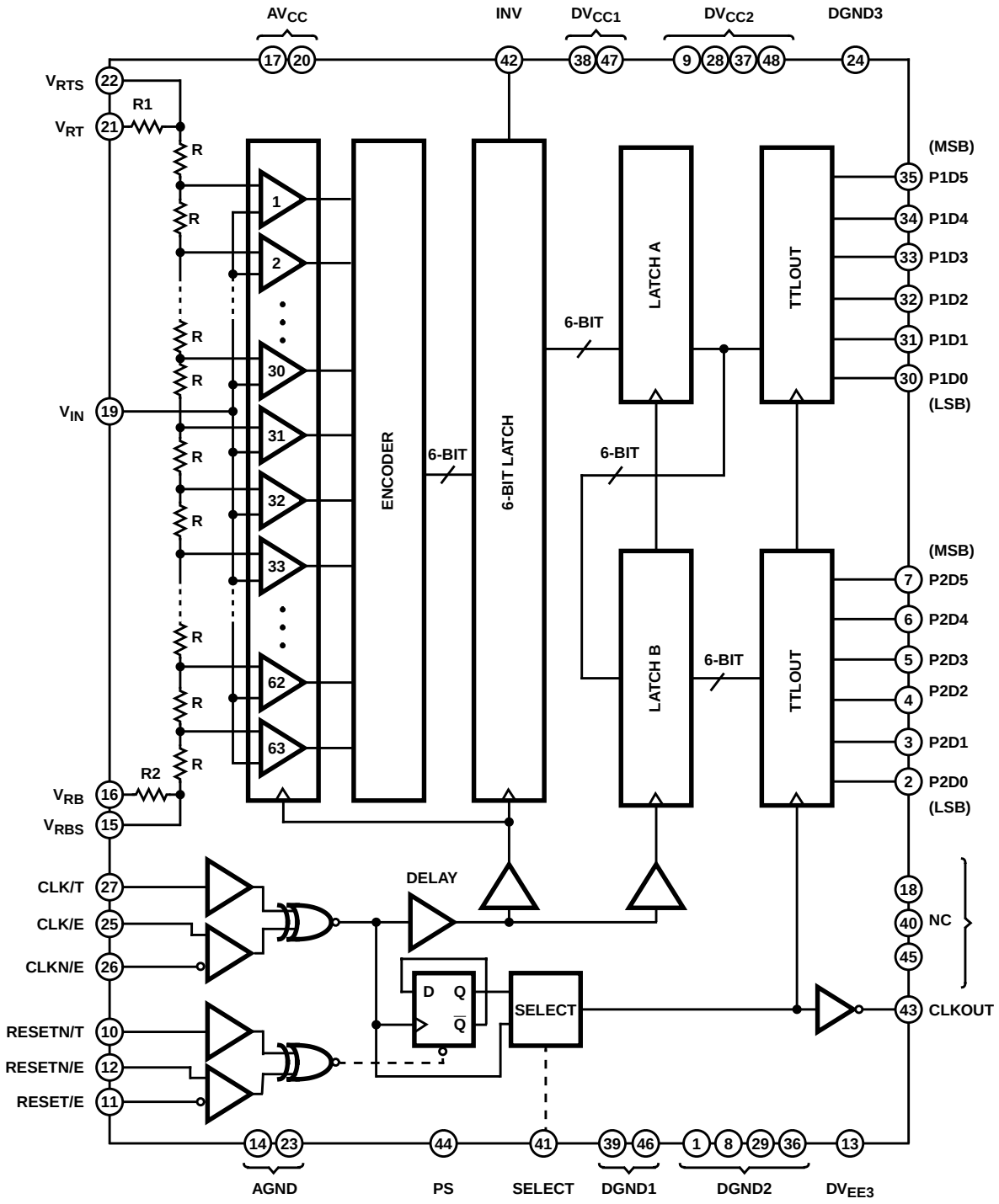
HI3086 (MQFP)
TOP VIEW



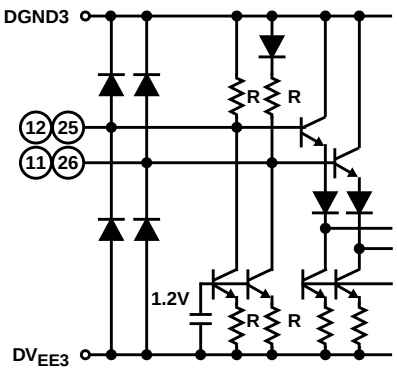
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **4110.1**

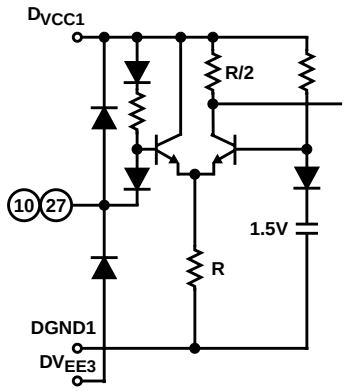
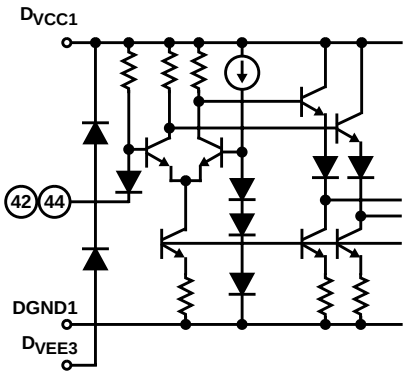
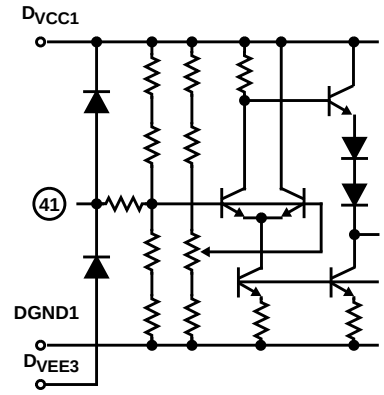
Functional Block Diagram



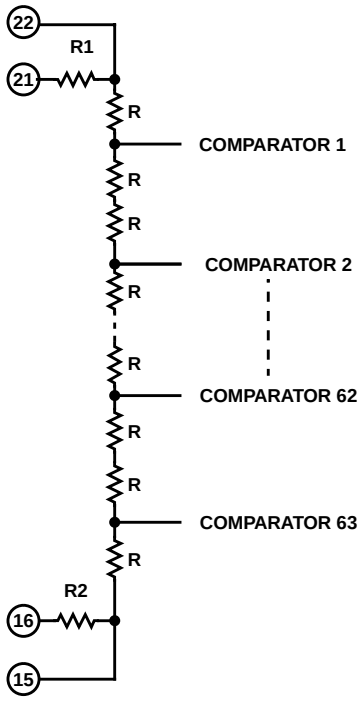
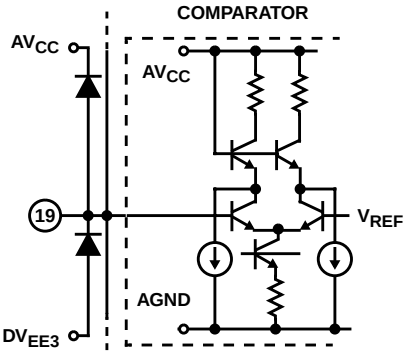
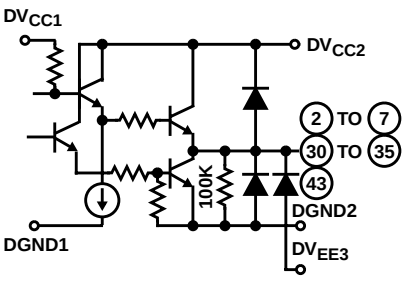
Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
14, 23	AGND		GND		Analog Ground. Separated from the digital ground.
17, 20	AV_{CC}		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
1, 8, 29, 36, 39, 46	DGND1 DGND2		GND		Digital Ground.
9, 28, 37, 38, 47, 48	DV_{CC1} DV_{CC2}		+5V (Typ)		Digital Power Supply.
24	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. +5V for PECL and TTL input.
13	D_{VEE3}		GND (With a Single Power Supply) -5V (Typ) (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. -5V for PECL and TTL input.
18, 40, 45	NC				No Connect pin. Not connected with the internal circuits.
25	CLK/E	I	ECL/PECL		Clock input.
26	CLKN/E	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
12	RESETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
11	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
27	CLK/T	I	TTL		Clock Input.
10	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
42	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1; I/O Correspondence Table).
44	PS	I	TTL		Power Saving Input. When the input is set to low level, the power saving mode is set. In this time the all TTL ouputs go into the high impedance state. Normally, set to high level or left open.
41	SELECT		V_{CC} or GND		Data Output Mode Selection. (See Table 2, Operating Mode Table).

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
22	V_{RTS}	O	+4.0V (Typ)		Reference Voltage Sense. Bypass to AGND with a 0.1µF chip capacitor.
21	V_{RT}	I	V_{RTS} + R1 x I_{REF}		Top Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and 0.1µF chip capacitor.
16	V_{RB}	I	V_{RBS} -R2 x I_{REF}		Bottom Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
15	V_{RBS}	O	+2.0V (Typ)		Reference Voltage Sense. Bypass to AGND with a 0.1µF chip capacitor.
19	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
30 to 35	P1D0 to P1D5	O	TTL		Port 1 Side Data Output.
2 to 7	P2D0 to P2D5	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2. Operating Mode Table.)

Absolute Maximum Ratings ($T_A = 25^oC$)

Supply Voltage . . . . . (AV_{CC}, DV_{CC1}, DV_{CC2}) -0.5V to 7.0V
($DGND3$) . . . . . -0.5V to 7.0V
(DV_{EE3}) . . . . . -7.0V to 0.5V
($DGND3 - DV_{EE3}$) . . . . . -0.5V to 7.0V
Analog Input Voltage (V_{IN}) . . . . . V_{RT} - 2.7V to AV_{CC}
Reference Input Voltage (V_{RT}) . . . . . 2.7V to AV_{CC}
(V_{RB}) . . . . . V_{IN} - 2.7V to AV_{CC}
($|V_{RT} - V_{RB}|$) 2.5V
Digital Input Voltage
ECL (***/E (Note 2)) . . . . . DV_{EE3} to 0.5V
PECL (***/E) . . . . . -0.5V to DGND3
TTL (***/T, INV P_S) . . . . . -0.5V to DV_{CC1}
Other (SELECT) . . . . . -0.5V to DV_{CC1}
V_{ID} (|***/E - ***N/E| (Note 3)) 2.7V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	63

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V
DV_{EE3}	-0.05	0	+0.05V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 0.5V
PECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV, PS) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode) Units = MSPS	100	-	-
Max Conversion Rate (f_C, DMUX Mode) Units = MSPS	140	-	-
Ambient Temperature (T_A)	-20^oC to 75^oC		

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	-0.05	0	+0.05V
DV_{EE3}	-5.5	-5.0	-4.75V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH} DGND3	DGND3 - 1.05		DGND3 - 0.5V
ECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode) Units = MSPS	100	-	-
Max Conversion Rate (f_C, DMUX Mode) Units = MSPS	140	-	-
Ambient Temperature (T_A)	-20^oC to 75^oC		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. ***/E and ***T indicate CLK/E and CLK/T, etc. for the pin name.
3. V_{ID}: Input Voltage Differential.

Electrical Specifications

$DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$, PECL Input

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			-	6	-	Bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	$V_{IN} = 2V_{P-P}$, f_C = 5 MSPS	-	-	±0.2	LSB
Differential Linearity Error	E_{DL}		-	-	±0.2	LSB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$, PECL Input **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	V_{IN} = +3.0V + 0.07V_{RMS}	-	7	-	pF
Analog Input Resistance	R_{IN}		16	-	150	kΩ
Analog Input Current	I_{IN}		0	-	125	µA
REFERENCE INPUT						
Reference Resistance (Note 5)	R_{REF}		160	225	308	Ω
Reference Current (Note 6)	I_{REF}		6.5	9.0	12.5	mA
Residual Resistance	R1		3.0	4.2	5.7	Ω
	R2		3.0	4.2	5.7	Ω
DIGITAL INPUT (ECL, PECL)						
Digital Input Voltage: High	V_{IH}		DGND3 -1.05	-	DGND3 -0.5	V
Digital Input Voltage: Low	V_{IL}		DGND3 -3.2	-	DGND3-1.4	V
Threshold Voltage	V_{TH}		-	DGND3 -1.2	-	V
Digital Input Current: High	I_{IH}	V_{IH} = DGND3 -0.8V	-50	-	+50	µA
Digital Input Current: Low	I_{IL}	V_{IL} = DGND3 -1.6V	-75	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL INPUT (TTL)						
Digital Input Voltage: High	V_{IH}		2.0	-	-	V
Digital Input Voltage: Low	V_{IL}		-	-	0.8	V
Threshold Voltage	V_{TH}		-	1.5	-	V
Digital Input Current: High	I_{IH}	V_{IH} = 3.5V	-50	-	0	µA
Digital Input Current: Low	I_{IL}	V_{IL} = 0.2V	-500	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL OUTPUT (TTL)						
Digital Output Voltage: High	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Digital Output Voltage: Low	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
Leakage Current	I_{OZ}	Power Saving Mode	-15	-	70	µA
SWITCHING CHARACTERISTICS						
Maximum Conversion Rate	f_C	DMUX Mode	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps
Sampling Delay	t_{DS}		3	4.5	6	ns
Clock High Pulse Width	t_{PW1}	CLK	2.9	-	-	ns
Clock Low Pulse Width	t_{PW0}	CLK	2.9	-	-	ns
Reset Signal Setup	t_{RS}	RESETN - CLK	3.5	-	-	ns
RESET Signal Hold	t_{RH}	RESETN - CLK	0	-	-	ns
CLKOUT Output Delay	t_{DCLK}	(C_L = 5pF)	3.5	7	9	ns
Data Output Delay (Note 7)	t_{DO1}	DMUX Mode (C_L = 5pF)	t (Note 6)	t + 1	t + 2	ns
	t_{DO2}	(C_L = 5pF)	4.5	8	10	ns
Output Rise Time	t_r	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
Output Fall Time	t_f	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$, PECL Input **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Input Bandwidth		$V_{IN} = 2V_{P-P}$, -3dB	200	-	-	MHz
S/N Ratio		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode	-	37.0	-	dB
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode	-	34.5	-	dB
Error Rate		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode Error > 4 LSB	-	-	10^{-12}	TPS (Note 8)
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode Error > 4 LSB	-	-	10^{-9}	TPS
		f_C = 100 MSPS, f_{IN} = 24.999MHz Full Scale, Straight Mode Error > 4 LSB	-	-	10^{-9}	TSP
POWER SUPPLY						
Supply Current	I_{CC}		54.0	67.5	90.0	mA
Supply Current	I_{EE}		0.4	0.6	0.8	mA
Power Consumption (Note 9)	P_D		290	360	470	mW
Supply Current	$I_{CC} + I_{EE}$	Power Saving Mode	2.0	-	8.0	mA
Power Consumption	P_D	Power Saving Mode	28.0	-	58.0	mW

NOTES:

4. R_{REF}: Resistance value between V_{RT} and V_{RB}.

5. $I_{REF} = \frac{V_{RT} - V_{RB}}{R_{REF}}$.

6. $t = \frac{1}{f_C}$.

7. TPS: Times Per Sample.

8. $P_D = (I_{CC} + I_{EE}) \bullet V_{CC} + \frac{(V_{RT} - V_{RB})^2}{V_{REF}}$.

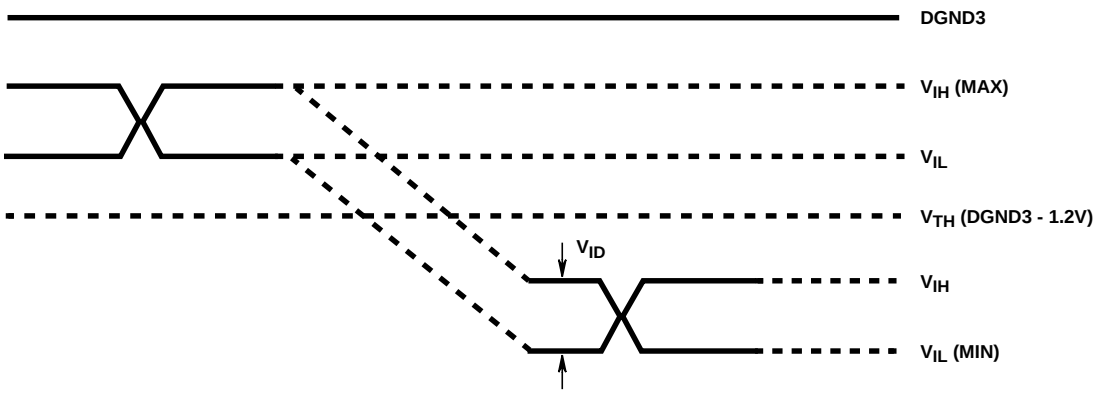


FIGURE 1. ECL AND PECL SWITCHING LEVEL

TABLE 1. I/O CORRESPONDENCE

V_{IN}	STEP	INV 1 D5	D4	D3	D2	D1	D0	INV 0 D5	D4	D3	D2	D1	D0
V_{RTS}	63	1	1	1	1	1	1	0	0	0	0	0	0
	62	1	1	1	1	1	0	0	0	0	0	0	1
	•			•						•			
	•			•						•			
	•			•						•			
	32	1	0	0	0	0	0	0	1	1	1	1	1
	31	0	1	1	1	1	1	1	0	0	0	0	0
	•			•						•			
	•			•						•			
	•			•						•			
	1	0	0	0	0	0	1	1	1	1	1	1	0
V_{RBS}	0	0	0	0	0	0	0	1	1	1	1	1	1

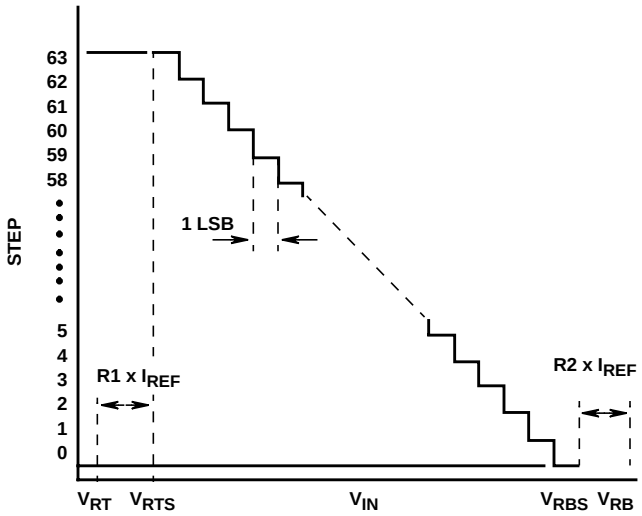


FIGURE 2.

Test Circuits

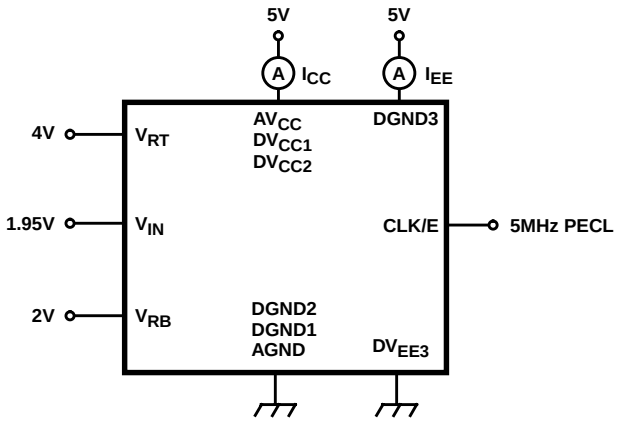


FIGURE 3. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

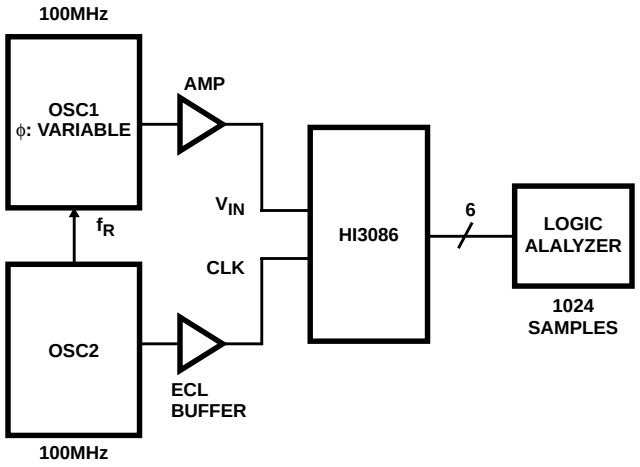


FIGURE 4. SAMPLING DELAY MEASUREMENT CIRCUIT APERTURE JITTER MEASUREMENT CIRCUIT

Test Circuits (Continued)

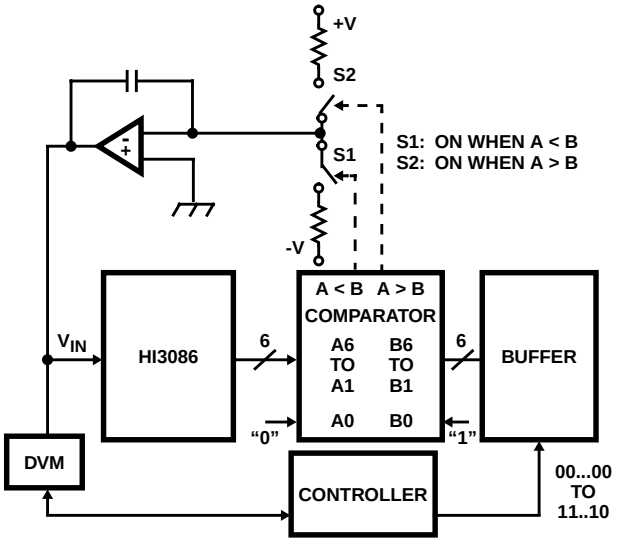
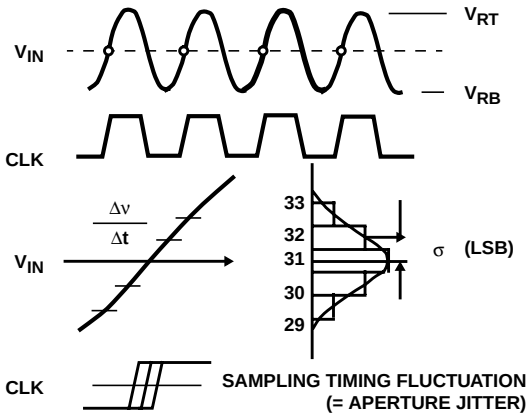


FIGURE 5. INTEGRAL LINEARITY ERROR MEASUREMENT CIRCUIT DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT



NOTE: Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter Tai is:

$$t_{AJ} = \sigma / \frac{\Delta \upsilon}{\Delta T} = \sigma / \left(\frac{64}{2} \times 2\pi f\right).$$

FIGURE 6. APERTURE JITTER MEASUREMENT METHOD

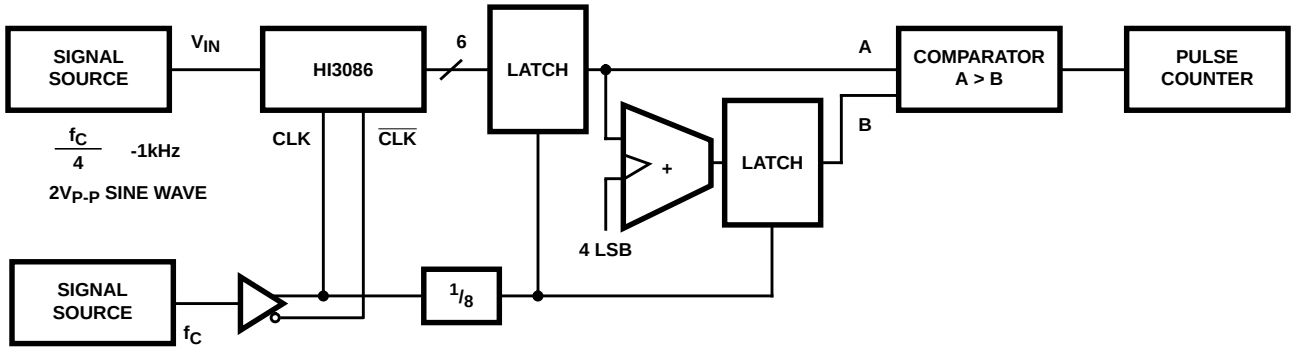


FIGURE 7. ERROR RATE MEASUREMENT CIRCUIT

Operating Modes

The HI3086 has two types of operating modes which are selected with Pin 41 (SELECT).

TABLE 2. OPERATING MODE

OPERATING MODE	SELECT	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V_{CC}	140 Mbps	Demultiplexed Output 70 Mbps	The input clock is $^1/_2$ frequency divided and output at 70MHz.
Straight Mode	GND	100 Mbps	Straight Output 100 Mbps	The input clock is inverted and output at 100MHz.

Demux Mode (See Figures 19, 20, 21).

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this $^1/_2$ frequency divided clock. The $^1/_2$ frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3086 units in parallel in this mode, differences in the start timing of the $^1/_2$ frequency divided clock may cause operation as shown in Figures 8 and 9. As a countermeasure, the HI3086 is equipped with a function which resets the $^1/_2$ frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at f_C (Min) = 140 MSPS in this mode.

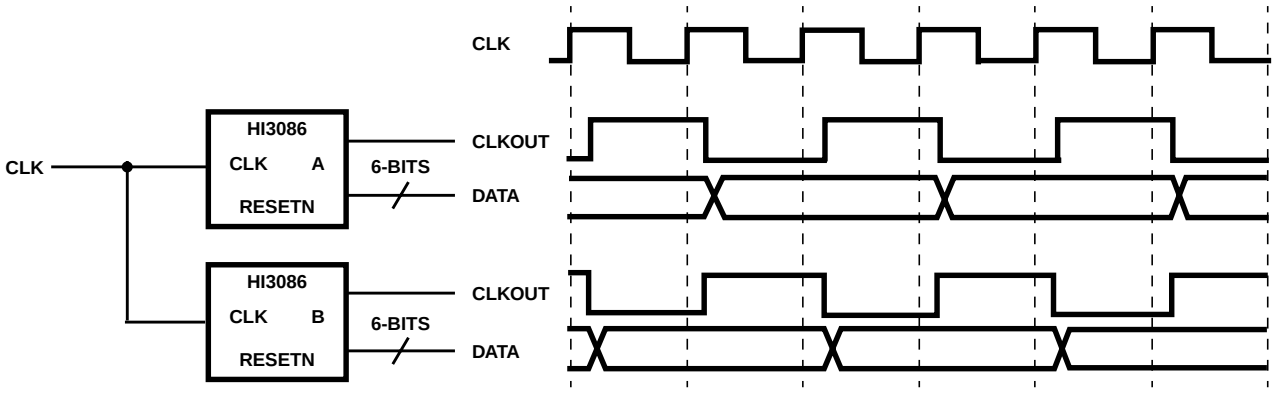


FIGURE 8. WHEN THE RESET PULSE IS NOT USED

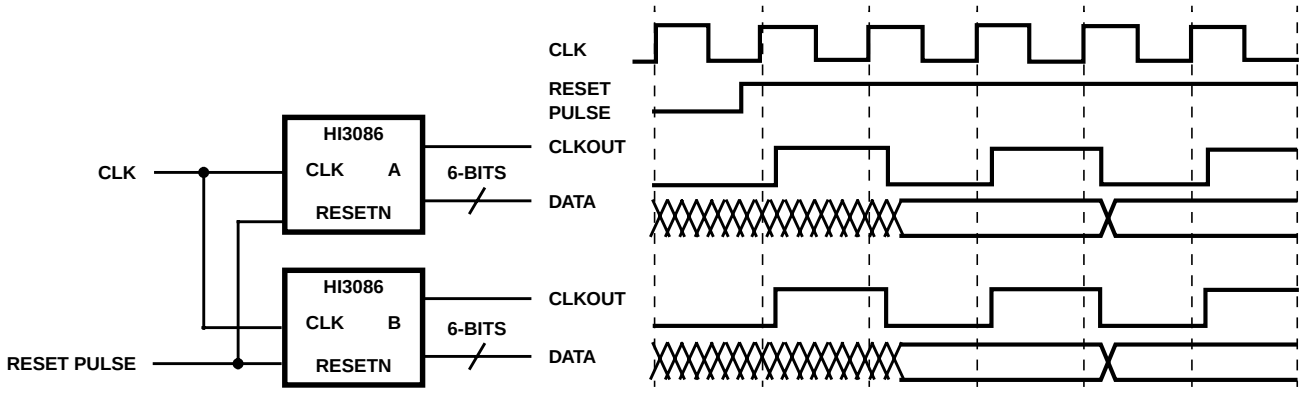


FIGURE 9. WHEN THE RESET PULSE IS USED

Straight Mode (See Figures 22, 23, 24 and 25).

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at f_C (Min) = 100 MSPS in this mode.

Digital Input Level and Supply Voltage Settings

The logic input level for the HI3086 supports ECL, PECL and TTL levels. The power supplies (D_{VEE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	D_{VEE3}	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS
ECL	-5V	0V	±5V	Figures 19, 22
PECL	0V	+5V	+5V	Figures 20, 23
TTL	0V	+5V	+5V	Figures 21, 24, 25

Timing Waveforms

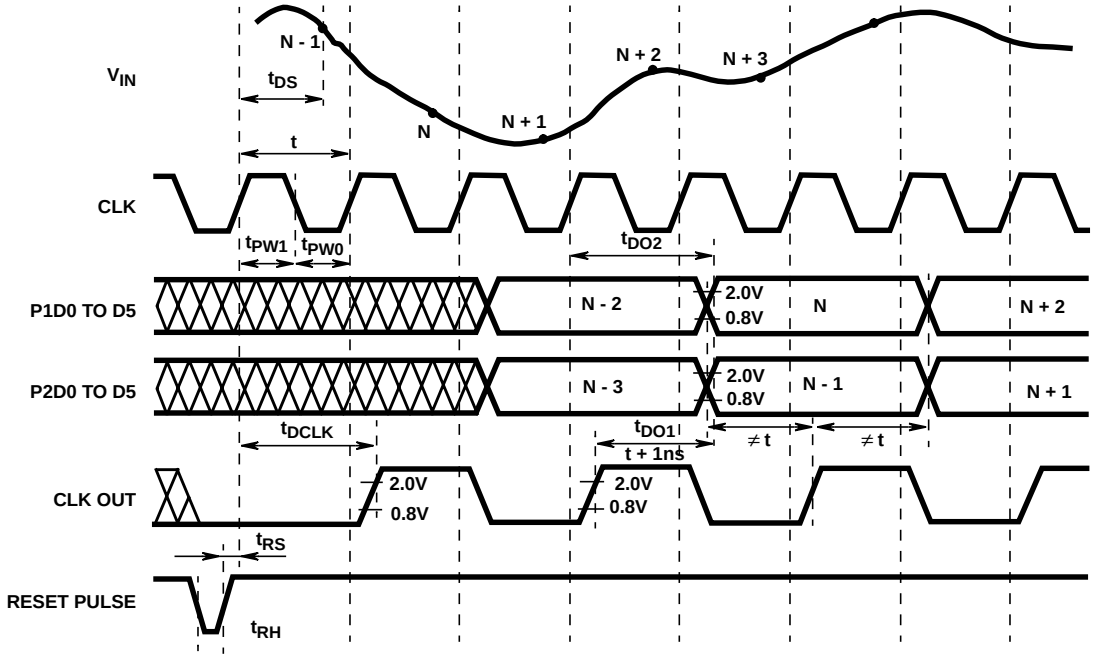


FIGURE 10. DEMUX MODE TIMING CHART (SELECT = V_{CC})

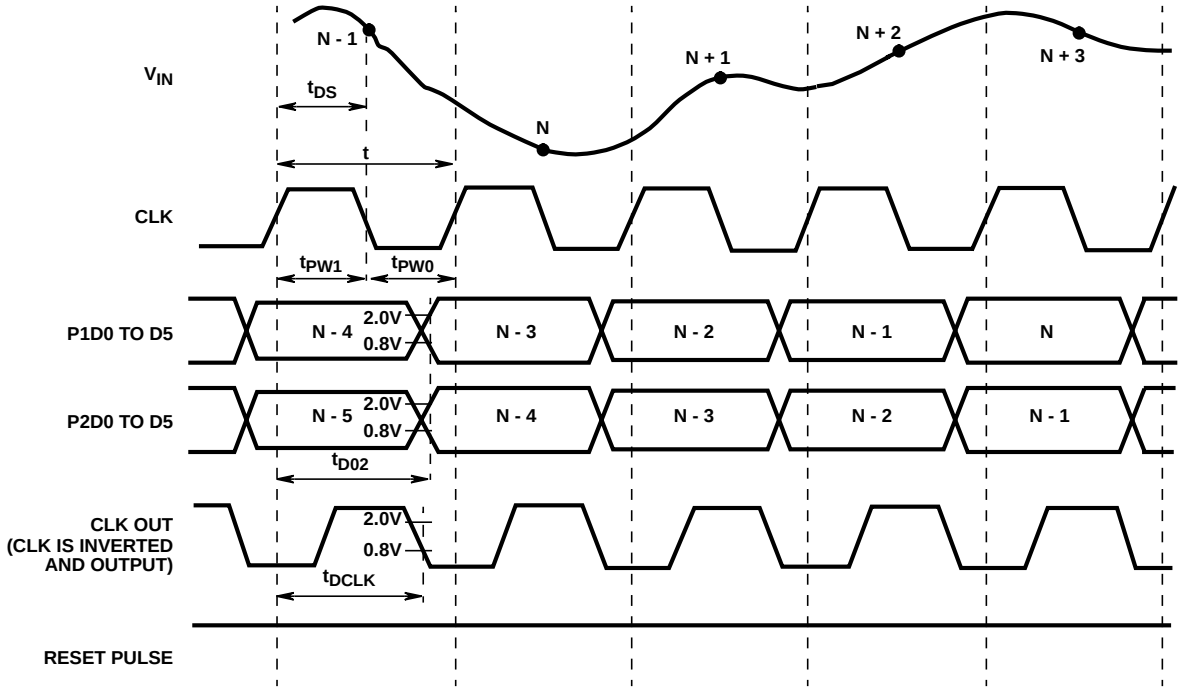


FIGURE 11. STRAIGHT MODE TIMING CHART (SELECT = GND)

Notes on Operation

- The HI3086 is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Ground the power supply pins (AV_{CC}, DV_{CC1}, DV_{CC2}, DVEE3) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AVCC pin to the AGND pattern and the DV_{CC1}, DV_{CC2}, DV_{EE3} pins to the DGND pattern.)
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 7pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit; keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1µF tantal capacitor and, 0.1µF chip capacitor as short as possible.
- The offset for residual is generated each for the reference voltage pins V_{RT} and V_{RB}. When the offset voltage has no influence on the IC operation, the voltage should be applied to the V_{RT} and V_{RB} pins directly, keeping the V_{RBS} pin open. When the reference voltage is to be supplied to these pins precisely, form the feedback loop circuit with V_{RT} and V_{RB} as a force pin and adjust the offset voltage to be 0V. See Figure 25 for details.
- If the CLKN/E pin is not used, bypass this pin to DGND with an approximately 0.1µF capacitor. At this time, approximately DGND3 -1.2V voltage is generated. However, this is not recommended for use as threshold voltage V_{BB} as it is too weak.
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and ***/E pins left open.

Typical Performance Curves

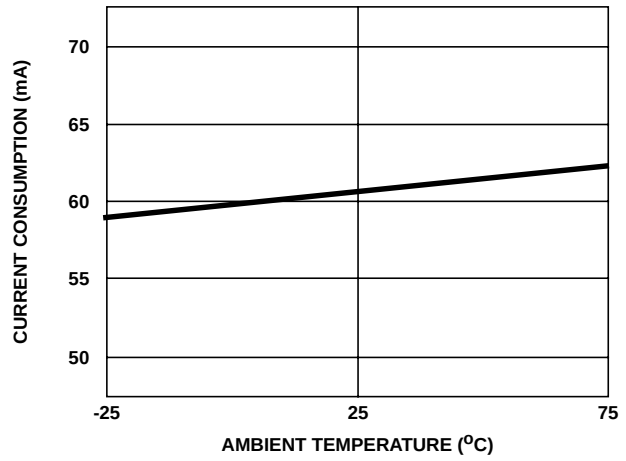


FIGURE 12. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

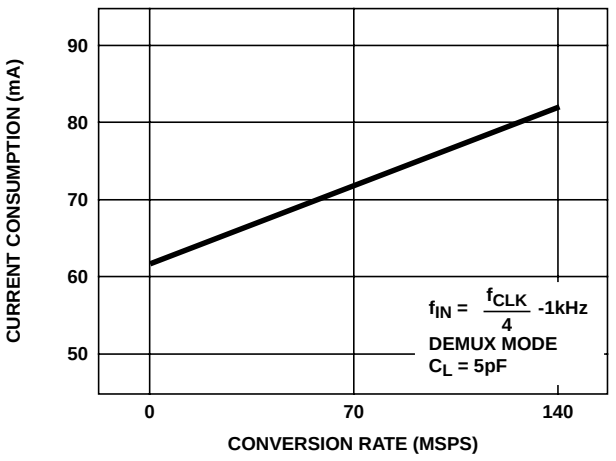


FIGURE 13. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS

Typical Performance Curves (Continued)

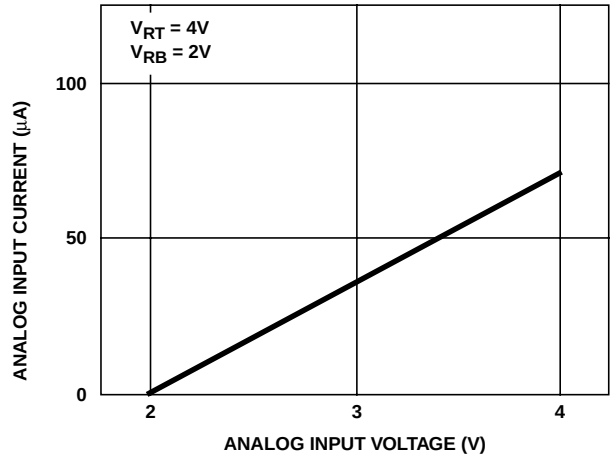


FIGURE 14. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

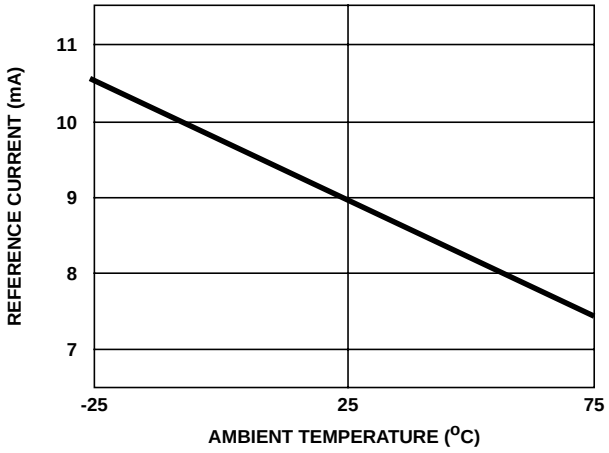


FIGURE 15. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

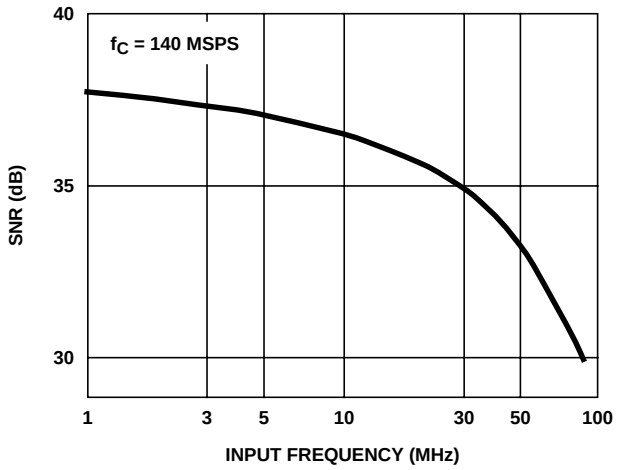


FIGURE 16. SNR vs INPUT FREQUENCY RESPONSE

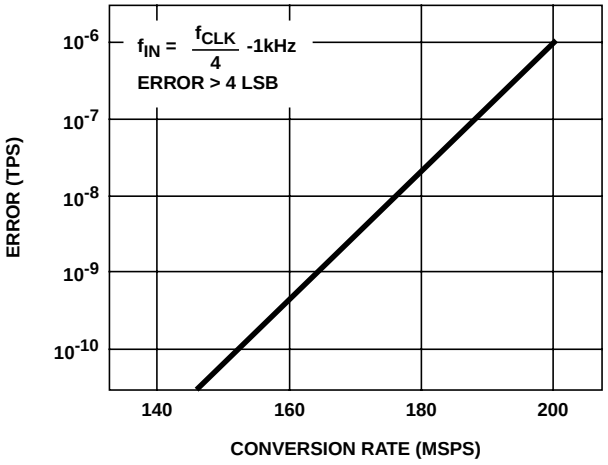


FIGURE 17. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

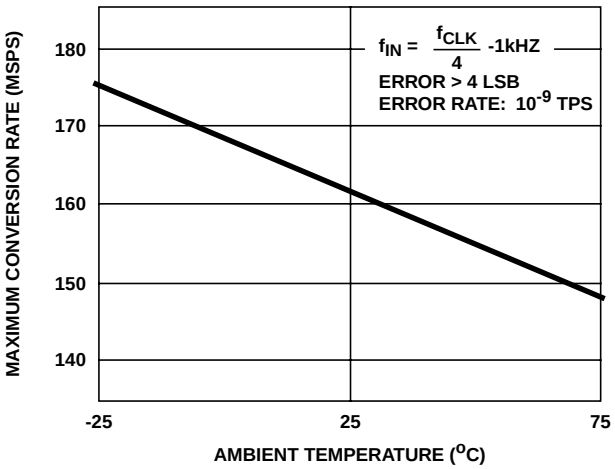


FIGURE 18. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Application Circuits

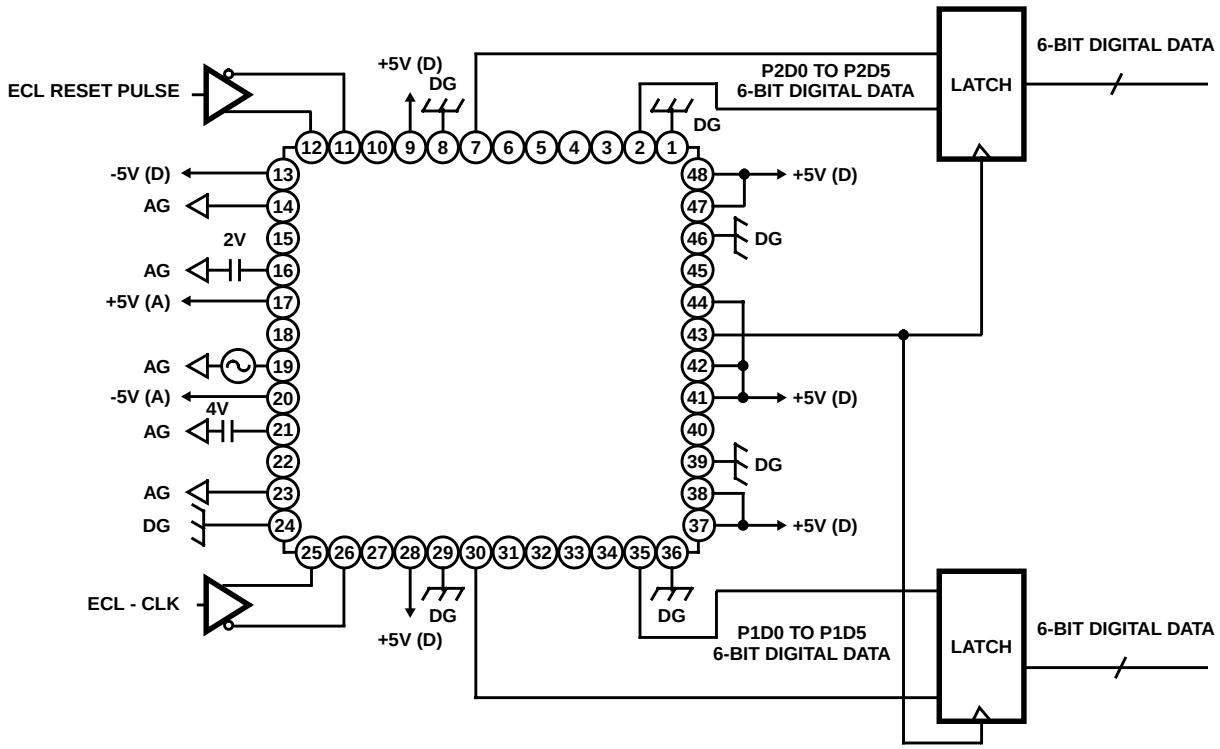


FIGURE 19. DEMUX ECL INPUT

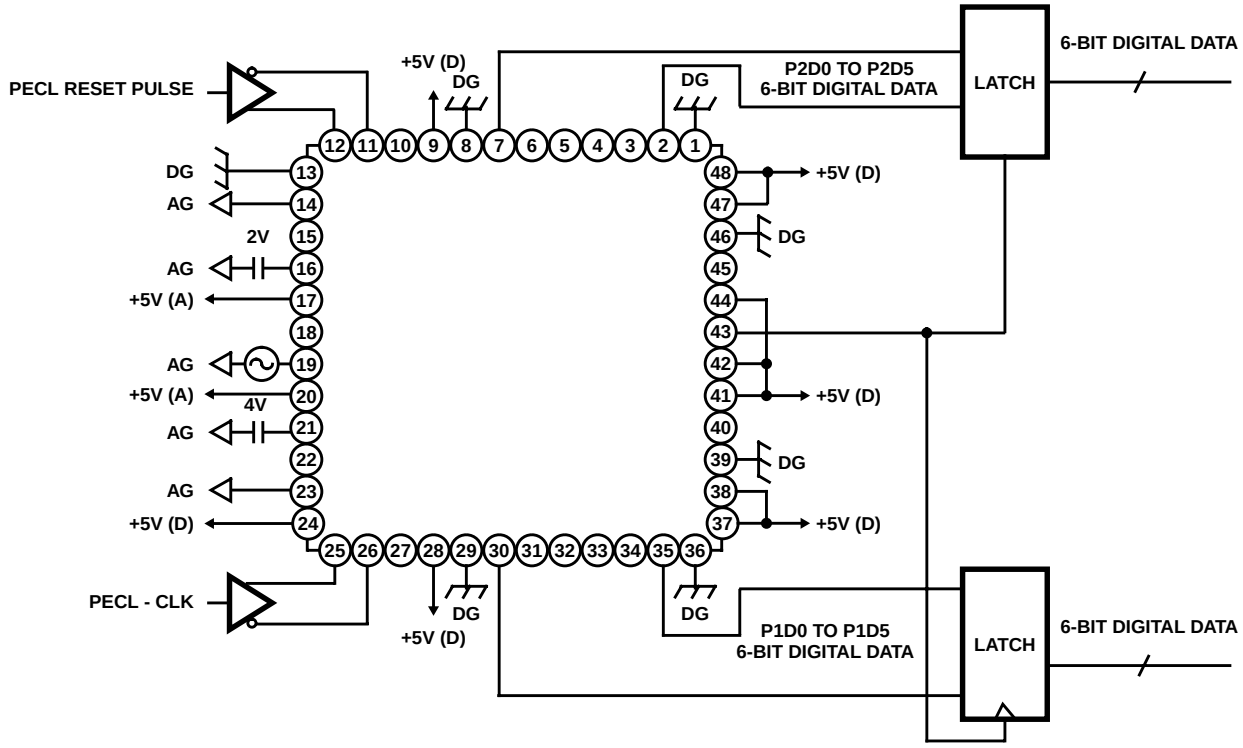


FIGURE 20. DEMUX PECL INPUT

Application Circuits (Continued)

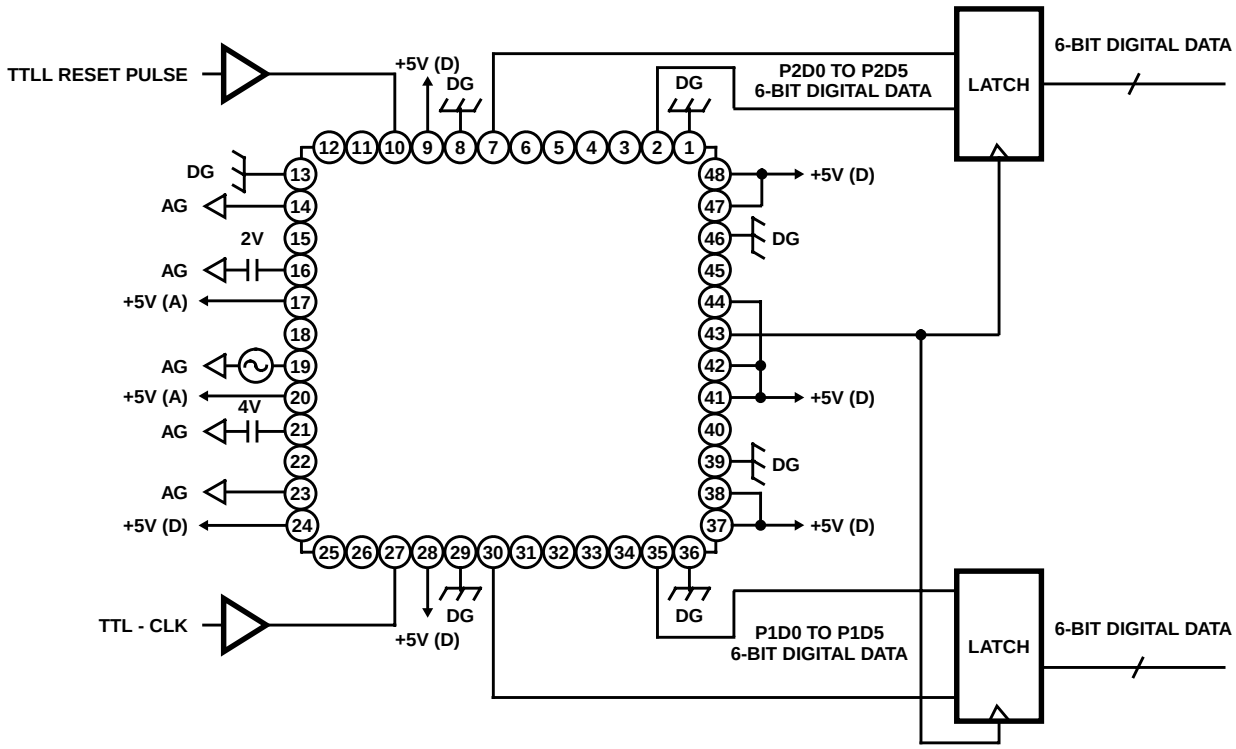


FIGURE 21. DMUX TTL INPUT

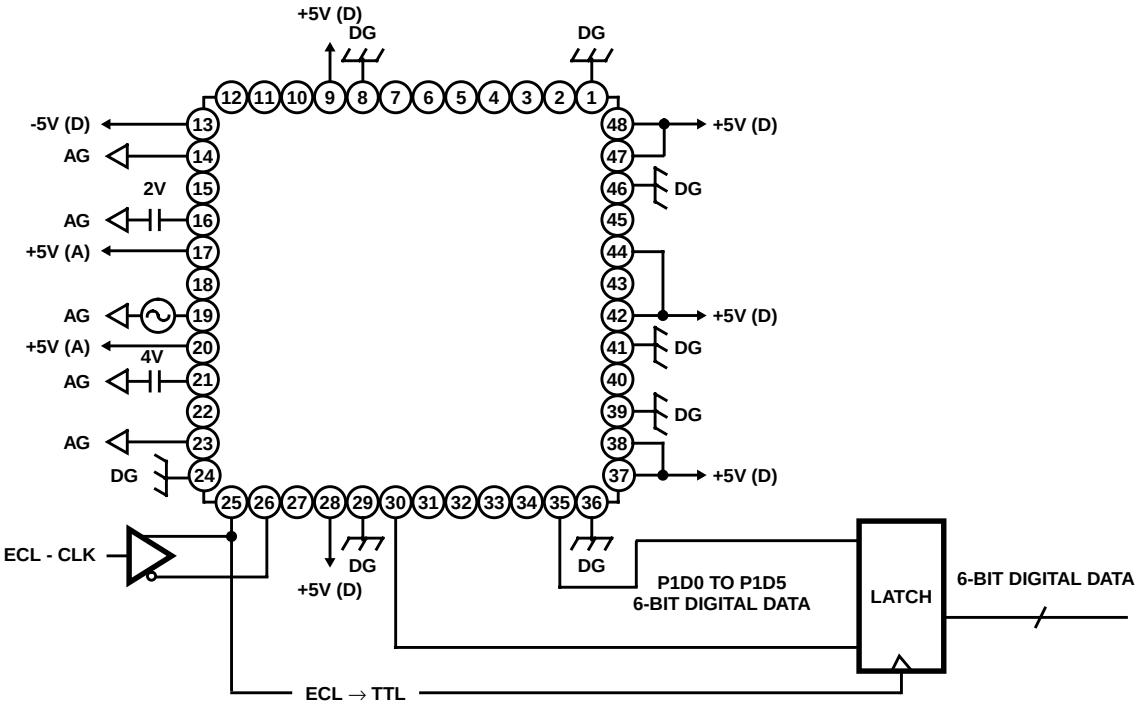


FIGURE 22. STRAIGHT ECL INPUT

Application Circuits (Continued)

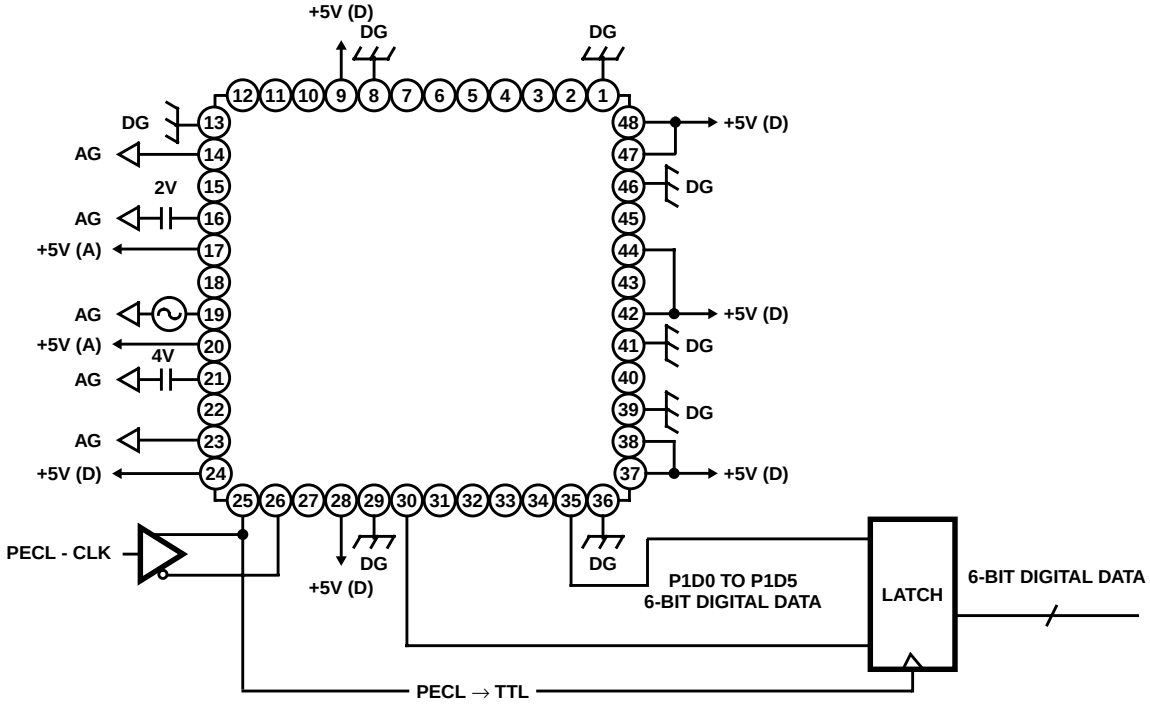


FIGURE 23. STRAIGHT PECL INPUT

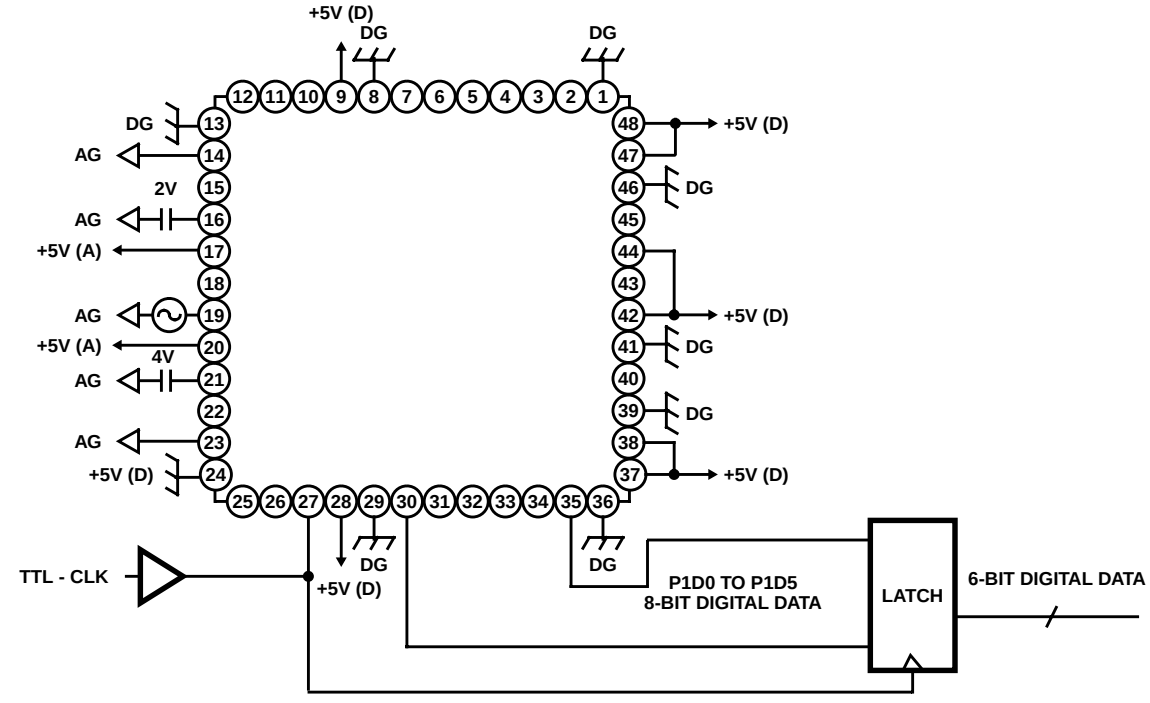


FIGURE 24. STRAIGHT TTL INPUT

Application Circuits (Continued)

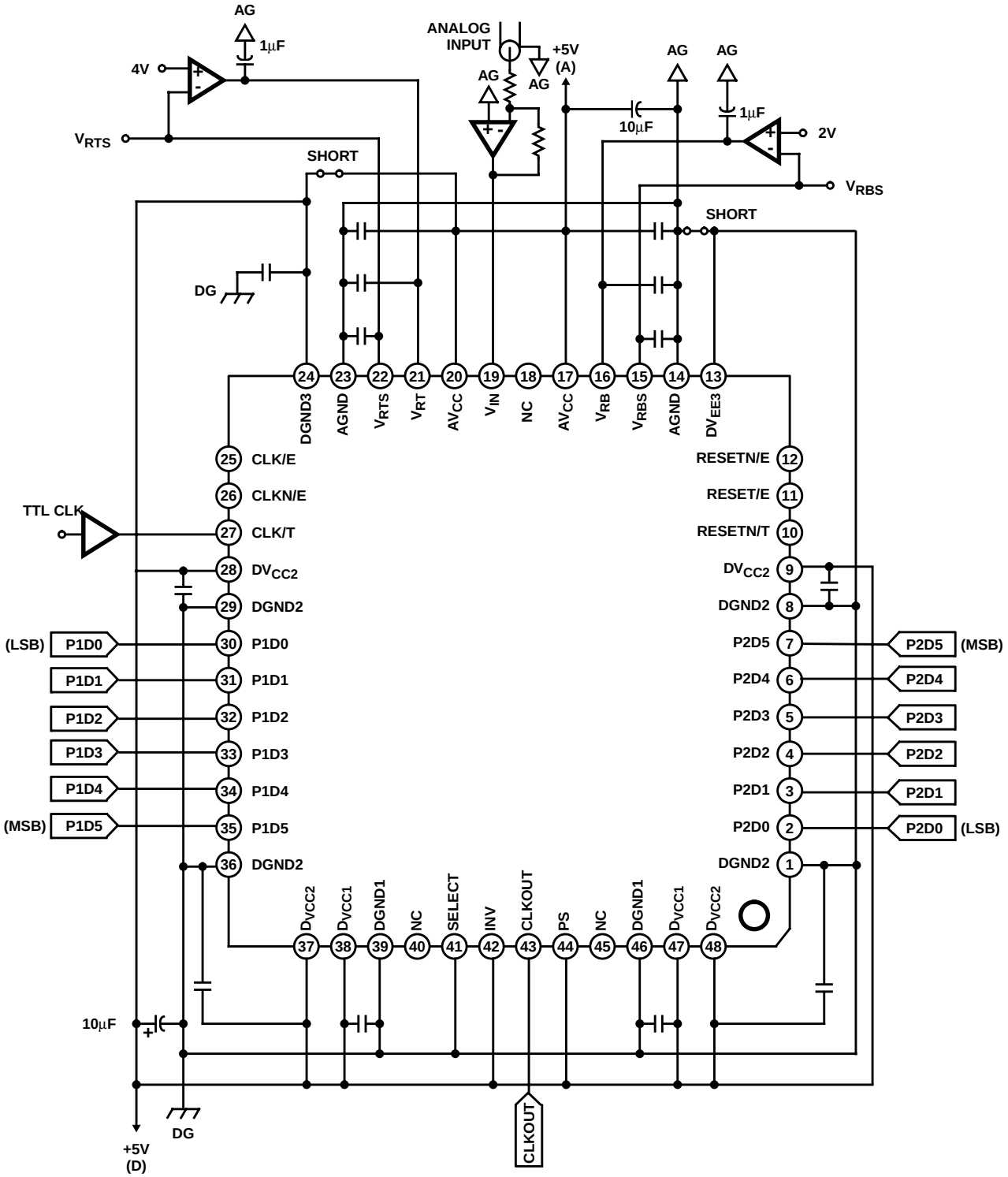


FIGURE 25. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029