Data Sheet | January 1999 | File Number 4114.2

8-Bit, 40MSPS, 2-Channel D/A Converter

The HI1177 is a dual 8-bit CMOS digital-to-analog converter. It has input/output equivalent to 2 channels of Y and C for video use or I and Q for modulators.

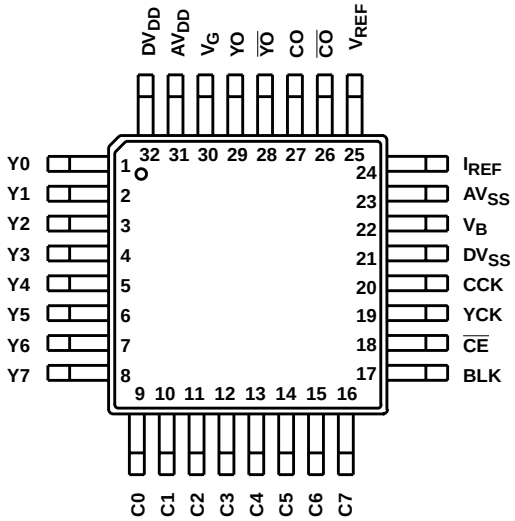
The HI1177 is available in the industrial temperature range and is supplied in a 32 lead plastic metric quad flatpack (MQFP) package.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1177JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S

Pinout

HI1177
(MQFP)
TOP VIEW



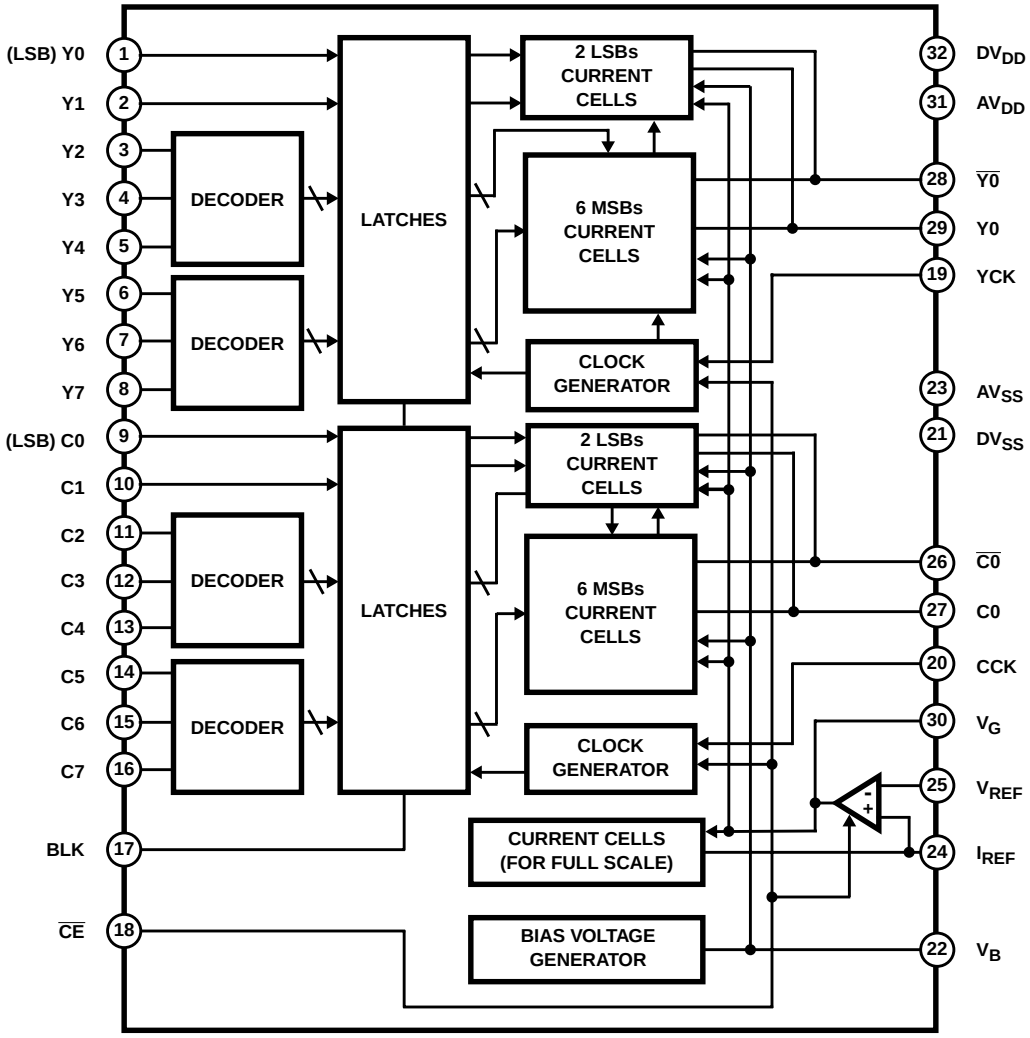
Features

- Resolution 8-Bit
- Maximum Conversion Speed 40MHz
- YC 2-Channel Input/Output
- Differential Linearity Error. . . . . $\pm$0.3 LSB
- Low Power Consumption . . . . . .160mW (200Ω Load for 2V_{P-P} Output)
- Power Supply . . . . . +5V Single
- Power-Down Mode
- Low Glitch Noise
- Direct Replacment for Sony CXD1177

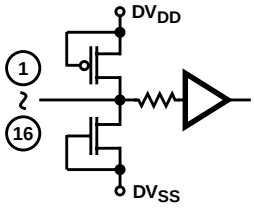
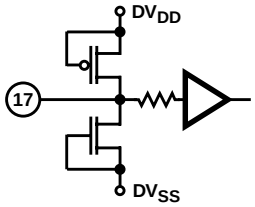
Applications

- I/Q Modulation
- YC Video
- Digital TV
- Wireless Transmitters

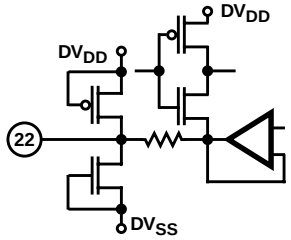
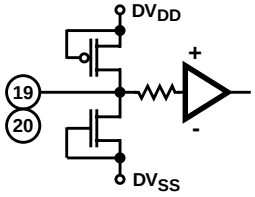
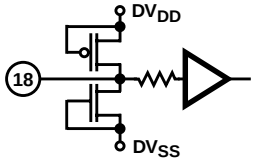
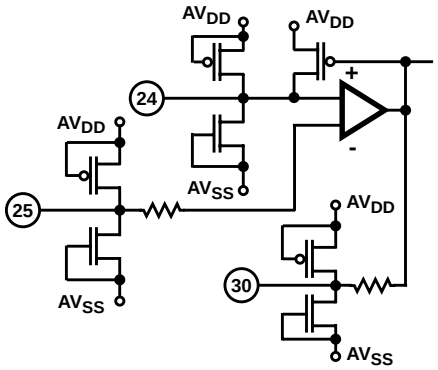
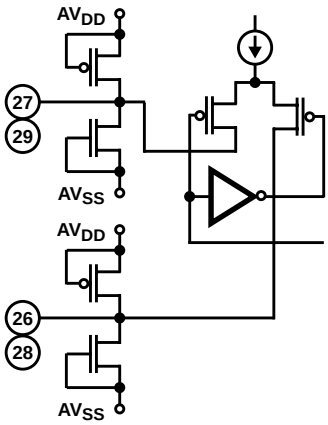
Functional Block Diagram



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	Y0 to Y7		Digital Input.
9 to 16	C0 to C7		
17	BLK		Blanking pin. No signal at “H” (Output 0V). Output condition at “L”.

Pin Descriptions (Continued)

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
22	V_B		Connect a capacitor of about 0.1µF.
19	YCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
20	CLK		
21	DV_{SS}		Digital GND.
23	AV_{SS}		Analog GND.
18	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at “H” and minimizes power consumption.
24	I_{REF}		Connect a resistance 16 times “16R” that of output resistance value “R”.
25	V_{REF}		Set full scale output value.
30	V_G		Connect a capacitor of about 0.1µF.
31	AV_{DD}		Analog V_{DD}.
27	CO		Current output pin. Voltage output can be obtained by connecting a resistance.
29	YO		
26	$\overline{CO}$		Inverted current output pin. Normally dropped to analog GND.
28	$\overline{YO}$		
32	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{DD} 7V
Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Output Current (For Each Channel), I_{OUT} . . . . . 0mA to 15mA

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Reference Input Voltage, V_{REF} 2.0V
Clock Pulse Width
t_{PW1} . . . . . 12.5ns (Min)
t_{PW0} . . . . . 12.5ns (Min)
Temperature Range, T_{OPR} . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 7) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_{CLK} = 40MHz, V_{DD} = 5V, R_{OUT} = 200Ω, V_{REF} = 2.0V, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	TEST LEVEL OR NOTES	MIN	TYP	MAX	UNITS
Resolution		n			-	8	-	bit
Maximum Conversion Speed		f_{MAX}			40	-	-	MHz
Linearity Error		E_L			-2.5	-	2.5	LSB
Differential Linearity Error		E_D			-0.3	-	0.3	LSB
Full Scale Output Voltage		V_{FS}			1.9	2.0	2.2	V
Full Scale Output Ratio		F_{SR}		Note 1	0	1.5	3	%
Full Scale Output Current		I_{FS}			-	10	15	mA
Offset Output Voltage		V_{OS}			-	-	1	mV
Power Supply Current		I_{DD}	14.3MHz, at Color Bar Data Input		-	-	32	mA
Digital Input Current	High Level	I_{IH}			-	-	5	µA
	Low Level	I_{IL}			-5	-	-	µA
Setup Time		t_S			5	-	-	ns
Hold Time		t_H			10	-	-	ns
Propagation Delay Time		t_{PD}			-	10	-	ns
Glitch Energy		GE	R_{OUT} = 75Ω		-	30	-	pV-s
Cross Talk		CT	1MHz Sin Wave Output		-	57	-	dB

NOTE:

1. Full scale output ratio = $\left|\frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}}(-1)\right| \times 100(\%)$.

I/O Correspondence Table (Output Full Scale Voltage: 2V)

INPUT CODE								OUTPUT VOLTAGE
MSB							LSB	
1	1	1	1	1	1	1	1	2.0V
⋮								
1	0	0	0	0	0	0	0	1.0V
⋮								
0	0	0	0	0	0	0	0	0V

Timing Diagram

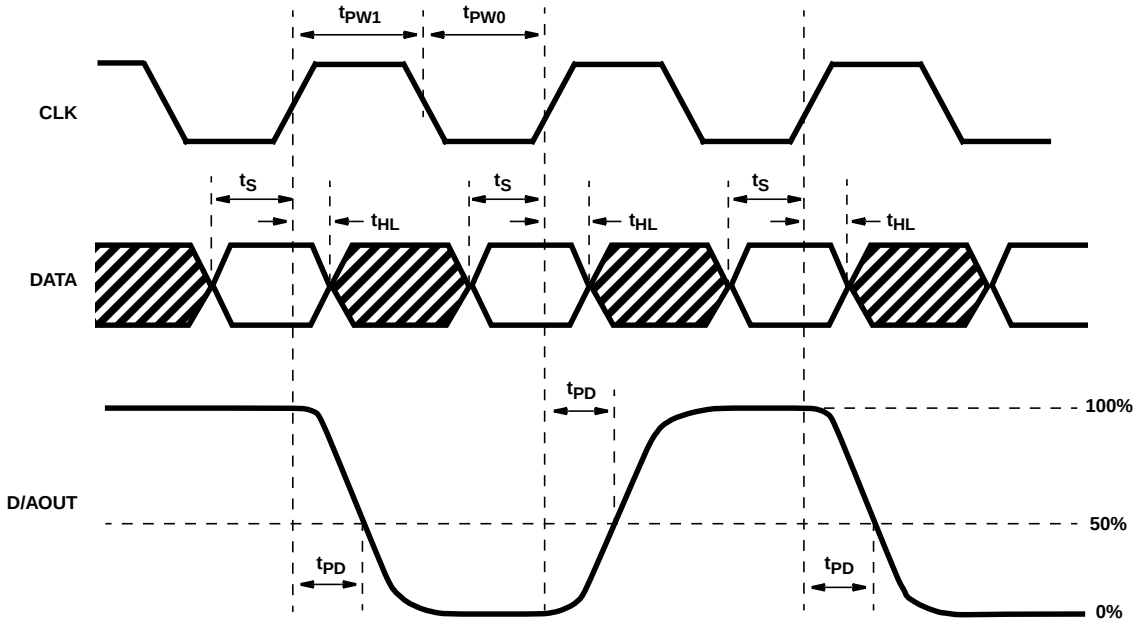


FIGURE 1.

Test Circuits

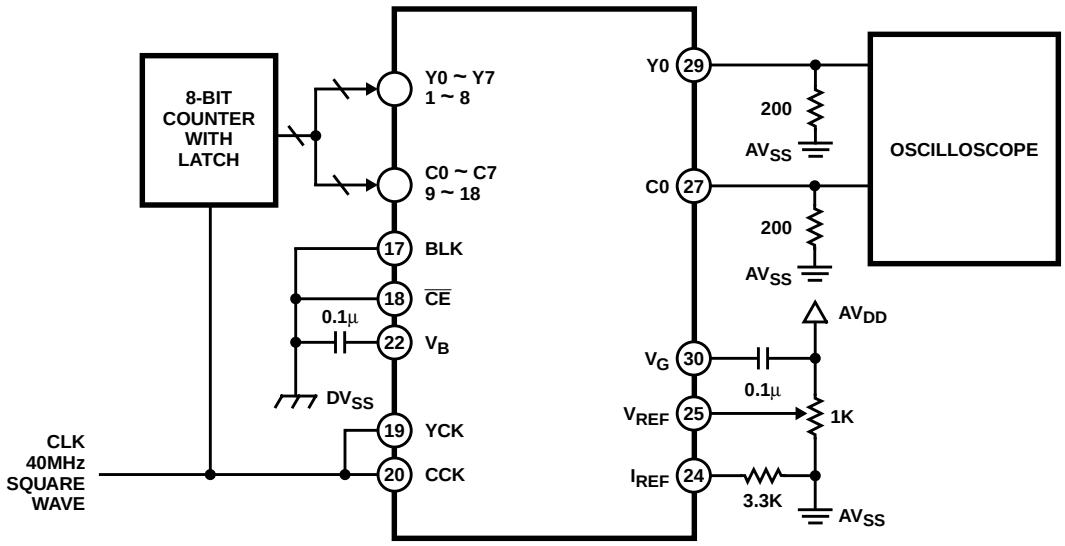


FIGURE 2. MAXIMUM CONVERSION

Test Circuits (Continued)

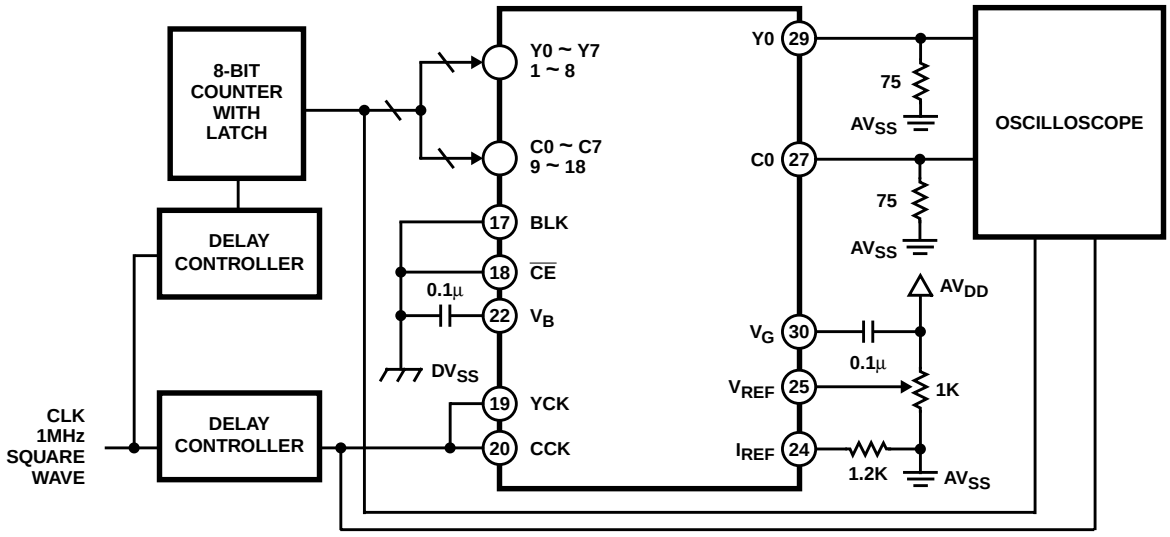


FIGURE 3. SETUP HOLD TIME AND GLITCH ENERGY

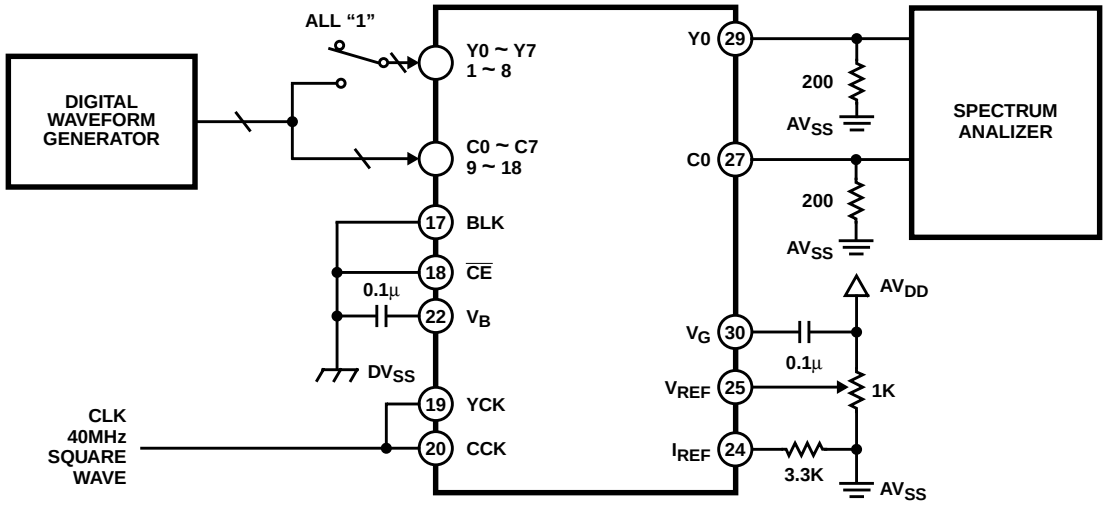


FIGURE 4. CROSSTALK

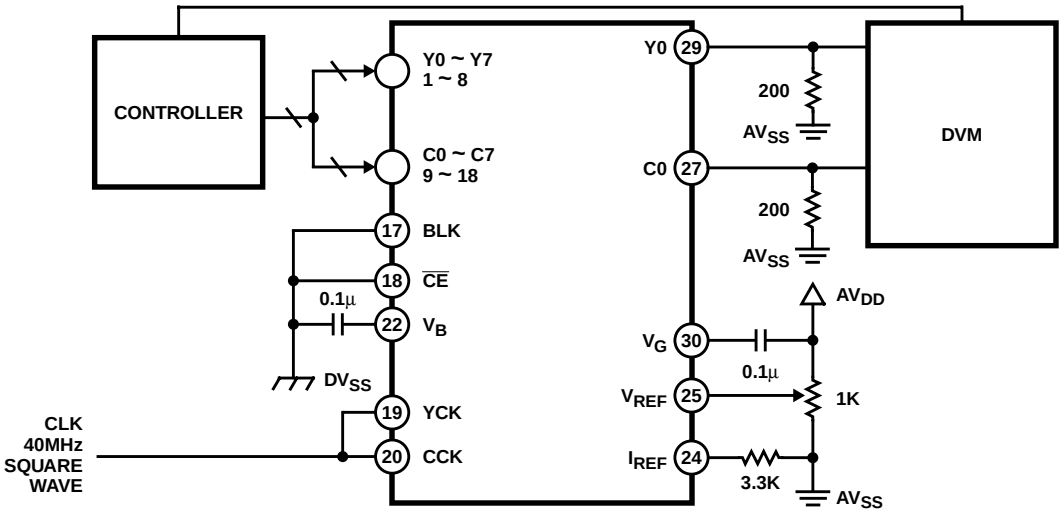


FIGURE 5. DC CHARACTERISTICS

Test Circuits (Continued)

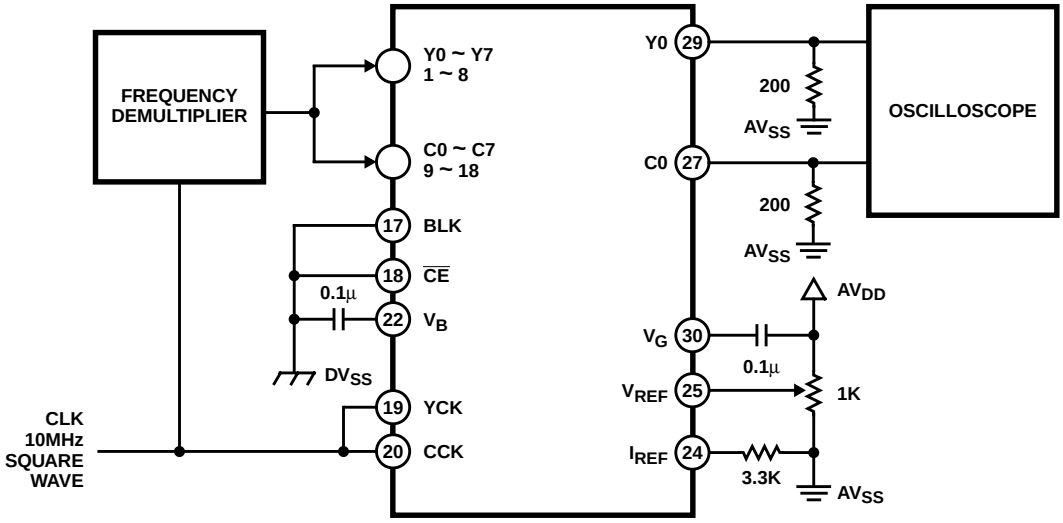


FIGURE 6. PROPAGATION DELAY TIME

Typical Performance Curves

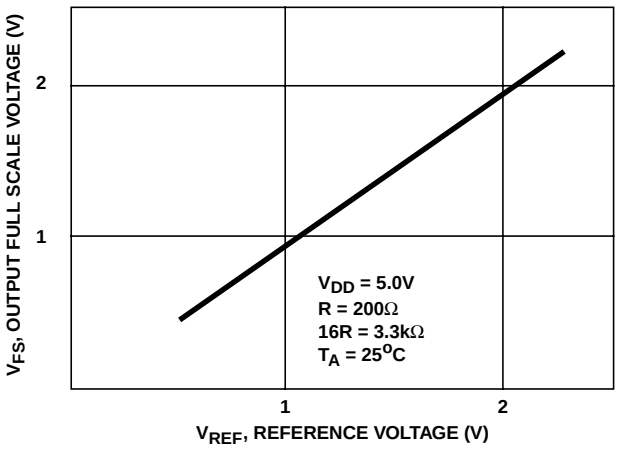


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

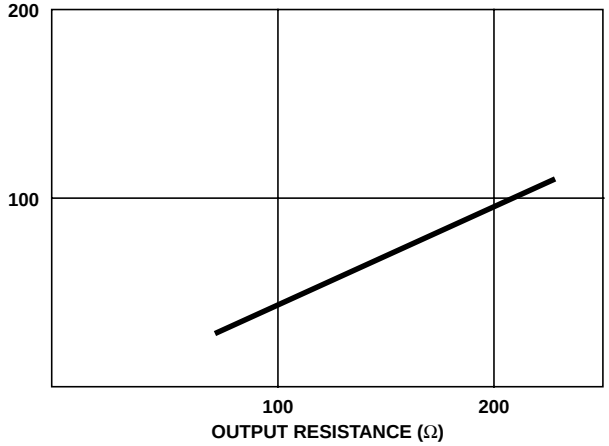


FIGURE 8. GLITCH ENERGY vs OUTPUT RESISTANCE

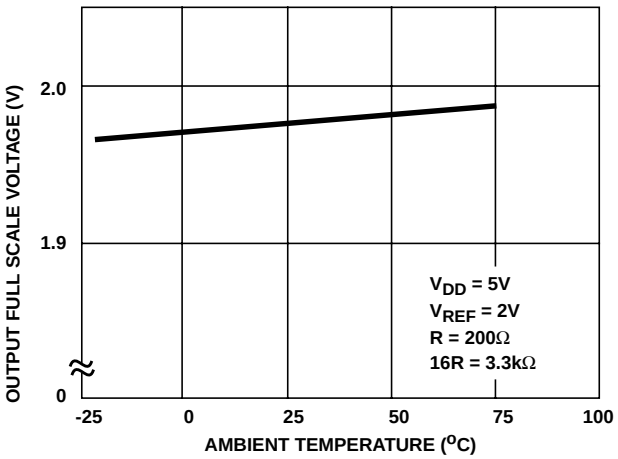


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

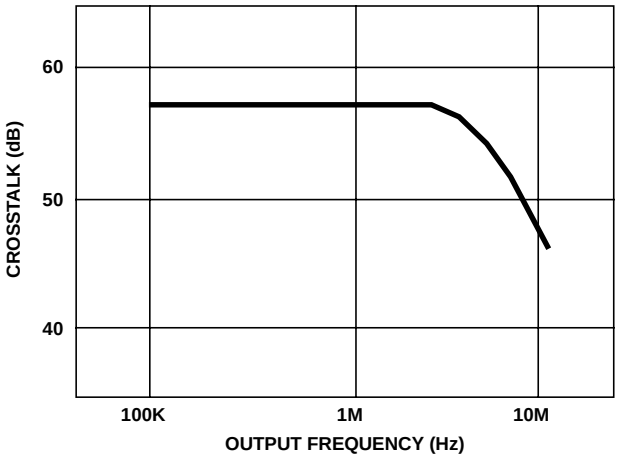


FIGURE 10. CROSSTALK vs OUTPUT FREQUENCY

Application Circuit

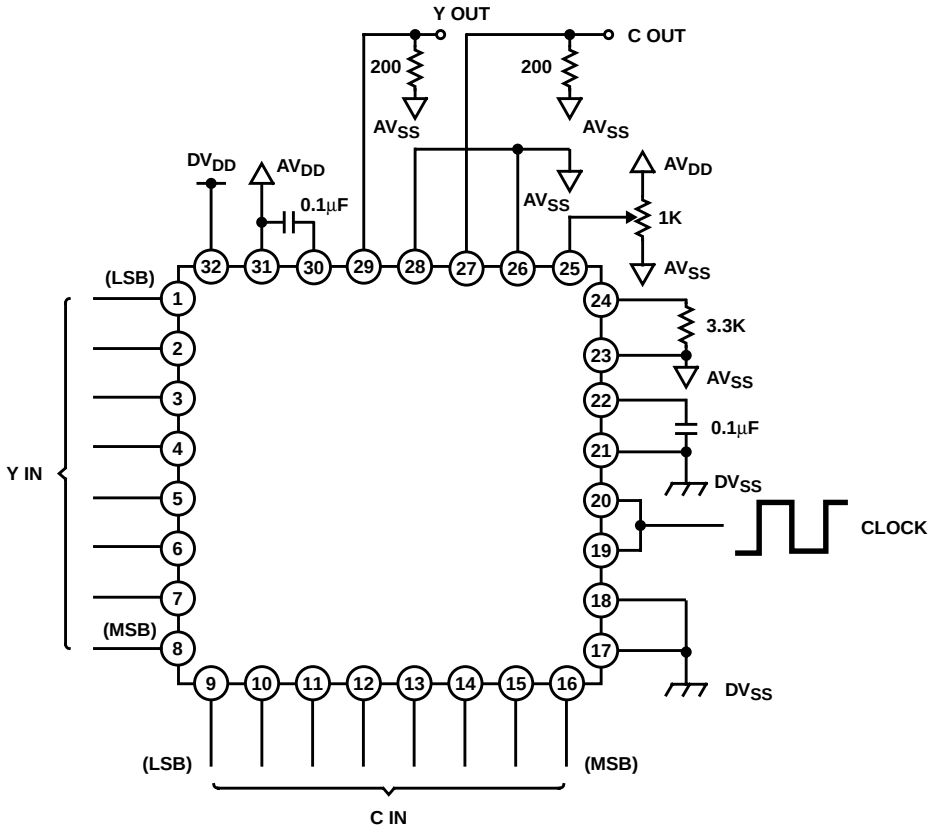


FIGURE 11.

Operation

- How to select the output resistance:
  - The HI1177 is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (Y0, C0). For specifications we have:

Output full scale voltage	V_{FS} = less than 2V
Output full scale current	I_{FS} = less than 15mA

  - Calculate the output resistance value from the relation of $V_{FS} = I_{FS}$ X R. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF}$ X 16R/R'. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.
- Phase relation between data and clock:
  - To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.
- V_{DD}, V_{SS}:
  - To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1μF, as close as possible to the pin.