

## 7V, 7A SynchroFET™ Complementary Drive Synchronous Half-Bridge

Designed with the Pentium® in mind, the Intersil SynchroFET family provides a new approach for implementing a synchronous rectified buck switching regulator. The SynchroFET™ replaces two power DMOSs, a Schottky diode, two gate drivers and synchronous control circuitry. The complementary drive circuit turns the upper FET on and the lower FET off when the input from the PWM is high. When the input from the PWM goes low the upper FET turns off and the lower FET turns on. The HIP5016 has a  $\overline{PWM}$  pin that inverts the relationship from the input to PHASE. This architecture allows the designer to utilize a low cost single-ended PWM controller in either a current or voltage mode configuration. The SynchroFET operates in continuous conduction mode reducing EMI constraints and enabling high bandwidth operation. Several features ensure easy start-up. First, the supply currents stay below specification as the supply voltages ramp up; no unexpected surges occur that might perturb a soft-start or deplete a charge-pump. Second, any power-up sequence of the  $V_{CC}$ ,  $V_{IN}$ , or PWM pins can be used without causing large currents. Third, the chip operates when  $V_{CC}$  is greater than 2V so  $V_{CC}$  can be created from a charge pump powered from  $V_{IN}$ .

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP5015IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5015IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C
HIP5016IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5016IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C

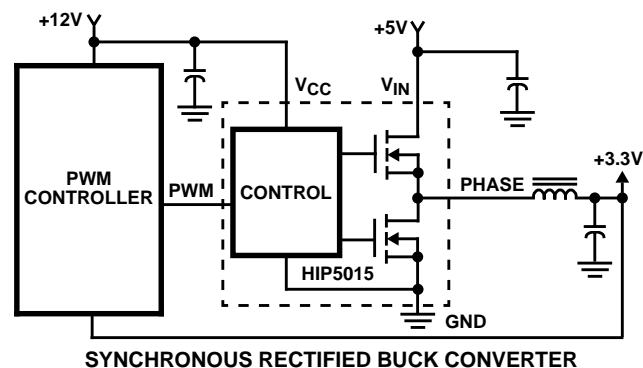
### Features

- Complementary Drive, Half-Bridge Power NMOS
- Use With Low-Cost Single-Output PWM Controllers
- Improve Efficiency Over Conventional Buck Converter with Schottky Clamp
- Minimum Deadtime Provided by Adaptive Shoot-Through Protection Eliminates External Schottky
- Grounded Case for Low EMI and Simple Heatsinking
- Low Operating Current
- Frequency Exceeding 1MHz
- Dual Polarity Input Options
- All Pins Surge Protected

### Applications

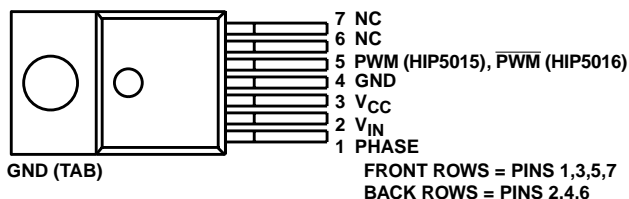
- 5V to  $\leq 3.3V$  Synchronous Buck Converters
- 3.3V to  $\leq 2.9V$  Synchronous Buck Converters
- Pentium Power Supplies
- Bus Terminations (BTL and GTL)
- Drive 5V Motors Directly from Microprocessor

### Typical Application Block Diagram

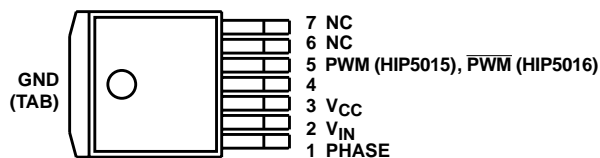


### Pinouts

HIP5015IS1, HIP5016IS1 (SIP - VERTICAL)  
TOP VIEW

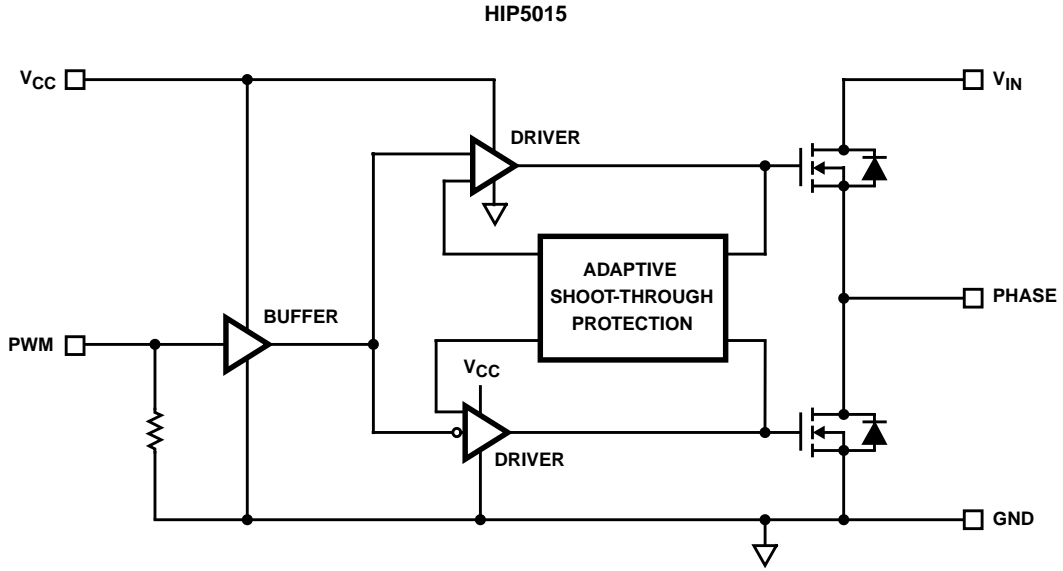


HIP5015IS, HIP5016IS (SIP - GULLWING)  
TOP VIEW

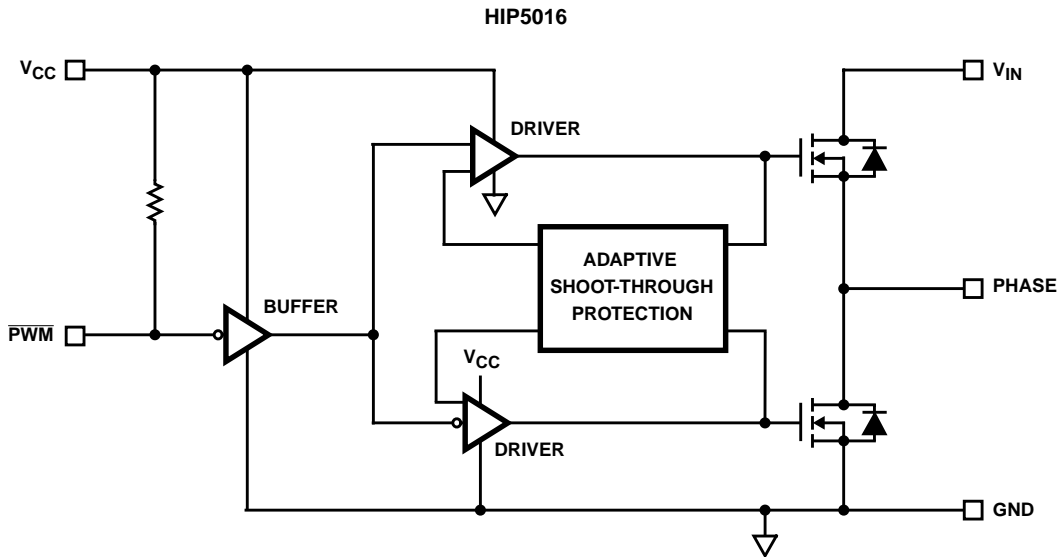


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SynchroFET™ is a trademark of Intersil Corporation.

**Non-Inverting SynchroFET Block Diagram**



**Inverting SynchroFET Block Diagram**



# HIP5015, HIP5016

## Absolute Maximum Ratings

Supply Voltage, $V_{CC}$	+16V
Input Voltage $V_{IN}$	+7V
$I_{PHASE}$ , $I_{VIN}$ , $I_{GND}$	7A (Repetitive Peak)
PWM Input	-4V to +16V
ESD Classification	Class 3 (4kV)
Lead Temperature (Soldering 10s) (Lead Tips Only)	300°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature Range	-40°C to 150°C

## Operating Conditions

Supply Voltage, $V_{CC}$	+12V, $\pm 20\%$
Input Voltage $V_{IN}$	0V to 5.5V
Supply Voltage, $V_{CC}$ , minimum for charge-pumped start-up	+4.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

## Thermal Information (Typical)

Package	$\theta_{JC}^{\dagger\dagger}$ (°C/W)	$\theta_{JA}$ (°C/W) <sup>†</sup>				
		0	1	2	3	3 <sup>†††</sup>
SIP (IS)	2	55	30	25	24	18
SIP (IS1)	2	55	-	-	-	-

<sup>†</sup> Versus additional square inches of 1 ounce copper on the printed circuit board.

<sup>††</sup>  $\theta_{JC}$  is typical with an infinite heatsink.

<sup>†††</sup> 200 linear feet per minute of air flow.

$I_{PHASE}$	.5A
$I_{VIN}$	.4A
$I_{GND}$	.3A

## Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ $T_J = +150^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
$r_{DS(ON)}$ Upper MOSFET	$R_{DSU}$	$V_{CC} = 12V, V_{IN} = 5V$	-	68	78	-	130	m $\Omega$
$r_{DS(ON)}$ Lower MOSFET	$R_{DSL}$	$V_{CC} = 12V, V_{IN} = 5V$	-	72	82	-	136	m $\Omega$
$V_{IN}$ Operating Current	$I_{VINO}$	$V_{IN} = 5V$ , No Load, 500kHz	-	1.8	4	-	5	mA
$V_{IN}$ Quiescent Current	$I_{VIN}$	PWM or $\overline{PWM} = V_{CC}$ or GND	-	0.1	10	-	100	$\mu\text{A}$
$V_{CC}$ Operating Current	$I_{CCO}$	$V_{CC} = 12V$ , 500kHz	-	4.3	7	-	9	mA
$V_{CC}$ Quiescent Current (HIP5015)	$I_{CCIH}$	PWM = $V_{CC}$	-	40	-	-	300	$\mu\text{A}$
$V_{CC}$ Quiescent Current (HIP5015)	$I_{CCIL}$	PWM = GND	-	0.1	10	-	100	$\mu\text{A}$
$V_{CC}$ Quiescent Current (HIP5016)	$I_{CCNIH}$	$\overline{PWM} = V_{CC}$	-	0.1	10	-	100	$\mu\text{A}$
$V_{CC}$ Quiescent Current (HIP5016)	$I_{CCNIL}$	$\overline{PWM} = GND$	-	100	-	-	300	$\mu\text{A}$
Low Level PWM Input Voltage	$V_{IL}$		-	1.8	-	1	-	V
High Level PWM Input Voltage	$V_{IH}$		-	2.1	-	-	3	V
PWM Input Voltage Hysteresis	$V_{IHYS}$		-	0.3	-	-	-	V
Input Pulldown Resistance (HIP5015)	$R_{PWM}$		-	220	-	100	400	k $\Omega$
Input Pullup Resistance (HIP5016)	$R_{PWM}$		-	220	-	100	400	k $\Omega$

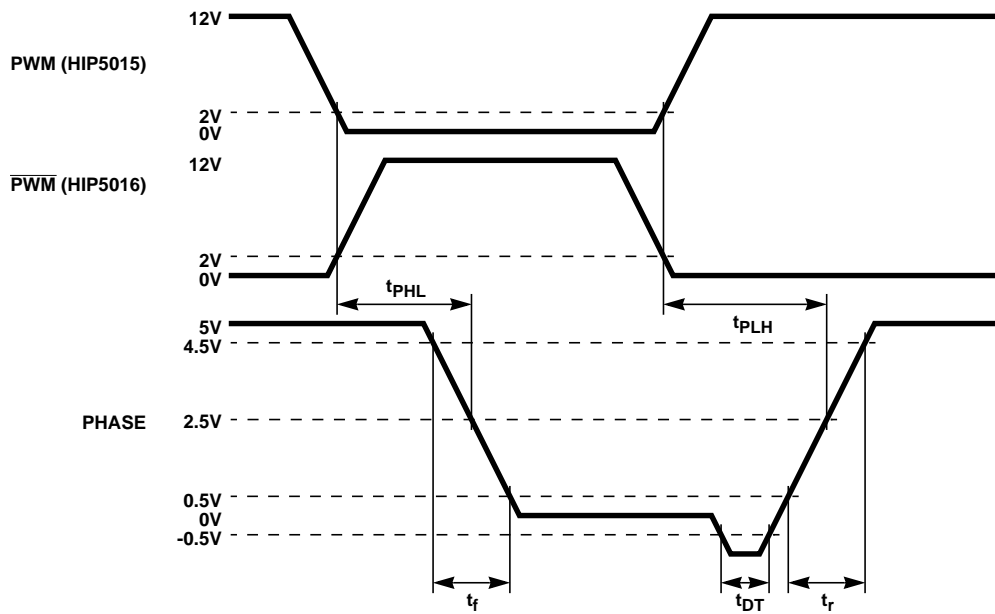
## Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ $T_J = +150^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Upper Device Turn-Off Delay	$t_{PHL}$	$V_{CC} = 12V, I_{PHASE} = -0.5A$	-	30	50	-	80	ns
Lower Device Turn-Off Delay	$t_{PLH}$	$V_{CC} = 12V, I_{PHASE} = +0.5A$	-	30	50	-	80	ns
Dead Time	$t_{DT}$	$V_{CC} = +12V, I_{PHASE} = -0.5A$	-	10	-	-	-	ns
Phase Rise-Time	$t_r$	$V_{CC} = 12V, I_{PHASE} = -0.5A$	-	20	-	-	-	ns
Phase Fall-Time	$t_f$	$V_{CC} = 12V, I_{PHASE} = +0.5A$	-	20	-	-	-	ns

**Pin Descriptions**

SYMBOL	DESCRIPTION
V <sub>CC</sub>	Positive supply to control logic and gate drivers. De-couple this pin to GND.
V <sub>IN</sub>	FET Switch Input Voltage. De-couple this pin to GND.
PHASE	Output.
PWM (HIP5015) PWM (HIP5016)	Single Ended Control Input. This input connects to the PWM controller output.
GND	System Ground.

**Timing Diagram**



NOTE: I<sub>PHASE</sub> = +0.5A for t<sub>PLH</sub> and t<sub>r</sub>, I<sub>PHASE</sub> = -0.5A for t<sub>PHL</sub>, t<sub>DT</sub>, and t<sub>f</sub>.

**FIGURE 1.**

Typical Performance Curves

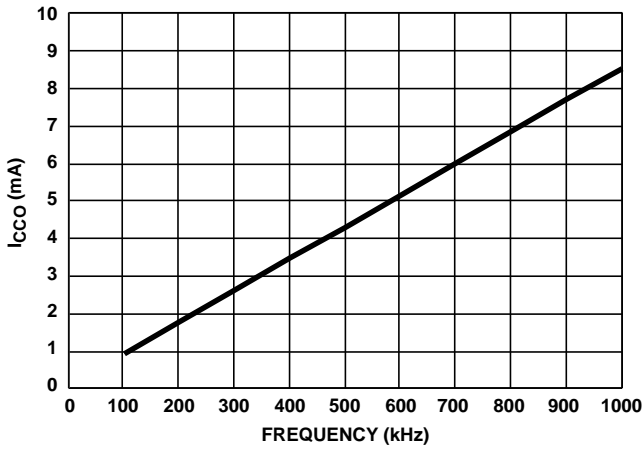


FIGURE 2. I<sub>CCO</sub> vs FREQUENCY

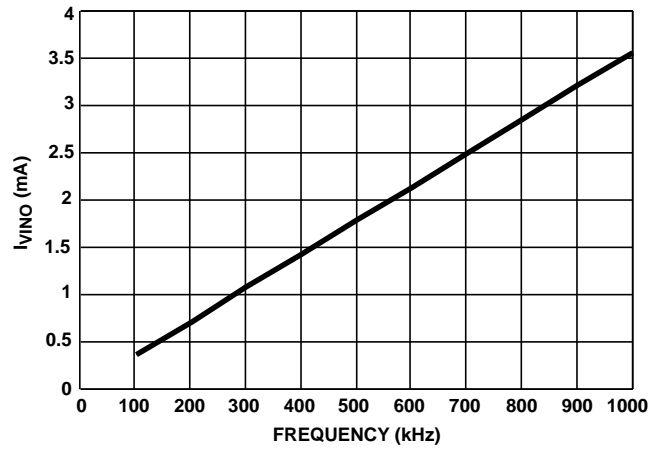


FIGURE 3. I<sub>VINO</sub> vs FREQUENCY

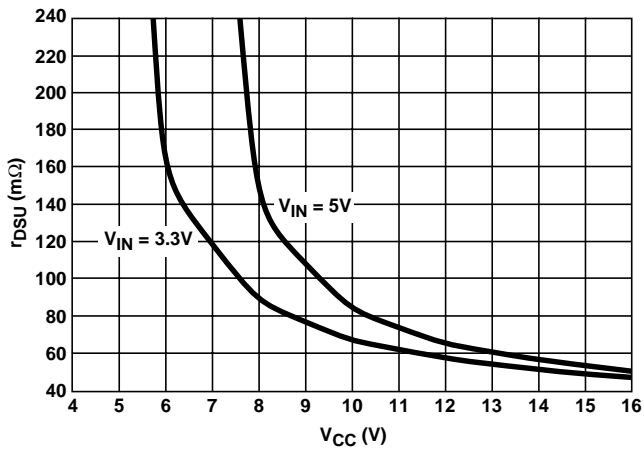


FIGURE 4. R<sub>DSU</sub> vs V<sub>Cc</sub>

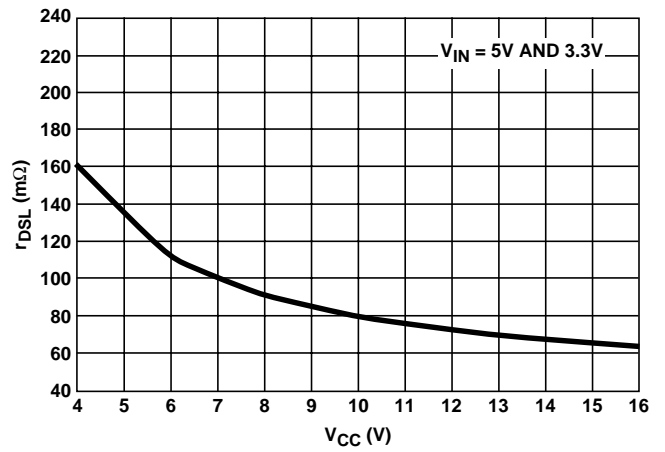


FIGURE 5. R<sub>DSL</sub> vs V<sub>Cc</sub>

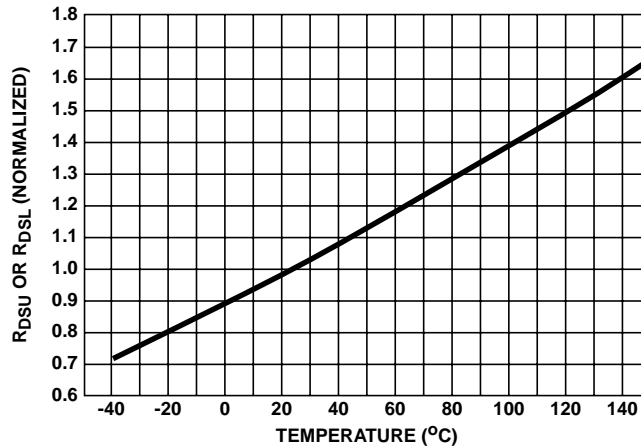


FIGURE 6. R<sub>DSU</sub> OR R<sub>DSL</sub> vs TEMPERATURE

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