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## PRELIMINARY

May 1999

## CDMA/AMPS Downconverter with AGC Capability

### Features

- RF Frequency Range . . . . . 869MHz to 895MHz
- IF Operation . . . . . 10MHz to 100MHz
- LNA Gain. . . . . 16dB
- LNA NF . . . . . 2.3dB
- Mixer Gain. . . . . 16dB
- Mixer NF . . . . . 11dB
- Single Supply Battery Operation . . . . . 2.7V to 3.3V
- Power Enable/Disable Control
- PIN Diode Attenuator DC Control

### Applications

- IS95A CDMA/AMPS Dual Mode Handsets
- Wideband CDMA Handsets
- CDMA/TDMA Packet Protocol Radios
- Full Duplex Transceivers
- Portable Battery Powered Equipment



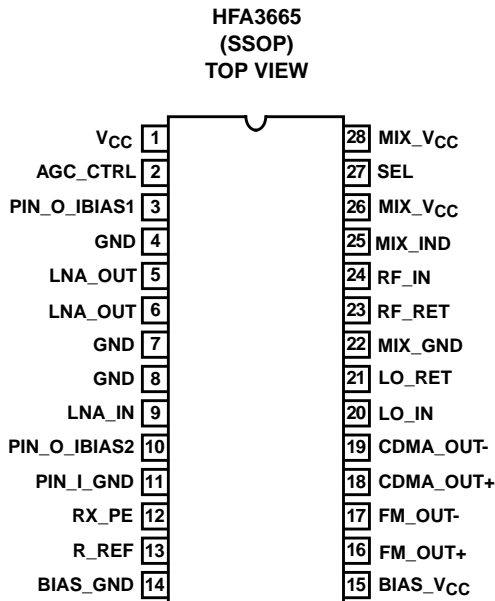
### Description

The HFA3665 is a monolithic bipolar downconverter for CDMA/AMPS cellular applications. Manufactured in the Intersil UHF1X process, the device consists of a low noise cascode amplifier, a double balanced downconversion mixer and a pair of linearized and temperature compensated PIN diode biasing current sources for external RF AGC applications. In addition, the device offers two independent and selectable differential mixer IF output ports to be used with dual mode IF filters and requires low drive levels from the local oscillator. The HFA3665 is one of the four chips in the PRISM<sup>TM</sup> chip set and is housed in a small outline 28 lead SSOP package ideally suited for cellular handset applications.

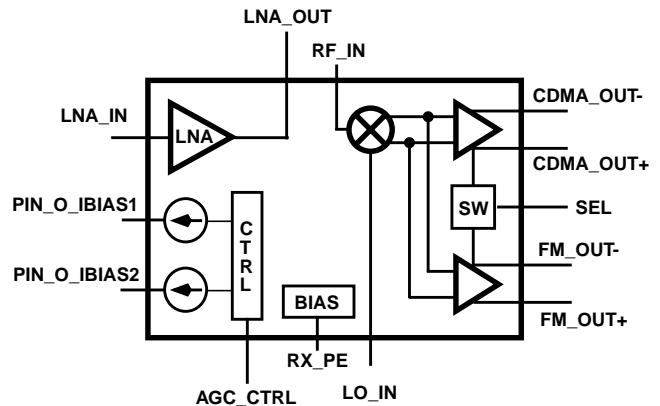
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE       | PKG. NO. |
|-------------|------------------|---------------|----------|
| HFA3665IA   | -40 to 85        | 28 Ld SSOP    | M28.15   |
| HFA3665IA96 | -40 to 85        | Tape and Reel |          |

### Pinout



### Block Diagram



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## HFA3665

### Pin Descriptions

| PIN NUMBER | NAME                 | DESCRIPTION  |
|------------|----------------------|--|
| 1          | V <sub>CC</sub>      | LNA and PIN diode bias control Power Supply. Use high quality RF decoupling capacitors at the pin.   |
| 2          | AGC_CTRL             | AGC control current input pin. Requires a 9.53K 1% resistor for scale factor and temperature compensation of the current sources.                              |
| 3          | PIN_O_IBIAS1         | Current output for a PIN diode bias control. Use a 2200pF filter capacitor to ground.  |
| 4          | GND                  | LNA bias ground return.  |
| 5, 6       | LNA_OUT              | LNA open collector output. This pins are internally bonded to the same device output.  |
| 7, 8       | GND                  | LNA RF ground return. Degeneration (inductance) can be added to this pin.  |
| 9          | LNA_IN               | LNA input.   |
| 10         | PIN_O_IBIAS2         | Second current output for PIN diode bias control. Use a 2200pF filter capacitor to ground.   |
| 11         | PIN_I_GND            | PIN diode bias control ground return.  |
| 12         | RX_PE                | Power enable control input. HIGH for normal operation. LOW for power down.   |
| 13         | R_REF                | Bias setting resistor. 523Ω 1% for optimum performance and parameter distribution.   |
| 14         | BIAS_GND             | Reference circuit ground return.   |
| 15         | BIAS_V <sub>CC</sub> | Reference circuit Power Supply. Use high quality RF decoupling capacitors right at the pin.  |
| 16         | FM_OUT+              | Positive IF FM output. Open collector PNP. Requires a DC return to ground.   |
| 17         | FM_OUT-              | Negative IF FM output. Open collector PNP. Requires a DC return to ground.   |
| 18         | CDMA_OUT+            | Positive IF CDMA output. Open collector PNP. Requires a DC return to ground.   |
| 19         | CDMA_OUT-            | Negative IF CDMA output. Open collector PNP. Requires a DC return to ground.   |
| 20         | LO_IN                | Mixer Local Oscillator input. Requires AC coupling and directly matches to 50Ω.  |
| 21         | LO_RET               | Mixer Local Oscillator complementary input. Requires a bypass capacitor to ground as a return reference.   |
| 22         | MIX_GND              | Mixer ground return.   |
| 23         | RF_RET               | Mixer RF port complementary input. Requires a bypass capacitor to ground as a return reference.  |
| 24         | RF_IN                | Mixer RF input. Requires AC coupling and a match network to 50Ω.   |
| 25         | MIX_IND              | Mixer common mode bias inductor. Use a RF choke to ground with high impedance at 900MHz. Low loss inductors with parallel resonance close to 900MHz are ideal. |
| 26, 28     | MIX_V <sub>CC</sub>  | Mixer Power Supply Pins. Use high quality RF decoupling capacitors at each one of the pins.  |
| 27         | SEL                  | Selects the CDMA or the FM output IF amplifier. HIGH selects the CDMA amplifier. LOW the FM amplifier output.  |

# HFA3665

## Absolute Maximum Ratings

Supply Voltage . . . . . -0.3 to 3.6V  
 Voltage on Any Other Pin except 5 and 6 (6.0V) . -0.3 to V<sub>CC</sub> +0.3V

## Operating Conditions

Supply Voltage Range . . . . . 2.7V to 3.3V  
 Temperature Range . . . . . -40°C ≤ T<sub>A</sub> ≤ 85°C

## Thermal Information

Thermal Resistance (Typical, Note 1) θ<sub>JA</sub> (°C/W)  
 SSOP Package . . . . . 88  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Temperature Range . . . . . -40°C ≤ T<sub>A</sub> ≤ 85°C  
 Maximum Storage Temperature Range . . . . . -65°C ≤ T<sub>A</sub> ≤ 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

| PARAMETER   | TEST CONDITION                         | (NOTE 2)<br>TEST LEVEL | TEMP (°C) | MIN  | TYP   | MAX   | UNITS |
|---|--|------------------------|-----------|------|-------|-------|-------|
| <b>LNA SPECIFICATIONS AT 885MHz, V<sub>CC</sub> = 3.0V, VLNA = 3.0V unless otherwise specified (Test schematics as in page 5)</b> |  |                        |           |      |       |       |       |
| RF Frequency Range  | Output Match net.                      | B                      | 25        | 869  | -     | 895   | MHz   |
| Power Gain  | -30dBm input                           | A                      | 25        | 14   | 16.0  | 17.5  | dB    |
| IP3I, Input referenced 3rd Order Intercept  | VLNA = 3.0V                            | A                      | 25        | -    | +2    | -     | dBm   |
|   | VLNA = 3.6V                            | A                      | 25        | -    | +6    | -     | dBm   |
|   | VLNA = 5.0V                            | A                      | 25        | -    | +7.5  | -     | dBm   |
| IP1dB, Input Referenced Compression Point   | VLNA = 3.6V                            | A                      | 25        | -    | -7    | -     | dBm   |
| Noise Figure  |  | B                      | 25        | -    | 2.3   | -     | dB    |
| Input VSWR  |  | A                      | 25        | -    | 2.2:1 | 2.5:1 | -     |
| Output VSWR   | Output network as in the Apps. diagram | A                      | 25        | -    | 1.6:1 | 2.0:1 | -     |
| <b>MIXER SPECIFICATIONS AT -3dBm LO at 970MHz AND IF of 85MHz</b>   |  |                        |           |      |       |       |       |
| RF Frequency Range (Typical)  |  | B                      | 25        | 869  | -     | 895   | MHz   |
| IF Frequency Range  |  | B                      | 25        | 10   | 85    | 100   | MHz   |
| LO Frequency Range (Typical)  |  | B                      | 25        | 954  | -     | 980   | MHz   |
| Power Conversion Gain   | Note 3                                 | A                      | 25        | 15.1 | 16.7  | 18.3  | dB    |
| Voltage Conversion Gain   | Differential IF output load = 2.95K    | B                      | 25        | -    | 34.4  | -     | dB    |
| Gain Flatness Across the RF Freq. Range   |  | B                      | 25        | -    | -     | 0.6   | dB    |
| Noise Figure, SSB   | Note 3                                 | B                      | 25        | -    | 10.6  | 11.4  | dB    |
| IP3I, Input Referenced 3rd Order Intercept  |  | A                      | 25        | 0    | 2.6   | -     | dBm   |
| IP1dB, Input Referenced Compression Point   |  | A                      | 25        | -    | -10   | -     | dBm   |
| LO Drive Level  |  | A                      | 25        | -6   | -3    | 0     | dBm   |
| LO to IF Isolation  |  | A                      | 25        | -    | 30    | -     |       |
| LO to RF Isolation  |  | A                      | 25        | 20   | 32    | -     | dB    |
| RF VSWR   | Input network as in the Apps diagram   | A                      | 25        | -    | 1.6:1 | 2:1   | -     |

## HFA3665

### Electrical Specifications (Continued)

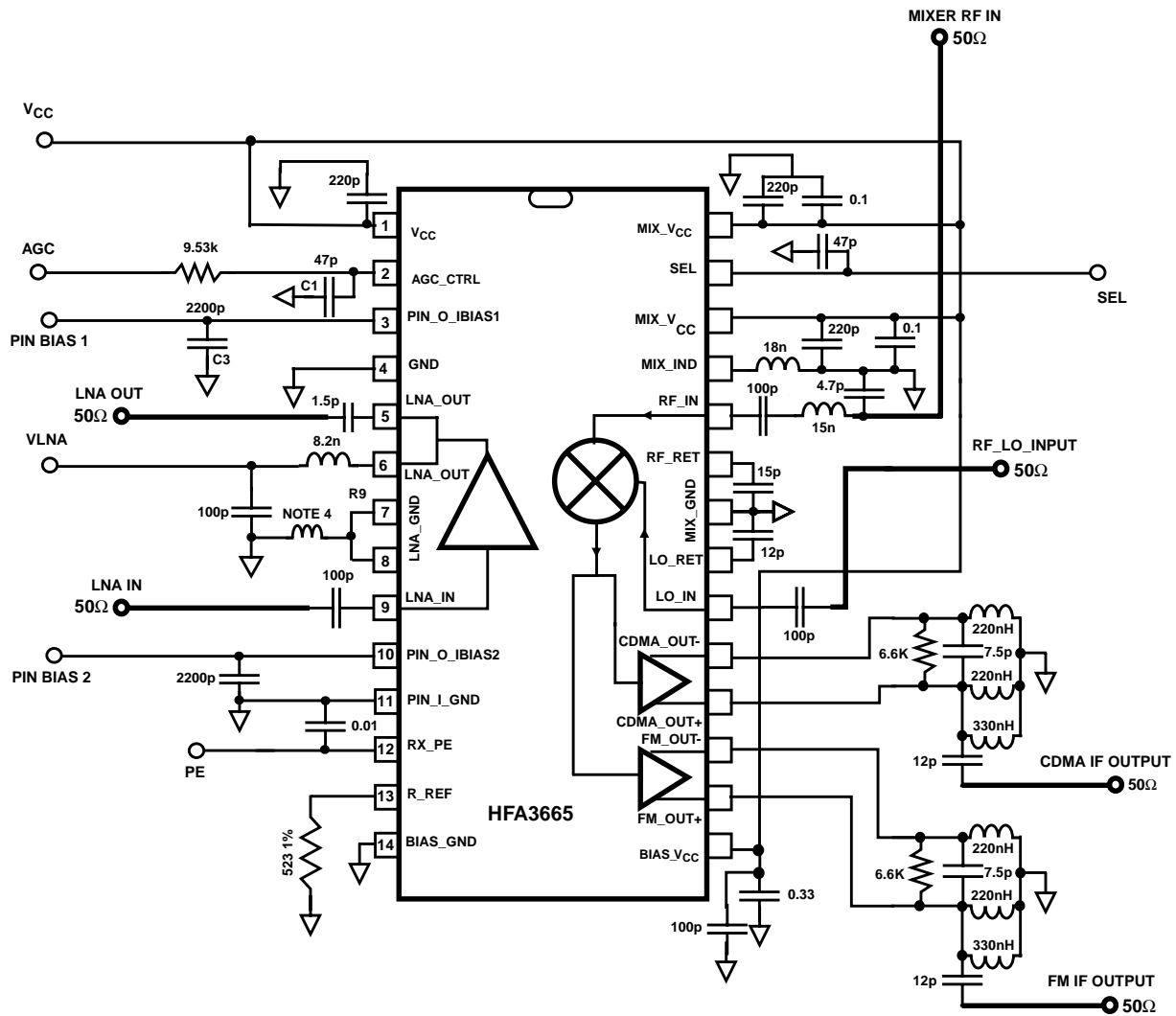
| PARAMETER  | TEST CONDITION         | (NOTE 2)<br>TEST LEVEL | TEMP (°C) | MIN  | TYP   | MAX  | UNITS |
|--|------------------------|------------------------|-----------|------|-------|------|-------|
| LO VSWR  |                        | A                      | 25        | -    | 2.0:1 | -    | -     |
| IF Output Parallel Resistance CDMA or FM port (85MHz) Single End to GND.               |                        | B                      | 25        | -    | 12.4  | -    | kΩ    |
| IF Output Parallel Capacitance CDMA or FM port (85MHz) Single End to GND.              |                        | B                      | 25        | -    | 1.7   | -    | pF    |
| <b>PIN DIODE BIAS CURRENT SOURCE SPECIFICATIONS (EACH OUTPUT Terminated into 0.7V)</b> |                        |                        |           |      |       |      |       |
| Typical PIN diode AGC Range  | Application schematic. | B                      | Full      | 33   | 38    | -    | dB    |
| AGC_CTRL Voltage control Range   | Rseries = 9.53K        | A                      | 25        | 0.5  | -     | 2.5  | V     |
| PIN_O_IBIAS Max. Source Current.   | AGC_CTRL = 2.0V        | A                      | 25        | -    | 5.2   | -    | mA    |
| PIN_O_IBIAS Current  | AGC_CTRL = 1.8         | A                      | 25        | -    | 3.0   | -    | mA    |
|  | AGC_CTRL = 1.4V        | A                      | 25        | -    | 0.47  | -    | mA    |
|  | AGC_CTRL = 1.0V        | A                      | 25        | -    | 0.04  | -    | mA    |
| PIN_O_IBIAS Leakage current  | AGC_CTRL = 0.5V        | A                      | 25        | -    | 0.0   | -    | mA    |
| PIN_O_IBIAS Current Vs Temperature   | AGC_CTRL = 1.8V        | B                      | 25        | -    | 200   | -    | μA/°C |
| PIN_O_IBIAS Current Vs Supply Voltage  | AGC_CTRL = 1.8V        | B                      | 25        | -    | 330   | -    | μA/V  |
| <b>POWER SUPPLY AND LOGIC SPECIFICATIONS</b>   |                        |                        |           |      |       |      |       |
| Supply Voltage   |                        | B                      | 25        | 2.7  | -     | 3.3  | V     |
| LNA Power supply (VLNA)  |                        | C                      | 25        | 2.7  | -     | 5.5  | V     |
| SEL And RX_PE, V <sub>IL</sub>   |                        | A                      | 25        | -    | -     | 0.8  | V     |
| SEL And RX_PE, V <sub>IH</sub>   |                        | A                      | 25        | 2.0  | -     | -    | V     |
| SEL AND RX_PE, Input Bias Currents at V <sub>CC</sub> = 3.0V                           | VIH = 3.0V             | A                      | 25        | -200 | -     | +200 | μA    |
|  | VIL = 0.0V             | A                      | 25        | -200 | -     | +200 | μA    |
| LNA/Mixer Supply Current   | AGC_CTRL = 0.5V        | A                      | 25        | -    | 45    | -    | mA    |
| Total PIN Diode Bias Circuit Supply Current  | AGC_CTRL = 1.8V        | B                      | 25        | -    | 11    | -    | mA    |
| Power Down Supply Current  | RX_PE = Low            | A                      | 25        | -    | 10    | 100  | μA    |
| Power Down Speed   |                        | B                      | 25        | -    | -     | 10   | μs    |

**NOTES:**

2. A = Production Tested, B = Based on Characterization, C = By Design
3. Output differential to single end match network to 50Ω for both CDMA and FM IF ports (Production Test Diagram in page 5).

# HFA3665

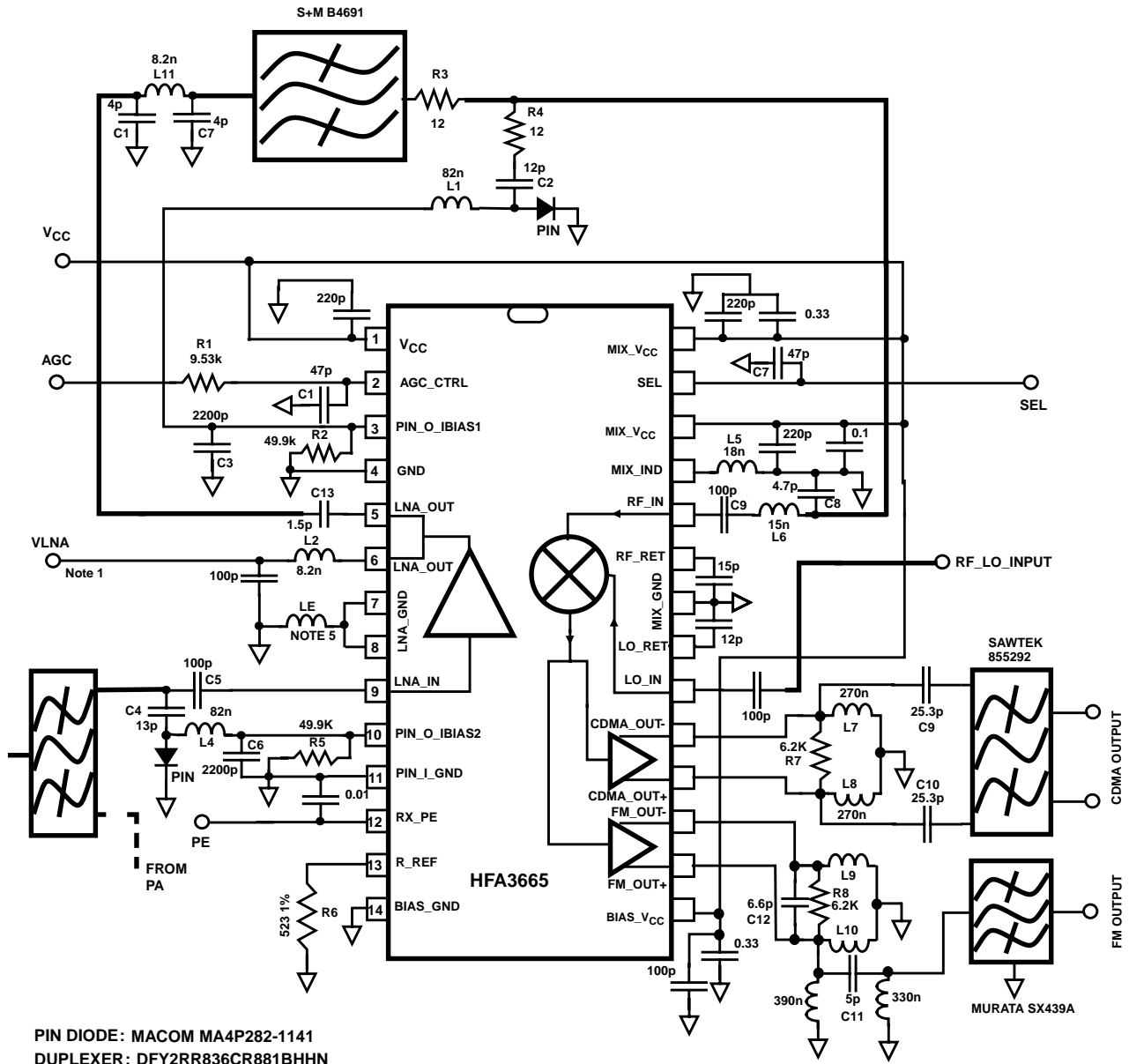
## Production Test Diagram



**NOTE:**

- PC trace degeneration inductor. 93mil by 8mil trace terminating in a 10mil via. Via is tied to a buried solid ground plane 12mils deep. Material is FR4 Er = 4.7.

# Typical RF Front End AGC Application Diagram



**NOTE:**

- 5. LNA degeneration inductance built with a PC trace to ground in combination with VLNA power supply to improve IIP3. A transmission line inductance of 1.2nH at 882MHz to a solid ground plane is typical (see Test Diagram).

## DESIGN INFORMATION

### **External AGC Application Components Description**

**(Please refer to Typical RF and Front End AGC Application Diagram)**

NOTE: In order to avoid input insertion losses and maintain the Noise Figure of this application optimized, the VSWR of the LNA input attenuator scheme is directly impacted by the input shunt PIN diode impedance when AGC is in action. This mismatch is absorbed by the duplexer/filter and there is no significant impact in its duplex characteristics to both antenna and transmitter ports.

**R3 and R4** limit the output attenuation range and output VSWR.

**R1** sets the scale factor, temperature coefficient and range of the gain control voltage.

**R2** sets the turn-on point for the output PIN diode attenuator and **R5** sets the turn-on point for the input PIN diode attenuator by shunting to ground some of the PIN diode bias current. By making R5 a smaller value than R2, the output attenuator turns on first, to optimize NF. Making R5 = R2 will turn both PIN diodes simultaneously to optimize the IIP3 during the initial AGC action. The R2/R5 combination can be tailored to specific AGC characteristics.

**R6** generates the reference current which is used to set the operating point of all the major RF and IF transistors. A proportional to temperature (PTAT) voltage of about 37mV at 25°C is applied to this resistor. PTAT biasing keeps the gain temperature independent. A 10% variation from 523Ω is allowed. Lower values increase the total LNA and Mixer bias currents.

**C1** filters noise from the gain control source to reduce unwanted AM modulation.

**C2 and C4** provide DC isolation for PIN diode biasing. Their values are chosen to provide series resonance cancelling of the diode package and PC board inductances.

**C3 and C6** decouple the PIN diode bias pins. Failure to decouple these pins may cause LNA oscillations.

**LE** adds degeneration to the LNA input for higher input intercept points. This combination of degeneration and a higher LNA  $V_{CC}$  (VLNA) improves considerably the input intercept point with a slight decrease in gain. LE shall have very high Q and can be built with a small PC trace.

**L1 and L4** permit DC biasing of the PIN diodes and RF isolation. Several types of 82nH inductors have SRF near 900MHz thus maximizing the RF isolation.

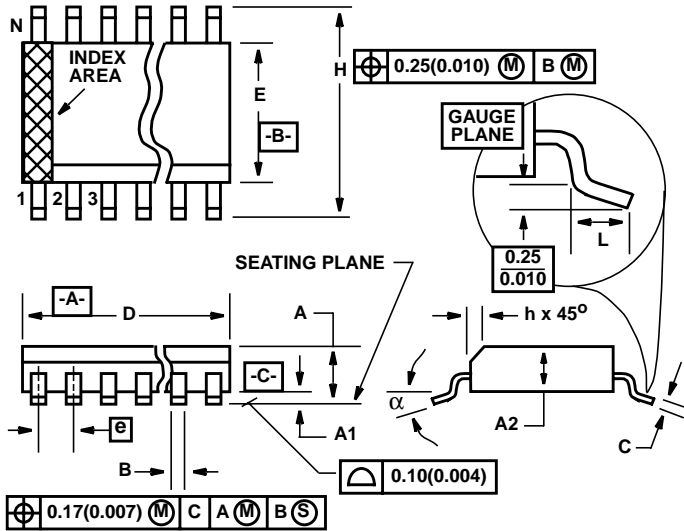
**L2 and C13** are part of the output matching network and provides the DC bias path for the open collector output.

**R7 and R8** define the Real part of the CDMA and FM output ports impedances. Unloaded "Q" of the coils used for proper biasing of these ports have to be taken into account when defining these values. The total load presented to these ports also define the achievable gain of the mixers. Because there is no internal feedback between the complementary ports of the differential channel, the loads and ports can be split into independent ports referenced to ground.

**L7, L8 and L9, L10** have two functions: They provide a DC path to ground required for proper operation of the CDMA and FM differential outputs and can also be part of the match network between these ports and IF filters. **C9, C10 and C12** are part of a match network to the suggested filters. **L9, L10 and C12** are part of a current summer network for a differential to single end conversion. **L12, L13 and C11** form a high "Q" match network between the converter and the suggested filter for the SAW IP3 distortion optimization.

All other unlabeled components on the schematics are bypass/decoupling capacitors. Values are chosen based on their SRF.

**Shrink Small Outline Plastic Packages (SSOP)**



**M28.15**  
**28 LEAD SHRINK NARROW BODY SMALL OUTLINE**  
**PLASTIC PACKAGE**

| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN       | MAX    | MIN         | MAX   |       |
| A      | 0.053     | 0.069  | 1.35        | 1.75  | -     |
| A1     | 0.004     | 0.010  | 0.10        | 0.25  | -     |
| A2     | -         | 0.061  | -           | 1.54  | -     |
| B      | 0.008     | 0.012  | 0.20        | 0.30  | 9     |
| C      | 0.007     | 0.010  | 0.18        | 0.25  | -     |
| D      | 0.386     | 0.394  | 9.81        | 10.00 | 3     |
| E      | 0.150     | 0.157  | 3.81        | 3.98  | 4     |
| e      | 0.025 BSC |        | 0.635 BSC   |       | -     |
| H      | 0.228     | 0.244  | 5.80        | 6.19  | -     |
| h      | 0.0099    | 0.0196 | 0.26        | 0.49  | 5     |
| L      | 0.016     | 0.050  | 0.41        | 1.27  | 6     |
| N      | 28        |        | 28          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    | -     |

Rev. 0 2/95

**NOTES:**

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
- Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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