Data Sheet | October 1998 | File Number 4356.1

10-Bit, 125 MSPS D/A Converter

The HI3197 is a high-speed D/A converter which can perform the multiplexed input of the two system 10-bit data. The maximum conversion rate achieves 125 MSPS. The multiplexed operation is possible by the 1/2 frequency-divided clock or by halving the frequency of the clock with the clock frequency divider circuit having the reset pin in the IC. The data input is TTL; the clock input pin and reset input pin can select either TTL or PECL according to the application.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3197JCQ	-20 to 75	48 Ld MQFP/ PQFP	Q48.7x7-S

Features

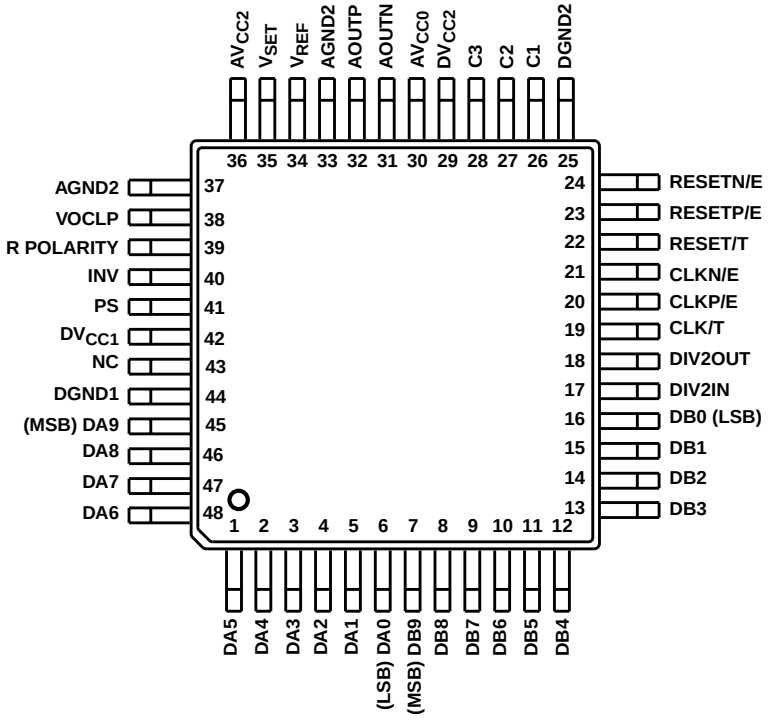
- Resolution . . . . . 10 Bits
- Conversion Rate . . . . . 125 MSPS (PECL) 100 MSPS (TTL)
- Data Input Level . . . . . TTL
- Low Power Consumption . . . . . 400mW (Typ)
- Low Glitch Energy . . . . . 1.5pV•s
- Clock, Reset Input Level: TTL and PECL Compatible 2:1 Multiplexed Input Function
- $^{1}/_{2}$ Frequency-Divided Clock Output Possible by the Built-In Clock Frequency Divider Circuit
- Voltage Output (50Ω Load Drive Possible)
- Single Power Supply or ±Dual Power Supplies
- Polarity Switching Function of Reset Signal

Applications

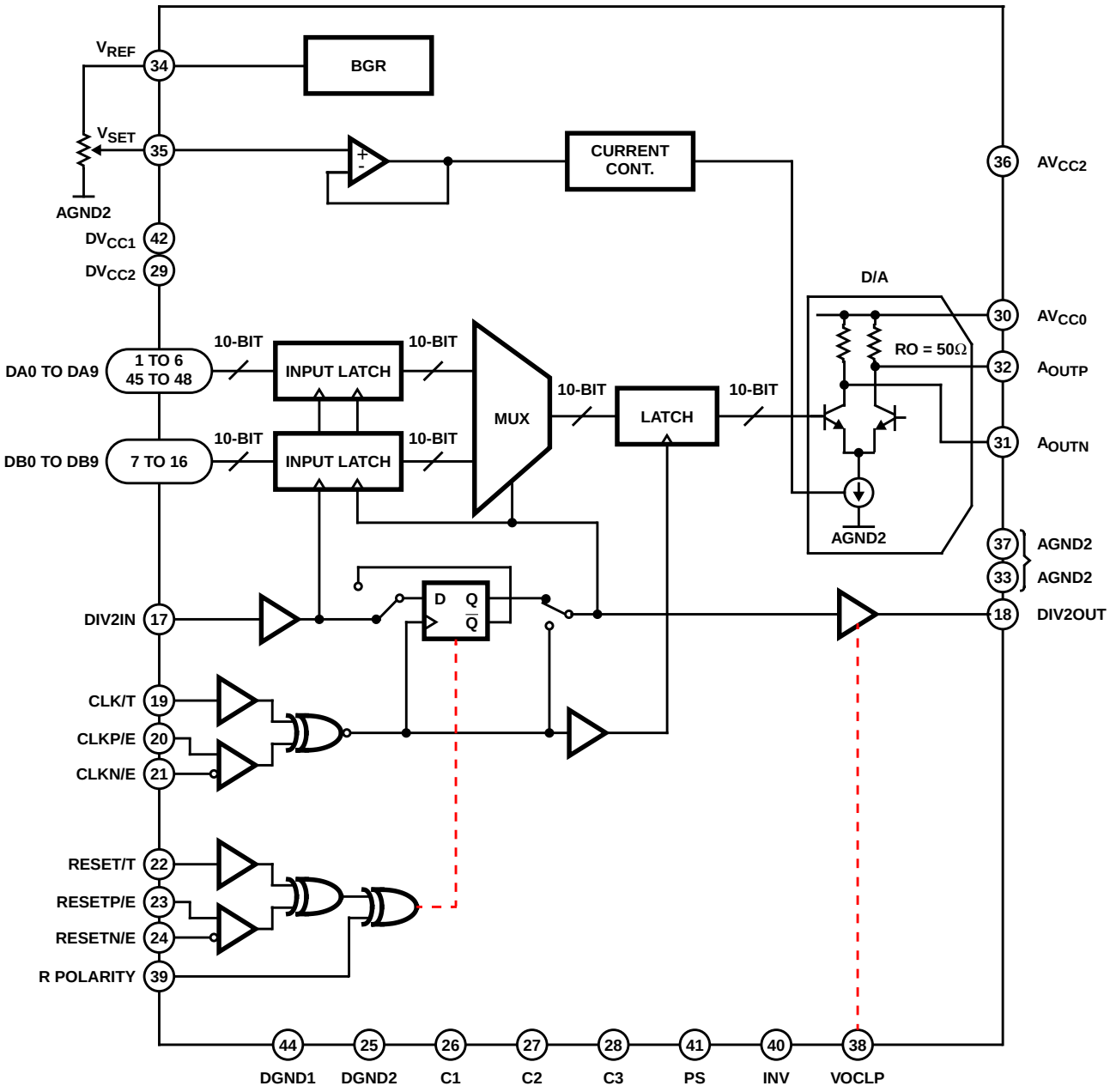
- LCD
- DDS
- HDTV
- Communications (QPSK, QAM)

Pinout

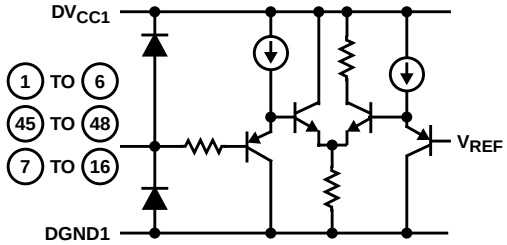
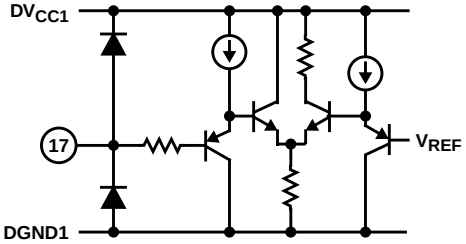
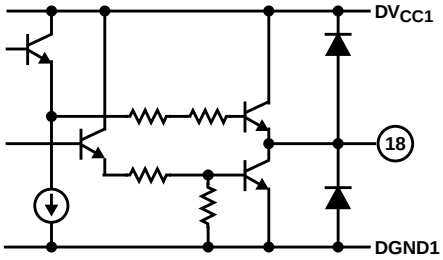
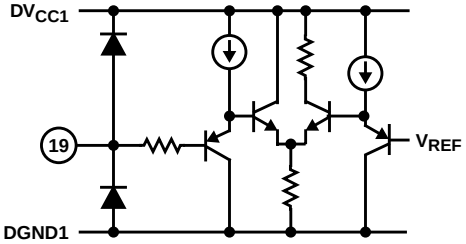
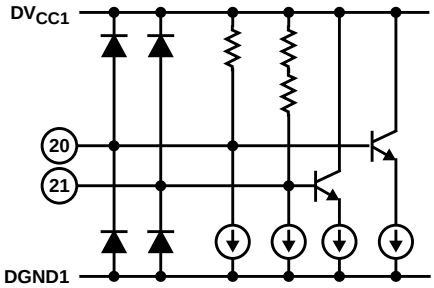
HI3197 (MQFP)
TOP VIEW



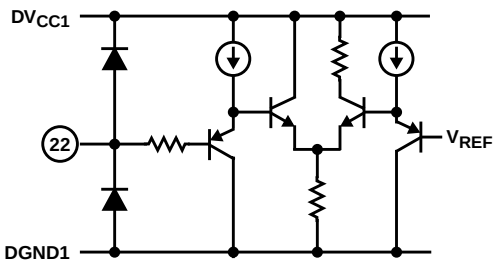
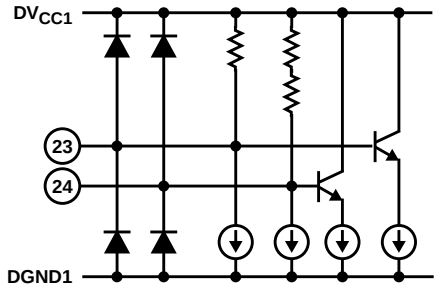
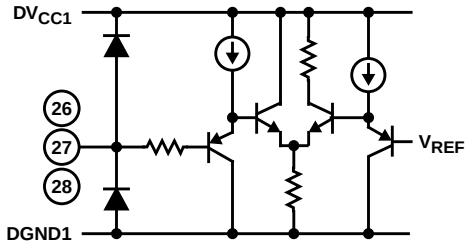
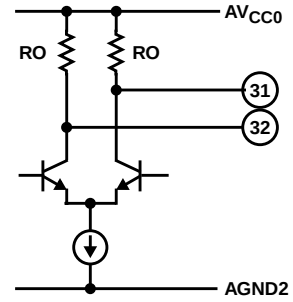
Block Diagram



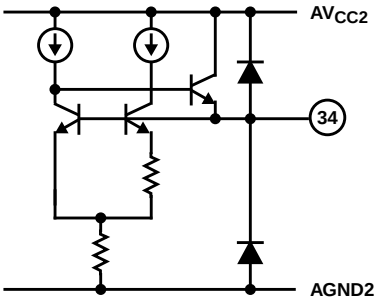
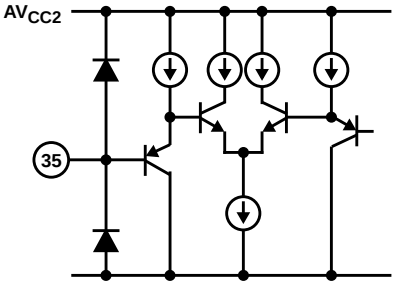
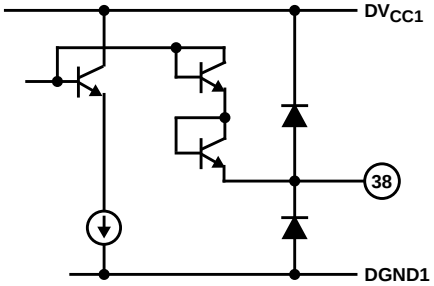
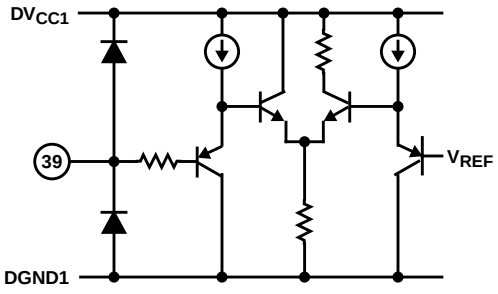
Pin Descriptions and I/O Pin Equivalent Circuits

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 6 45 to 48	DA0 to DA9	I	TTL		Side A Data Input.
7 to 16	DB0 to DA9	I	TTL		Side B Data Input.
17	DIV2IN	I	TTL		$^1/_2$ Frequency-Divided Clock Input. Use this pin for MUX.1A or MUX.2 mode. Leave open for other modes.
18	DIV2OUT	O	TTL		$^1/_2$ Frequency-Divided Clock Output. The signal with the $^1/_2$ frequency divided clock (DIV2OUT) is output for MUX.1A mode. Leave open for other modes.
19	CLK/T	I	TTL		Clock Input. Use this pin when the clock is input in the TTL level. At this time, leave Pins 20 and 21 open.
20	CLKP/E	I	PECL		Clock Input. Use this pin when the clock is input in PECL level. At this time, leave Pin 19 open.
21	CLKN/E	I	PECL		CLKP/E Complementary Input. When left open, this pin goes to the threshold potential. Operation is possible only with CLKP/E, but complementary input is recommended to attain fast and stable operation.

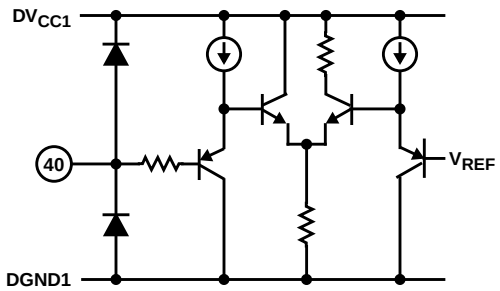
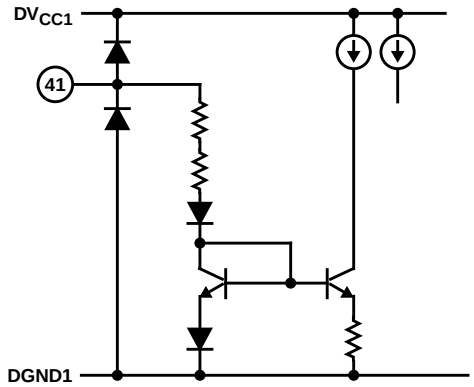
Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
22	RESET/T	I	TTL		Reset signal input. When the multiple HI3197 are operated at a time for MUX.1A or MUX.1B mode, the start timing of the internal $^1/_2$ frequency divider circuits should be matched. At this time, the reset signal is used; when the reset signal is the TTL level, Pin 22 is used and Pins 23 and 24 are left open. When the reset signal is the PECL level, Pins 23 and 24 are used and Pin 22 is left open. For the PECL level, operation is possible only with RESETP/E as with the case for the clock. The reset signal polarity can be set by Pin 39 (RPOLARITY). Leave the reset pin open when the other modes are used.
23	RESETP/E	I	PECL		
24	RESETN/E	I	PECL		
25	DGND2		Single Power Supply: GND Dual Power Supplies: -5V		Digital Power Supply.
26	C1	I	TTL		Function setting.
27	C2	I	TTL		
28	C3	I	TTL		
29	DV_{CC2}		Single Power Supply: +5V Dual Power Supplies: GND		Digital Power Supply.
30	AV_{CC0}				Analog Output Power Supply.
31	OUTN	O	AV_{CC0} - V_{FS}		D/A Negative Output. The inversion of the D/A positive output pin is output. Terminate the inversion without pin with 50Ω when the inversion output is not used and the positive output is terminated with 50Ω.
32	AOUTP	O	AV_{CC0} - V_{FS}		D/A positive output.
33	AGND2		Single Power Supply: GND Dual Power Supplies: -5V		Analog Ground.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
34	V_{REF}	O	AGND +1.2V		Analog Reference Voltage Output.
35	V_{SET}	I	AGND2 + 0.7V to AGND2 + 1.03V		Full scale adjustment.
36	AV_{CC2}		Single Power Supply: +5V Dual Power Supplies: GND		Analog Power Supply.
37	AGND2		Single Power Supply: GND Dual Power Supplies: -5V		Analog Power Supply
38	VOCLP	I	Clamp Voltage		TTL Output High Level Clamp. The TTL level signal is output from the DIV2OUT pin for MUX.1A mode. The TTL high level voltage is clamped to the value approximately equivalent to the voltage supplied to this pin. Leave the VOCLP pin open for other modes.
39	P Polarity	I	TTL		Reset signal polarity switching. At high level, the reset polarity is active high; at low level, active low.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
40	INV	I	TTL		Analog Output polarity inversion. The analog output is inverted at low level.
41	PS	I	TTL		Power saving. Power saving at low level. Normally pull up the PS pin to high level as this pin is open low.
42	DV_{CC1}		5V		Digital Power Supply.
43	NC				No connection.
44	DGND1		0V		Digital Ground.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{CC0}, AV_{CC2}, DV_{CC2}) . . . . . -0.5 to +7.0V
AGND2, DGND2 . . . . . -7.0 to +0.5V
DV_{CC1} . . . . . -0.5 to +7.0V
AV_{CC2} - AGND2 . . . . . -0.5 to +7.0V
AV_{CC0} - AGND2 . . . . . -0.5 to +7.0V
DV_{CC2} - DGND2 . . . . . -0.5 to +7.0V
Input Voltage
V_{SET}, ... AGND2 -05 to AV_{CC2} + 0.5V
TTL Pin . . . . . DGND1 -0.5 to DV_{CC1} + 0.5V
PECL Pin, ... DGND1 -0.5 to DV_{CC1} + 0.5V
PS. . . . . DGND1 -0.5 to DV_{CC1} + 0.5V
(Others), VOCLP . . . . . DGND1 -0.5 to DV_{CC1} + 5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 70
Maximum Power Dissipation, P_D 1.4W
(When mounted on a glass fabric base epoxy board with 76mm x 114mm, 1.6mm thick)
Maximum Junction Temperature (Hermetic Package or Die) . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range, T_{STG} . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
AV_{CC0}, AV_{CC2}	+4.75	+5.0	+5.25V
AGND2	-0.05	0	+0.05V
DV_{CC1}	+4.75	+5.0	+5.25V
DGND1	-0.05	0	+0.05V
DV_{CC2}	-4.75	+5.0	+5.25V
DGND2	-0.05	0	+0.05V

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
AV_{CC0}, AV_{CC2}	-0.05	0	+0.05V
AGND2	-5.50	-5.0	-4.75V
DV_{CC1}	4.75	5.0	+5.25V
DGND1	-0.05	0	+0.05V
DV_{CC2}	-0.05	0	+0.05V
DGND2	-5.50	-5.0	-4.75V

Recommended Operating Conditions (Applying to Single and Dual Power Supplies)

	MIN	TYP	MAX
Analog Input Voltage, V_{SET}	AGND2 + 0.7	-	AGND2 + 1.03V
Digital Input Voltage			
PECL, V_{IH}	DGND1 + 2.6		DV_{CC1}
PECL, V_{IL}	-	V_{IH} - 0.8	V_{IH} - 0.4V
TTL, V_{IH}	DGND1 + 2.0	-	-
TTL, V_{IL}	-	-	DGND1 + 0.8V
PS, V_{IH}	DGND1 + 2.0	-	-
PS, V_{IL}	-	-	DGND1 + 0.8V
Other, V_{OCLP}	DGND1 + 2.7	-	DV_{CC1}

Ambient Temperature (T_A) . . . . . -20^oC to 75^oC
Clock Pulse Width
t_{PW1} . . . . . 4ns (Min)
t_{PW0} . . . . . 4ns (Min)

	MIN	TYP	MAX
Load Resistance, R_L	50	50	≥10kΩ
Analog Output Full Scale Voltage			
$R_L \geq 10k\Omega$, V_{FS}	1.5	2.0	2.2V
$R_L = 50\Omega$, V_{FS}	0.75	1.0	1.2V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	n		-	10	-	Bit
Maximum Conversion Rate	f_{CECL}	PECL Operation	-	-	125	MSPS
	f_{CTTL}	TTL Operation	-	-	100	MSPS
Integral Linearity Error	INL	V_{FS} = 1V	-	-	±1.2	LSB
Differential Linearity Error	DNL		-	-	-0.85 to 0.5	LSB
	DNL	AOUTP Transitions from 0000111111 - 0001000000	-	-	-1.2 to 0.5	LSB
	DNL	AOUTN Transitions from 1111000000 - 1110111111	-	-	-1.2 to 0.5	LSB
ANALOG OUTPUT						
Output Full-Scale Voltage	V_{FS}	$R_L = 50\Omega$	0.75	1	1.05	V
		$R_L \geq 10k\Omega$	1.5	2.0	2.2	V
Compliance Voltage $V_{OC(MIN)}$: $(AV_{CC0}-V_{FS} - DV_{CC2}) \geq -2.V$, $V_{OC(MAX)}$: $(AV_{CC0}-V_{OF} - DV_{CC2}) \geq 1.5$	V_{OC}	Measured to DV_{CC2}	-2.1	-	1.5	V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Zero Offset Voltage	V_{OF}	$R_L \geq 10k\Omega$, V_{SET} = AGND2 + 0.9375V	0	-	20	mV
		$R_L = 50\Omega$, V_{SET} = AGND2 + 0.9375V	0	-	10	mV
Output Resistance	R_O		-	50	-	Ω
Output Capacitance	C_O		-	10	-	pF
Absolute Amplitude Error	EG	V_{SET} = AGND2 + 0.9375V	-4	-	4	% of FS
Absolute Amplitude Error Temperature Characteristics	TCG	V_{FS} = 1V at 25°C	-	-	60	ppm/°C
Analog Output Rise Time	t_r	$R_L = 50\Omega$, V_{FS} = 1V, 10 - 90%	0.85	-	1.05	ns
Analog Output Fall Time	t_f		0.75	-	0.85	ns
Settling Time	t_{SET}		-	-	3.5	ns
Glitch Energy	GE		-	1.5	5.0	pVS
REFERENCE						
V_{REF} Pin Voltage	V_{REF}	I_{REF} = 1mA	AGND2+1.18	AGND2+1.25	AGND2+1.32	V
V_{REF} Temperature Drift			-	-	250	ppm/°C
V_{REF} Multiplying Bandwidth		$100mV_{P-P}$ Sinewave at -3dB	50	-	-	MHz
Digital Input (TTL Pin)	V_{IH}		2	-	-	V
	V_{IL}		-	-	0.8	V
	V_{TH}		-	1.5	-	V
	I_{IH}	V_{IH} = 3.5V	-1	-	1	µA
	I_{IL}	V_{IL} = 0.2V	-2	-	0	µA
Digital Output (DIV2OUT TTL Pin)	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
	I_{OZ}	V_O = 5V	10	-	100	µA
	I_{OZ}	V_O = 0V	-1	-	1	µA
	t_r	0.8 to 2.4V (C_L = 10pF)	1.0	-	1.5	ns
	t_f	2.4 to 0.8V (C_L = 10pF)	0.6	-	1.2	ns
Digital Input (PECL Pin)	V_{IH}		DV_{CC1} - 1.5	-	DV_{CC1} - 0.5	V
	V_{IL}		DV_{CC1} - 3.2	-	DV_{CC1} - 1.4	V
	I_{IH}	$V_{IH} = DV_{CC1}$ - 0.8V	0	-	20	µA
	I_{IL}	$V_{IL} = DV_{CC1}$ - 1.5V	-30	-	0	µA
Digital Input Current (PS)	V_{IH}		2	-	-	V
	V_{IL}		-	-	0.8	V
	I_{IH}	V_{IH} = 3.5V	-1	-	100	µA
	I_{IL}	V_{IL} = 0.2V	-1	-	0	µA
Clamp Pin Input Current (V_{OCLP})	I_{CCLP}	$V_{CCLP} = DV_{CC1}$	-	-	5	µA
	I_{CCLP}	V_{CCLP} = 2.4V	-60	-	-10	µA
Digital Input Capacitance	C_{IN}		-	3	5	pF
CURRENT CONSUMPTION						
Supply Current (Operating)	I_{CC}	Total Operating	63	96	129	mA
	DI_{CC1}		7	15.5	24	mA
	DI_{CC2}		13	19	25	mA
	AI_{CC2}		6	8.5	11	mA
	AI_{CC0}		37	53	68	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (PS Mode)	I_{CC}	Power Saving Mode	-	0.432	4	mA
NOTE: The current consumption in power saving mode does not include the voltage reference (V_{REF}) current. When using the internal reference the additional current I_{REF} = V_{REF} / R_{REF} should be added to the table values for an accurate estimate of total standby current.	DI_{CC1}	Power Saving Mode	-	0.38	1.5	mA
	DI_{CC2}	Power Saving Mode	-	0.001	0.2	mA
	AI_{CC2}	Power Saving Mode	-	0.05	0.3	mA
	AI_{CC0}	Power Saving Mode	-	0.001	2	mA

AC Specifications MUX.1A and MUX.1B Modes

	CLK SIGNAL LEVEL		PECL			TTL			PECL			
	RESET SIGNAL LEVEL		PECL			TTL			TTL			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MUX.1A MODE												
Maximum Conversion Rate	f_C		125	-	-	100	-	-	125	-	-	MSPS
Clock High Pulse Width	t_{PW1}		3.5	-	-	4.5	-	-	3.5	-	-	ns
Clock Low Pulse Width	t_{PW0}		3.5	-	-	3.0	-	-	3.5	-	-	ns
Reset Signal Setup Time	t_{S-RST}		0	-	-	1.0	-	-	4.0	-	-	ns
Reset Signal Hold Time	t_{H-RST}		1.0	-	-	3.0	-	-	0	-	-	ns
DIV2OUT Output Delay	t_{D-DIV}	C_L = 10pF	5.5	6.5	8	8.0	9.5	12.0	5.5	6.5	8	ns
DIV2OUT to DIV2IN Maximum Delay Time	2T-tm		-	-	2T - 7	-	-	2T - 7	-	-	2T - 7	ns
Data Input Setup Time	t_S		1.0	-	-	1.0	-	-	1.0	-	-	ns
Data Input Hold Time	t_H		5.0	-	-	5.0	-	-	5.0	-	-	ns
Analog Output Pipeline Delay	t_{PD} (A)		-	4	-	-	4	-	-	4	-	CLK
	t_{PD} (B)		-	5	-	-	5	-	-	5	-	CLK
Analog Output Delay	t_{DO}		5.0	5.5	6.0	6.5	7.5	8.5	5.0	5.5	6.0	ns
MUX.1B MODE												
Maximum Conversion Rate	f_C		125	-	-	100	-	-	125	-	-	MSPS
Clock High Pulse Width	t_{PW1}		3.5	-	-	4.5	-	-	3.5	-	-	ns
Clock Low Pulse Width	t_{PW0}		3.5	-	-	3.0	-	-	3.5	-	-	ns
Reset Signal Setup Time	t_{S-RST}		0	-	-	1.0	-	-	4.0	-	-	ns
Reset Signal Hold Time	t_{H-RST}		1.0	-	-	3.0	-	-	0	-	-	ns
Data Input Setup Time	t_S		1.0	-	-	1.0	-	-	1.0	-	-	ns
Data Input Hold Time	t_H		4.0	-	-	6.0	-	-	4.0	-	-	ns
Analog Output Pipeline Delay	t_{PD} (A)		-	2	-	-	2	-	-	2	-	CLK
	t_{PD} (B)		-	3	-	-	3	-	-	3	-	CLK
Analog Output Delay	t_{DO}		5.0	5.5	6.0	6.5	7.5	8.5	5.0	5.5	6.0	ns

AC Specifications MUX.2, SEL.A, and SEL.B Modes

	CLK SIGNAL LEVEL		PECL			TTL			
	RESET SIGNAL LEVEL		(NOTE 2)			(NOTE 2)			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MUX.2 MODE									
Maximum Conversion Rate	f_C		125	-	-	100	-	-	MSPS
Clock High Pulse Width	t_{PW1}		3.5	-	-	4.5	-	-	ns
Clock Low Pulse Width	t_{PW0}		3.5	-	-	3.0	-	-	ns
DIV2IN Signal Setup Time	t_{S-DIV}		4.5	-	-	2.0	-	-	ns

AC Specifications MUX.2, SEL.A, and SEL.B Modes

PARAMETER	CLK SIGNAL LEVEL / RESET SIGNAL LEVEL SYMBOL	CONDITIONS	PECL (NOTE 2) MIN	PECL TYP	PECL MAX	TTL (NOTE 2) MIN	TTL TYP	TTL MAX	UNITS
DIV2IN Signal Hold Time	t_{H-DIV}		0	-	-	3.5	-	-	ns
Data Input Setup Time	t_S		1.0	-	-	1.0	-	-	ns
Data Input Hold Time	t_H		5.0	-	-	5.0	-	-	ns
Analog Output Pipeline Delay	t_{PD} (A)		-	2	-	-	2	-	CLK
	t_{PD} (B)		-	3	-	-	3	-	CLK
Analog Output Delay	t_{DO}		5.0	5.5	6.0	6.5	7.5	8.5	ns
SEL. A, SEL. B MODES									
Maximum Conversion Rate	f_C		125	-	-	100	-	-	MSPS
Clock High Pulse Width	t_{PW1}		3.5	-	-	4.5	-	-	ns
Clock Low Pulse Width	t_{PW0}		3.5	-	-	3.0	-	-	ns
C2 Signal Setup Time	t_{S-C2}		1.0	-	-	1.0	-	-	ns
C2 Signal Hold Time	t_{H-C2}		2.5	-	-	3.5	-	-	ns
Data Input Setup Time	t_S		1.0	-	-	1.5	-	-	ns
Data Input Hold Time	t_H		2.0	-	-	3.5	-	-	ns
Analog Output Pipeline Delay	t_{PD} (A)		-	1	-	-	1	-	CLK
	t_{PD} (B)		-	1	-	-	1	-	CLK
Analog Output Delay	t_{DO}		5.0	5.5	6.0	6.5	7.5	8.5	ns

NOTE:

2. The RESET signal is not input in MUX.2, SEL. A, or SEL. B modes.

Electrical Characteristics Measurement Circuits

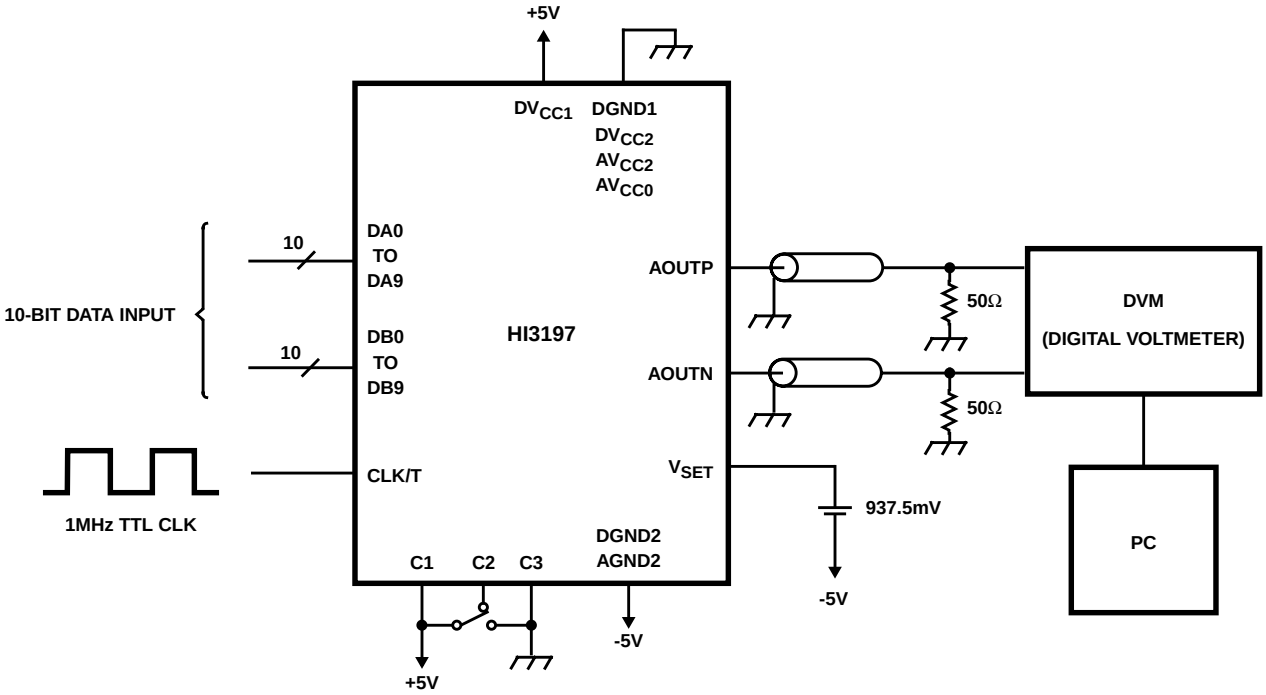


FIGURE 1. DIFFERENTIAL LINEARITY ERROR, INTEGRAL LINEARITY ERROR

Electrical Characteristics Measurement Circuits (Continued)

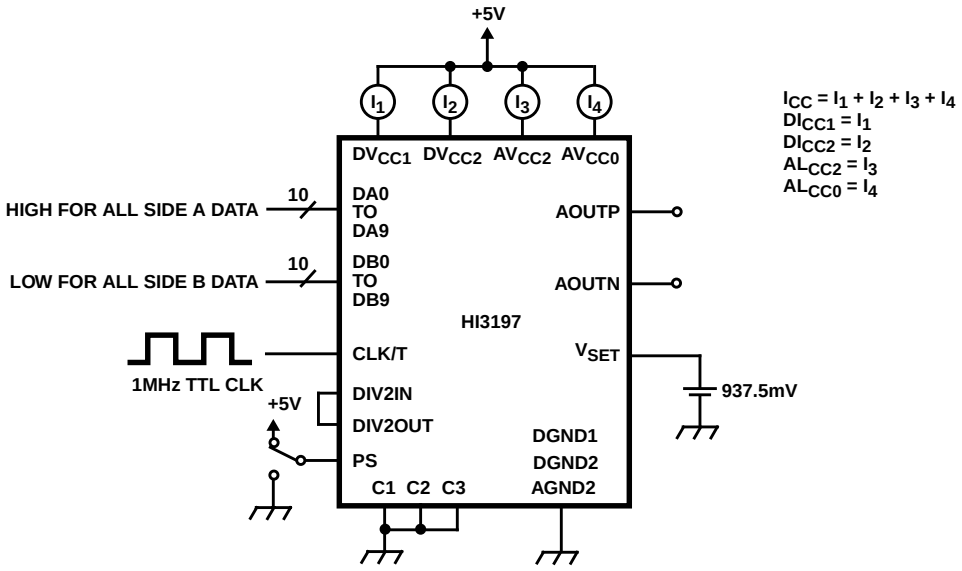


FIGURE 2. CURRENT CONSUMPTION

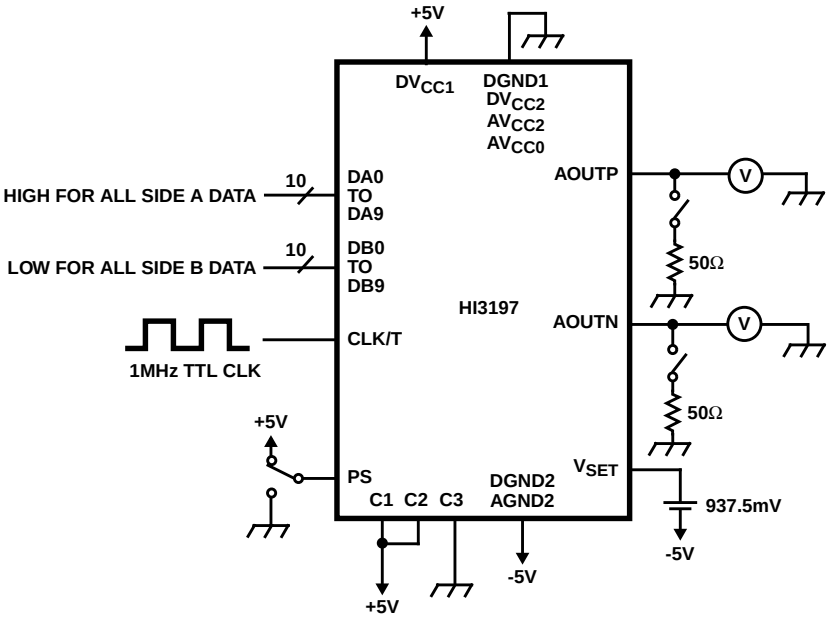


FIGURE 3. ANALOG OUTPUT CHARACTERISITCS, OUTPUT FULL-SCALE ABSOLUTE AMPLITUDE ERROR, OUTPUT ZERO OFFSET VOLTAGE

Electrical Characteristics Measurement Circuits (Continued)

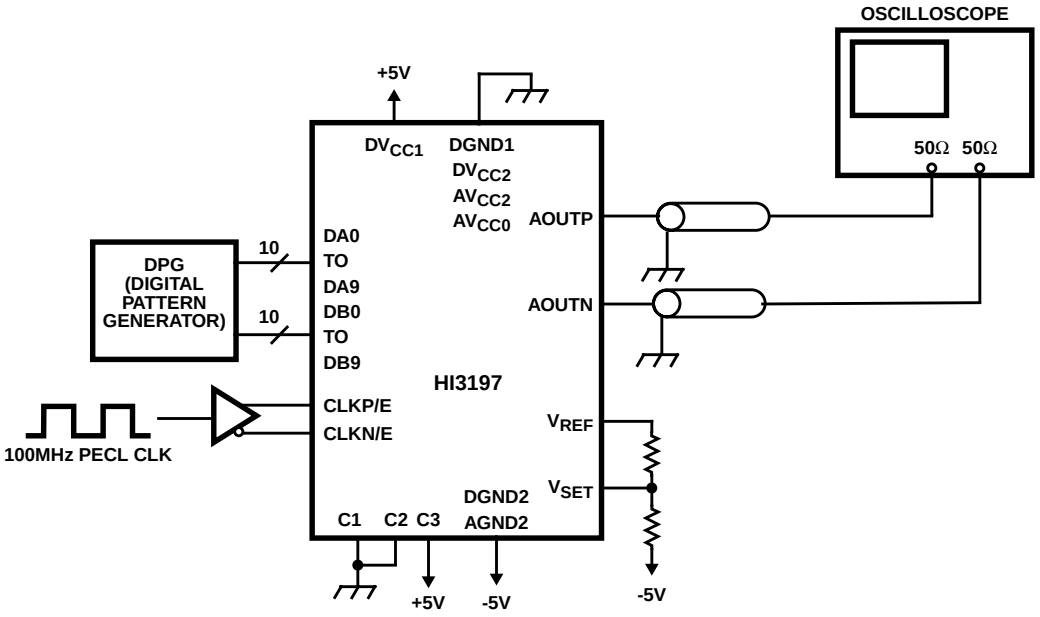


FIGURE 4. ANALOG OUTPUT RISE TIME, ANALOG OUTPUT FALL TIME, SETTLING TIME AND GLITCH ENERGY

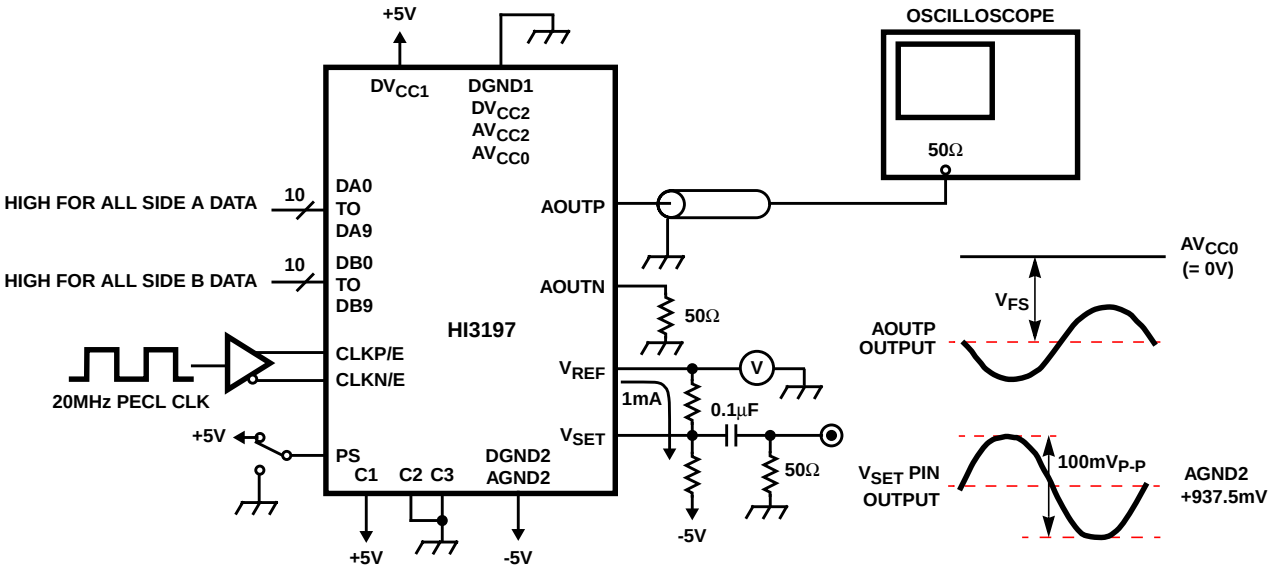


FIGURE 5. REFERENCE/CONTROL AMPLIFIER CHARACTERISITCS, V_{REF} PIN OUTPUT VOLTAGE, V_{REF} PIN OUTPUT VOLTAGE IN POWER SAVING MODE, MULTIPLYING BANDWIDTH

Electrical Characteristics Measurement Circuits (Continued)

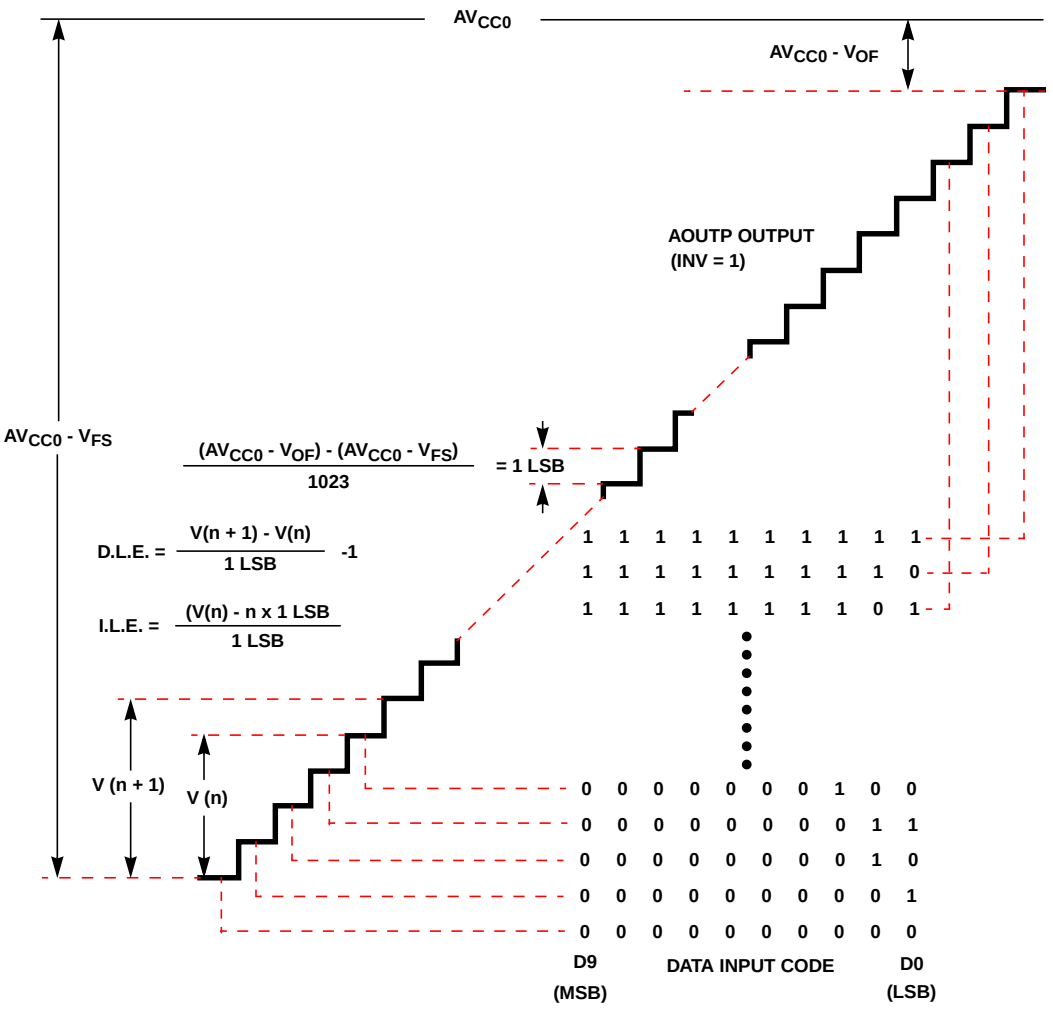


FIGURE 6.

TABLE 1. I/O CORRESPONDENCE TABLE

DATA INPUT CODE				ANALOG OUTPUT LEVEL	
INV = 1		INV = 0			
(MSB) D9	(LSB) D0	(MSB) D9	(LSB) D0	AOUTP	AOUTN
1111111111		0000000000		$AV_{CC0} - V_{OF}$	$AV_{CC0} - V_{FS}$
⋮		⋮		⋮	⋮
0000000000		1111111111		$AV_{CC0} - V_{FS}$	$AV_{CC0} - V_{OF}$

Description of Operation

The HI3197 has four types of operation modes to support various applications. The operation mode is set by switching the function setting pins (C1, C2 and C3).

The HI3197 can input data divided into two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplex the data, and output it as an analog signal, making it possible to halve the data rate. This lets the HI3197 support the TTL data input level in contrast to the ECL data input level for conventional high-speed D/A converters. The clock signal and reset signal input levels can be selected from either TTL or PECL according to the application. (However, setting both signals to either TTL or PECL input level is recommended.)

MUX.1A Mode

Set C1, C2 and C3 all Low for this mode.

In MUX.1A mode, the frequency of the clock input from the clock input pin is halved internally, and the 1/2 frequency-divided signal is output at TTL level from the DIV2OUT pin. Data synchronized with the DIV2OUT signal (the signal output from the DIV2OUT pin) can be obtained by operating the HI3197 front-end system with the DIV2OUT signal. The timing at which the data output delay of the HI3197 front-end system matches with the hold time during HI3197 data input can be easily set by inputting this synchronized data to the data input pins and the DIV2OUT signal to the DIV2IN pin. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplexed, and extracted as analog output.

When using the multiple HI3197 in MUX.1A mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in Figure 7. As a countermeasure, the MUX.1A mode has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See Figure 7 for the detailed timing.

TABLE 2. OPERATING MODES

MODE	C1	C2	C3	CLK IN (MSPS)	DATA IN (Mbps)	AOUT (Mbps)	DIV2OUT PIN	DESCRIPTION OF OPERATION
MUX.1A	0	0	0	125	62.5	125	Outputs CLK/2 at TTL Level	MUX Operation by the Internal CLK/2
MUX.1B	0	0	1	125	62.5	125	High Impedance	MUX Operation by the Internal CLK/2
MUX.2	0	1	0	125	62.5	125	High Impedance	MUX Operation by DIV2IN
SELE.A	1	0	0	125	125	125	High Impedance	D/A Conversion of Side A Data Input
SELE.B	1	1	0	125	125	125	High Impedance	D/A Conversion of Side B Data Input

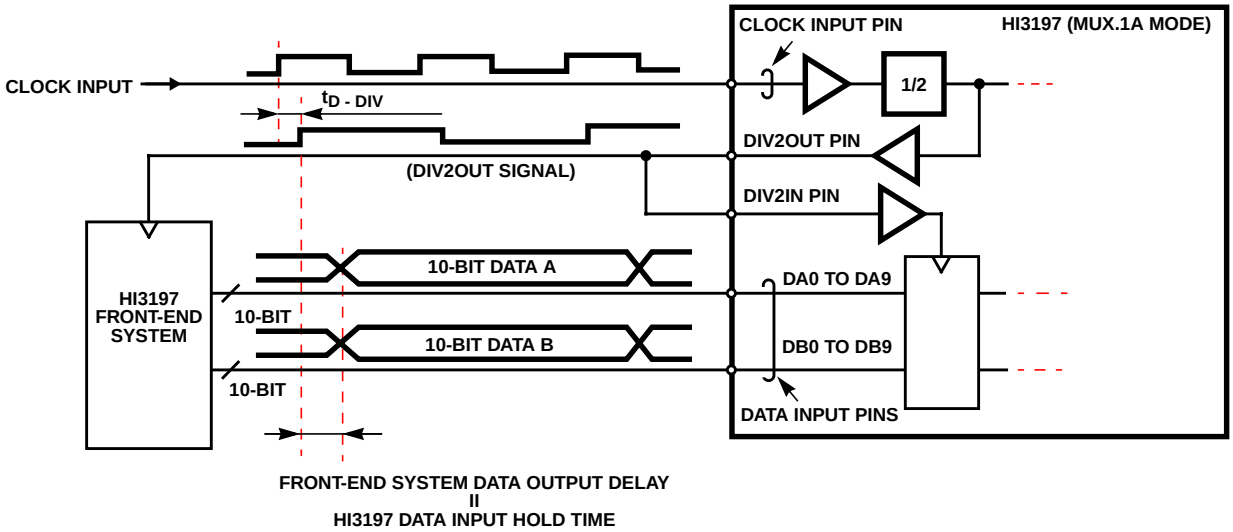


FIGURE 7A. MUX.1A

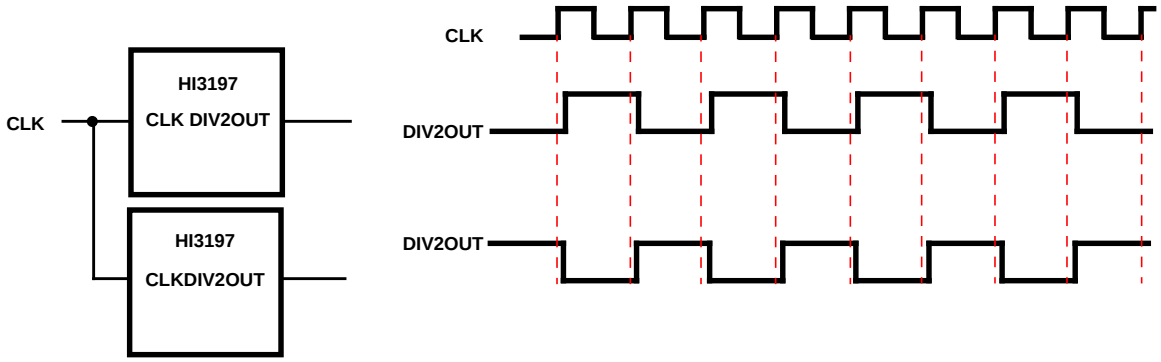


FIGURE 7B. MUX.1A EXAMPLE WHEN NOT USING THE RESET SIGNAL

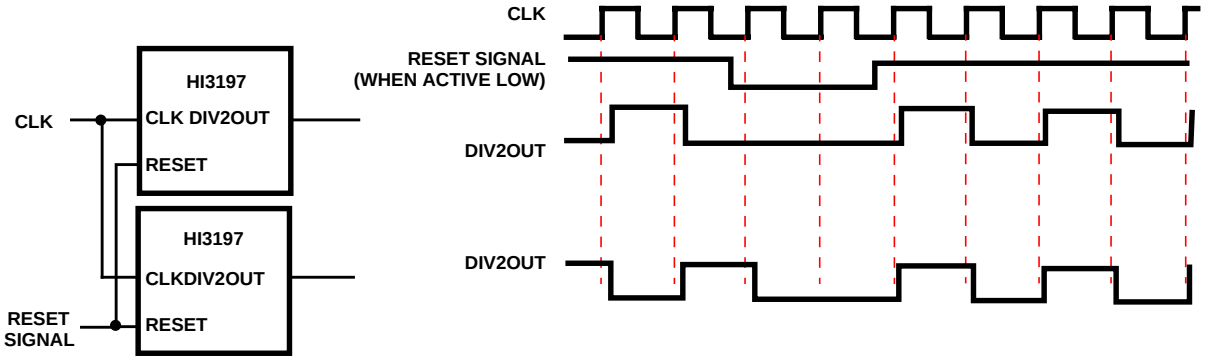


FIGURE 7C. MUX.1A EXAMPLE WHEN USING THE RESET SIGNAL

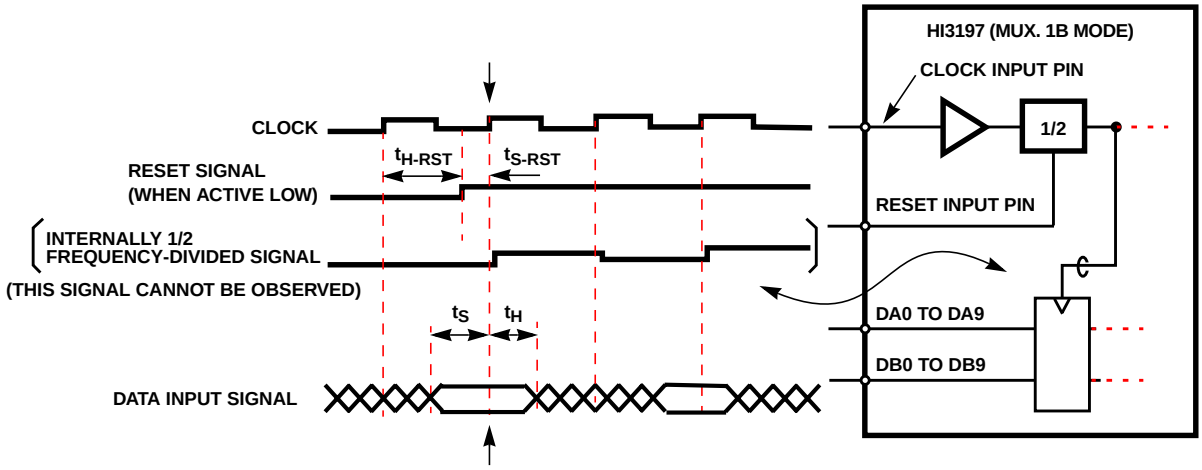
FIGURE 7. MUX.1A MODE

MUX.1B Mode

Set C1 and C2 Low and C3 High for this mode.

In MUX.1B mode, the frequency of the clock input from the clock input pin is halved internally, and the data is loaded by this 1/2 frequency-divided signal. The 1/2 frequency-divided signal cannot be observed at this time, so the data is actually loaded by observing the clock and reset signals to estimate the rising edge of the internally 1/2 frequency-divided signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay after loading by the clock.

Like MUX.1A mode, when using the multiple HI3197 in MUX.1B mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example below. As a countermeasure, the MUX.1B mode also has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See Figure 8 for the detailed timing.



AFTER THE RESET IS RELEASED, THE INTERNAL 1/2 FREQUENCY-DIVIDED SIGNAL COMMENCES AT THE FIRST CLOCK EDGE, SO BE SURE TO INPUT THE DATA IN A MANNER THAT SATISFIES THE SETUP TIME (TS) AND HOLD TIME (TH) WITH RESPECT TO THIS CLOCK EDGE.

FIGURE 8A.

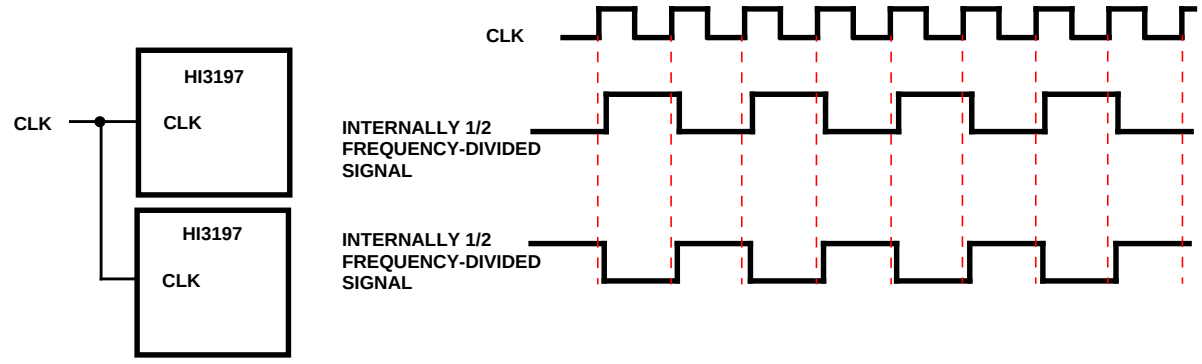


FIGURE 8B. EXAMPLE WHEN NOT USING THE RESET SIGNAL

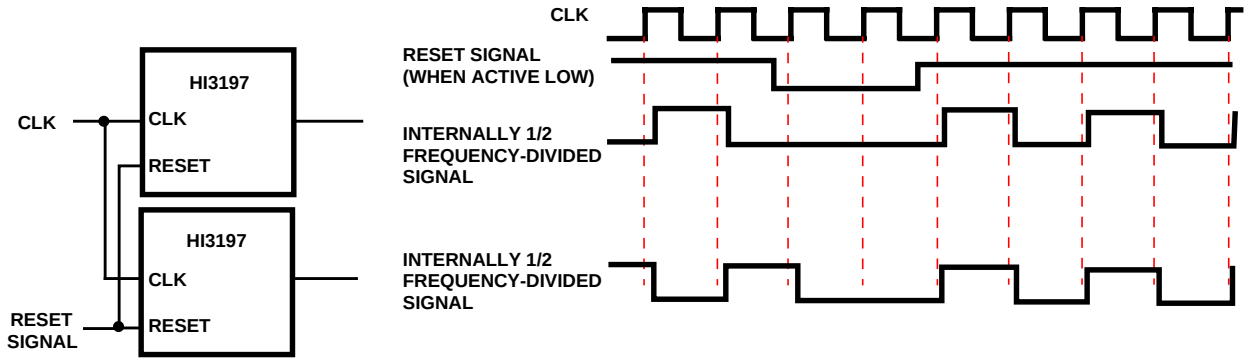


FIGURE 8C. EXAMPLE WHEN USING THE RESET SIGNAL

FIGURE 8. MUX.1B MODE

MUX.2 Mode

Set C1 and C3 Low and C2 High for this mode.

In MUX.2 mode, the clock is input to the clock input pin, and the signal with a cycle half that of the clock (hereafter, DIV2IN signal) is input to the DIV2IN pin at TTL level. The DIV2IN signal is internally latched by the clock, so consideration must be given to the setup time (t_{S_DIV}) and hold time (t_{H_DIV}) with respect to the clock. In addition, the data is loaded by the DIV2IN signal, so consideration must also be given to the setup time (t_S) and hold time (t_H) with respect to the DIV2IN signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data `is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay from the clock that loads the DIV2IN signal. See Figure 9 for the detailed timing.

SELECT.A Mode and SELE.B Mode

Set C1 High and C2 and C3 Low for SELE.A mode.

In SELE.A mode, the clock is input to the clock input pin, and the data is input to the system A (DA0 to DA9) data input pins.

Set C1 and C2 High and C3 Low for SELE.B mode.

In SELE.B mode, the clock is input to the clock input pin, and the data is input to the system B (DB0 to DB9) data input pins. In either mode, consideration must be given to the setup time, (t_S) and hold time (t_H) with respect to the clock. Also, the data is output as an analog signal with a 1-clock pipeline delay after loading by the clock.

Switching between SELE.A mode and SELE.B mode is done by switching the C2 pin between High and Low levels. Also, the mode can be switched at high speed in sync with the clock by inputting the switching signal (02 signal) to the C2 pin. The C2 signal is internally latched by the clock, so consideration must be given to the setup time (t_{S_C2}) and hold time (t_{H_C2}) with respect to the clock. See Figure 10 for the detailed timing.

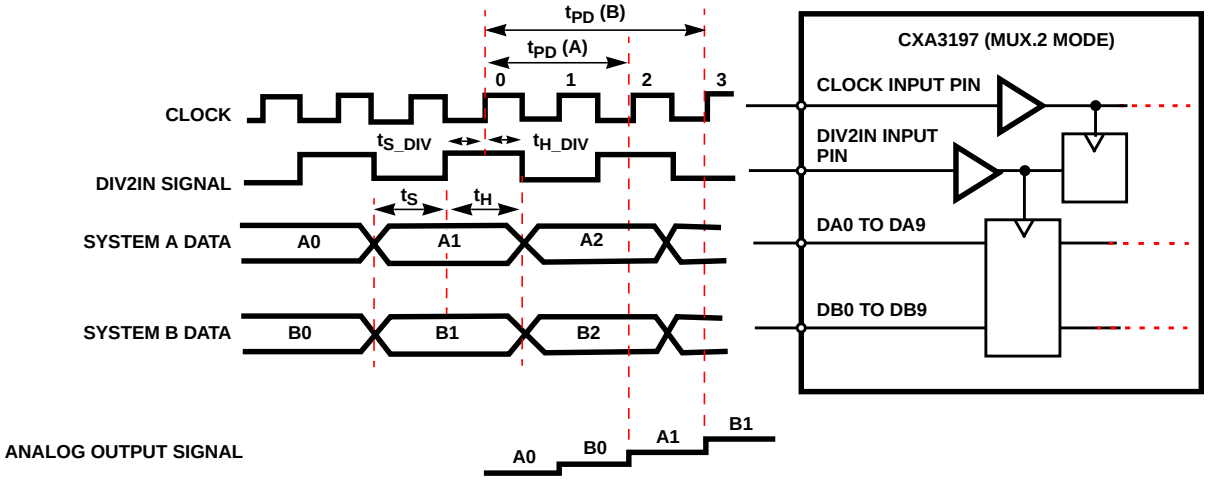


FIGURE 9. MUX.2 MODE

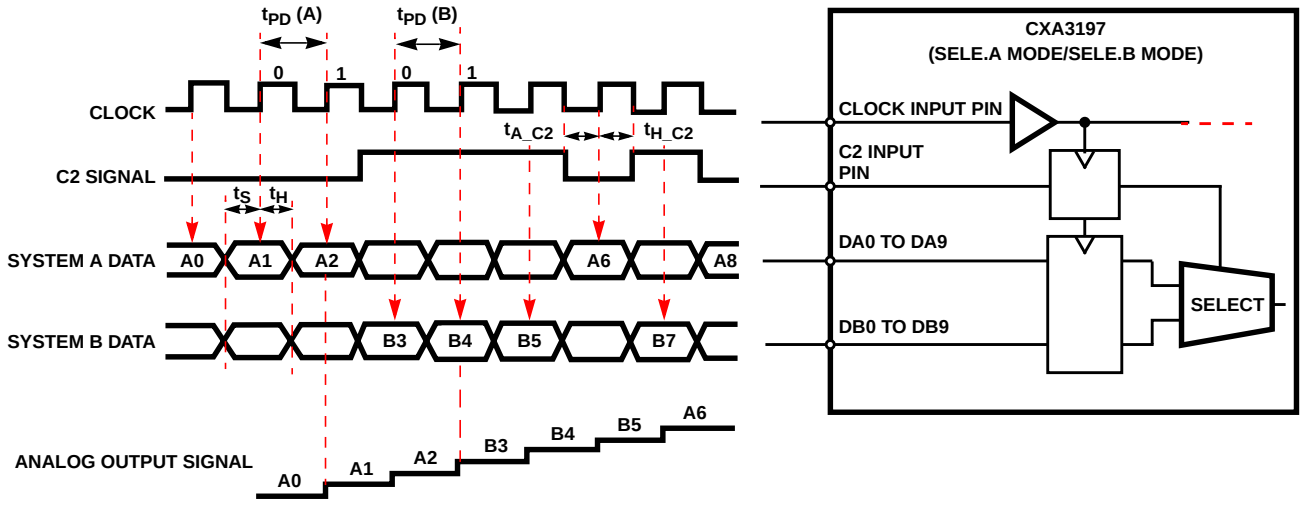


FIGURE 10. SELECT A MODE AND SELECT B MODE

Block Diagram and Timing Charts

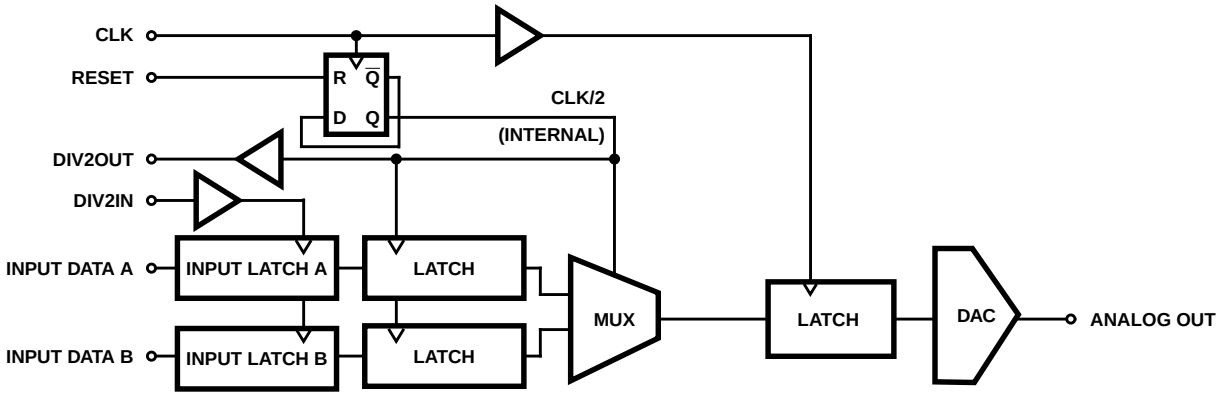


FIGURE 11A. BLOCK DIAGRAM (MUX.1A MODE)

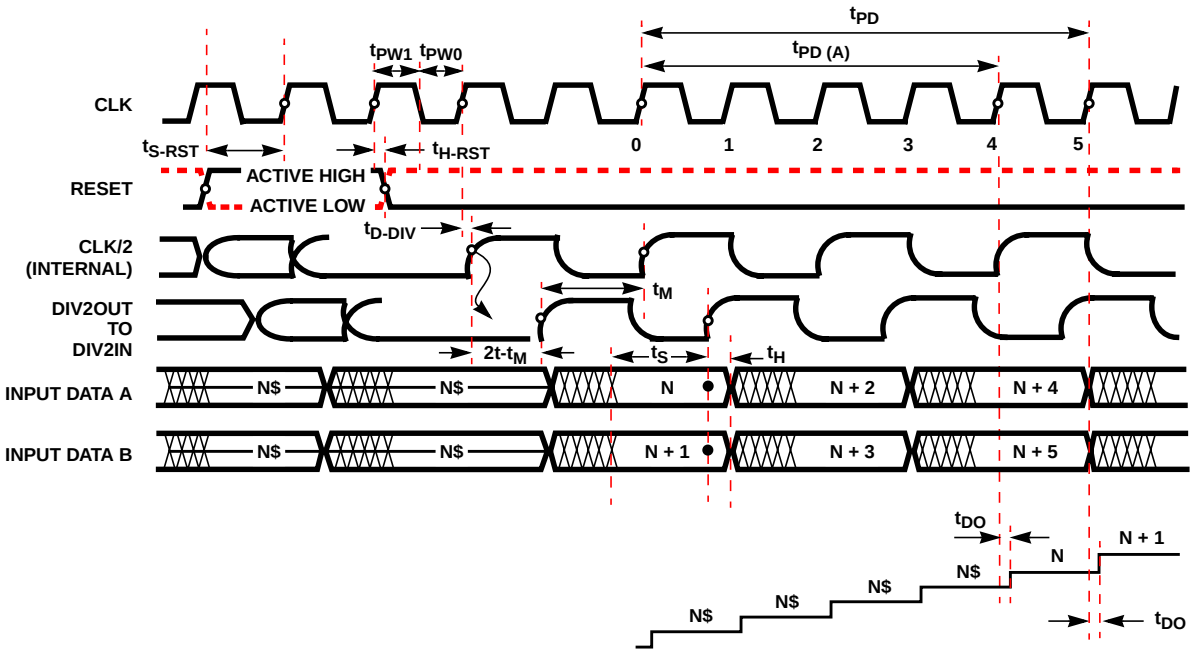


FIGURE 11B. TIMING CHART (MUX.1A MODE)

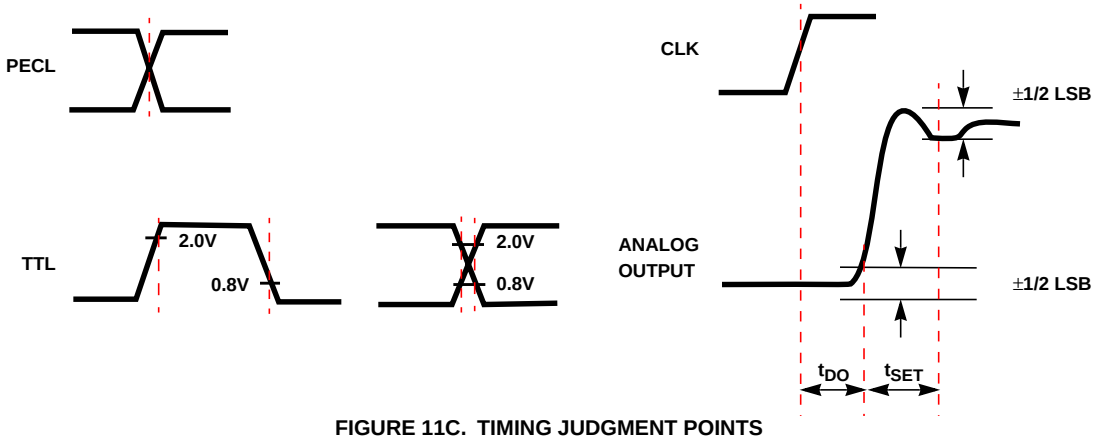


FIGURE 11C. TIMING JUDGMENT POINTS

NOTE: In MUX.1A mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit and the CLK/2 can be output at TTL level (D1V201.~). CLK/2 can be reset by the reset signal.

Block Diagram and Timing Charts (Continued)

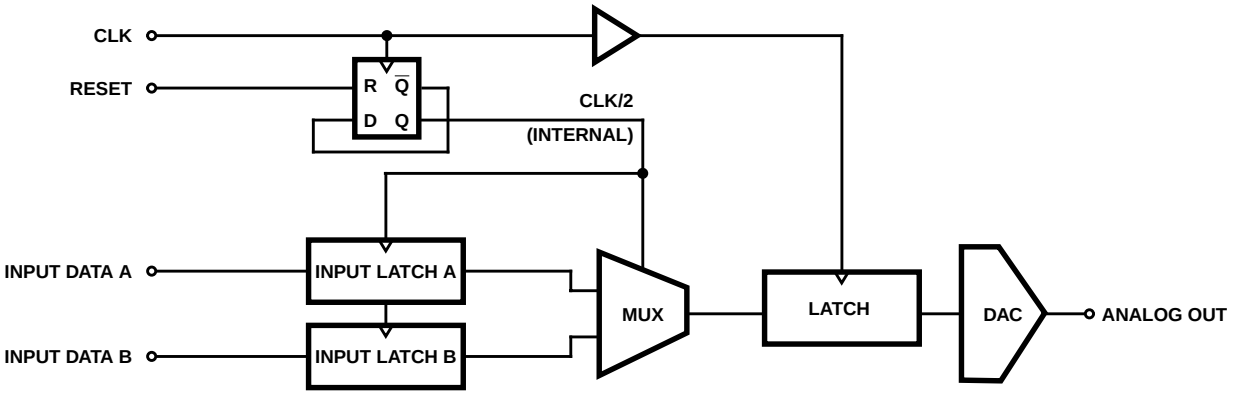


FIGURE 12A. BLOCK DIAGRAM (MUX.1B MODE)

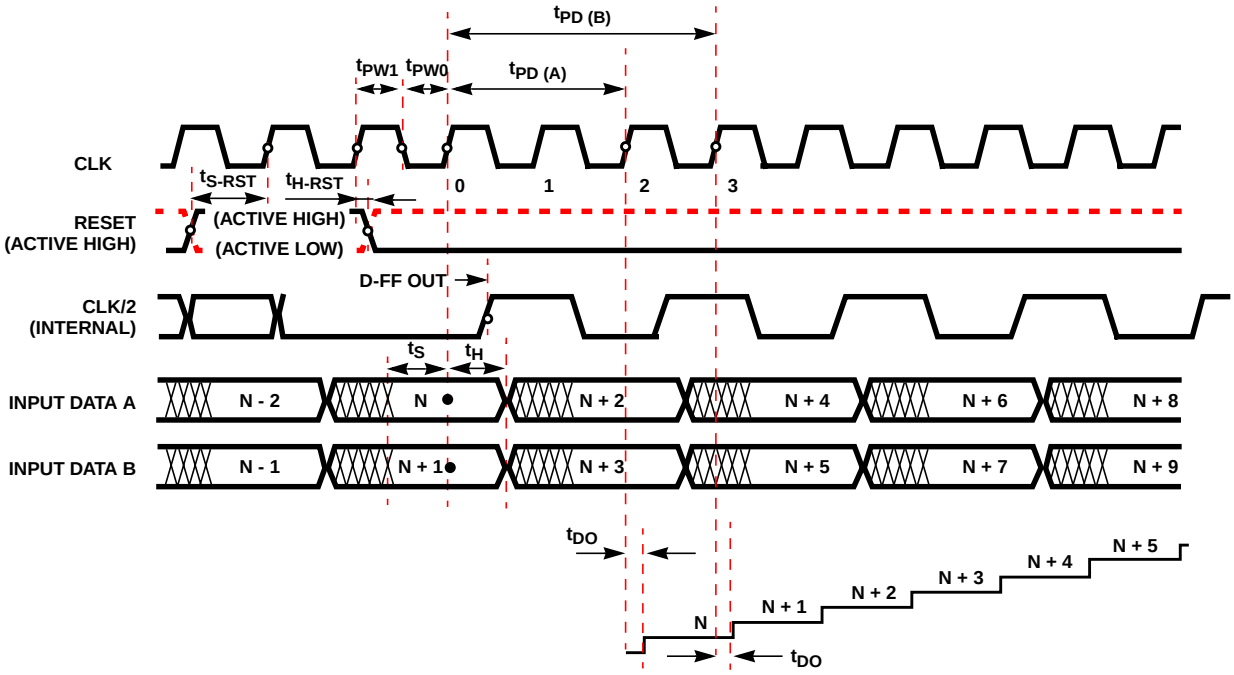


FIGURE 12B. TIMING CHART (MUX.1B MODE)

NOTE: In MUX.1B mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit. CLK/2 can be reset by the reset signal.

Block Diagram and Timing Charts (Continued)

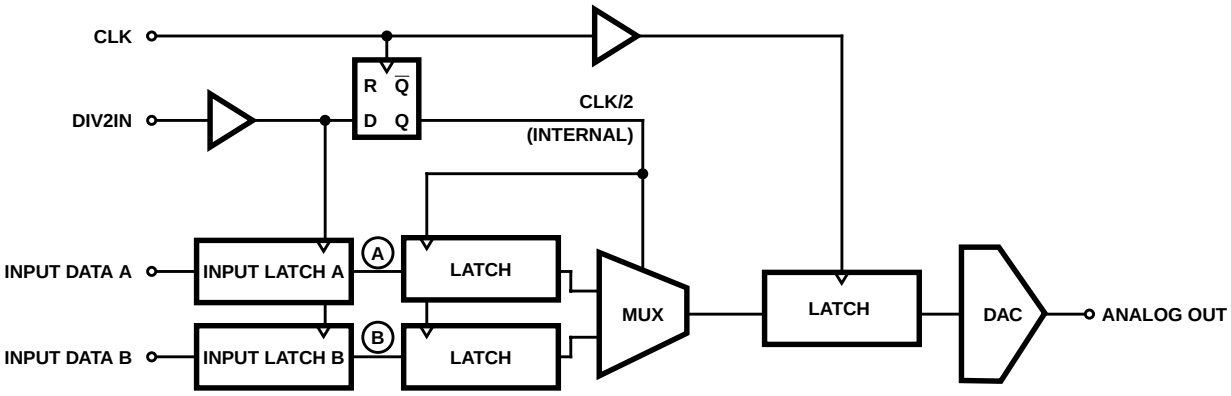


FIGURE 13A. BLOCK DIAGRAM (MUX.2 MODE)

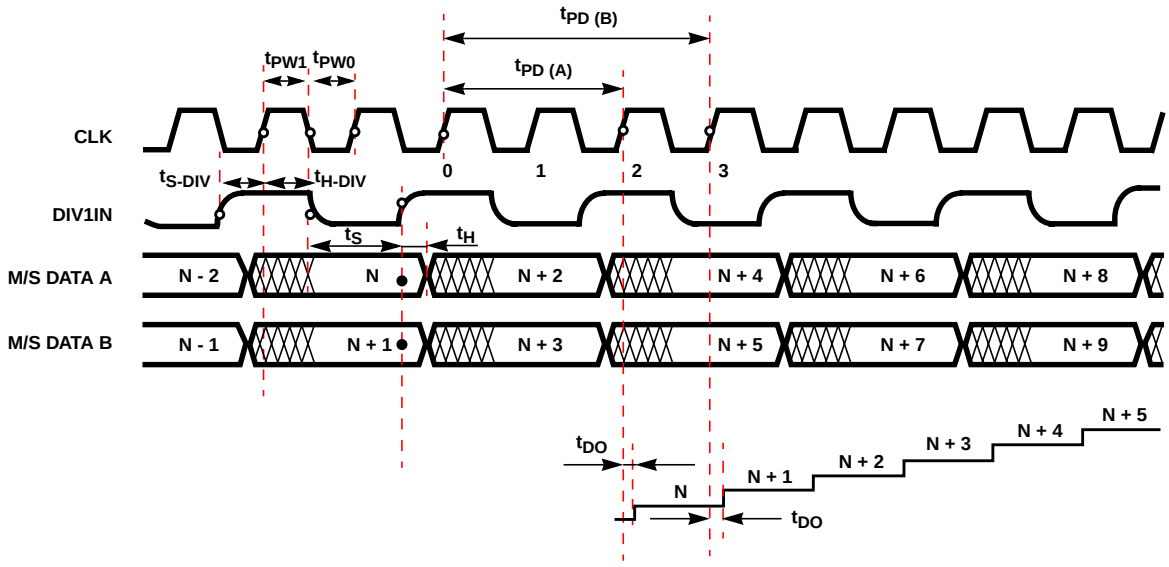


FIGURE 13B. TIMING MODE (MUX.2 MODE)

NOTE: In MUX.2 mode, the 1/2 frequency-divided clock signal (DIV2IN) and Data A and Data B, which are synchronized with DIV2IN, are provided simultaneously. These signals are internally multiplexed and the resulting signal can be analog output.

Block Diagram and Timing Charts (Continued)

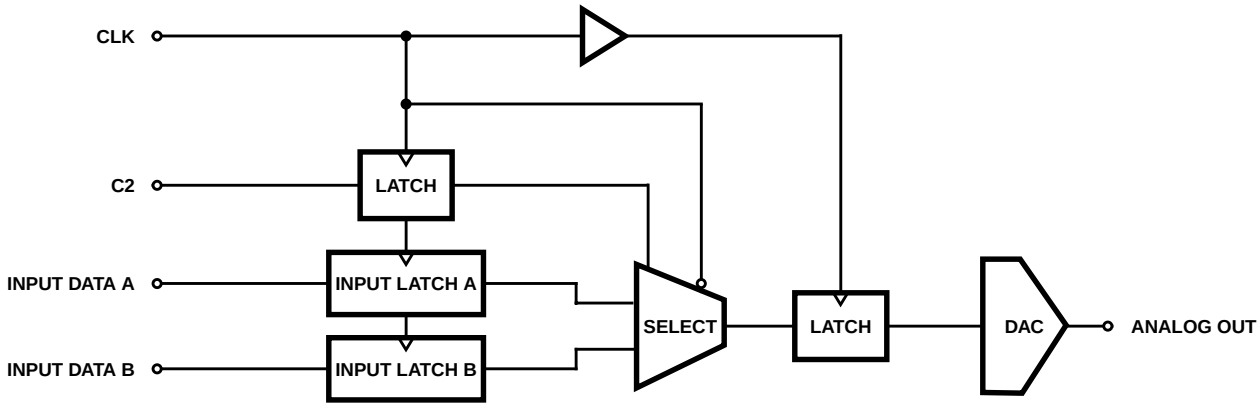


FIGURE 14A. BLOCK DIAGRAM (SELE.A, SELE.B MODE)

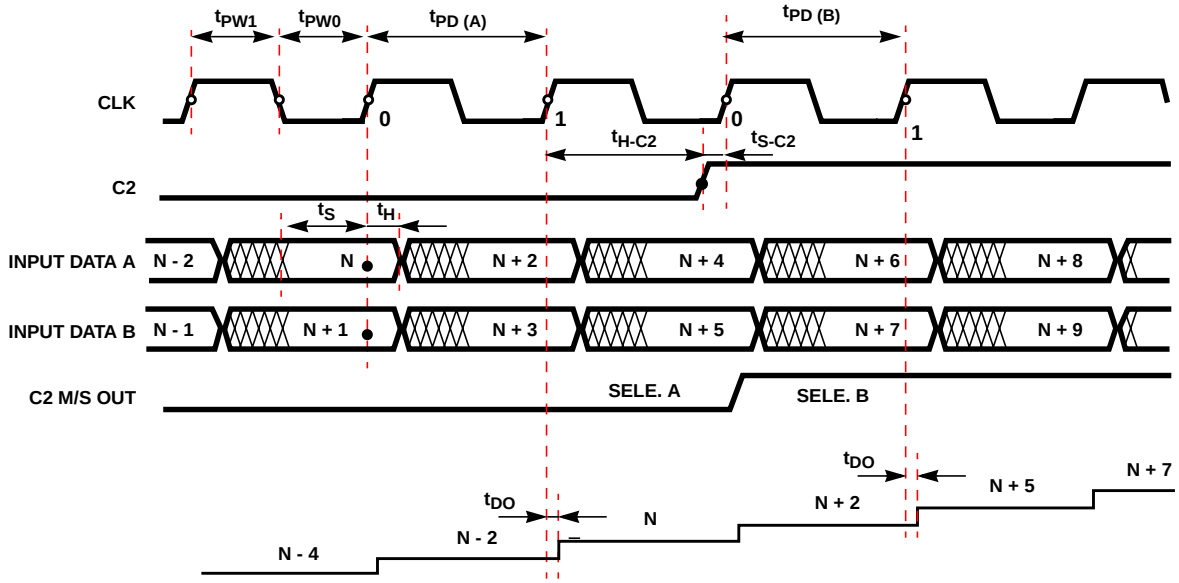


FIGURE 14B. TIMING CHART (SELE.A, SELE.B MODE)

NOTE: In SELE.A and SELE.B modes, input Data A or Data B is selected and the selected data can be analog output. When C1 = 1 and C3 = 0, Data A is selected for C2 = 0, and Data B is selected for C2 = 1.

Typical Performance Curves

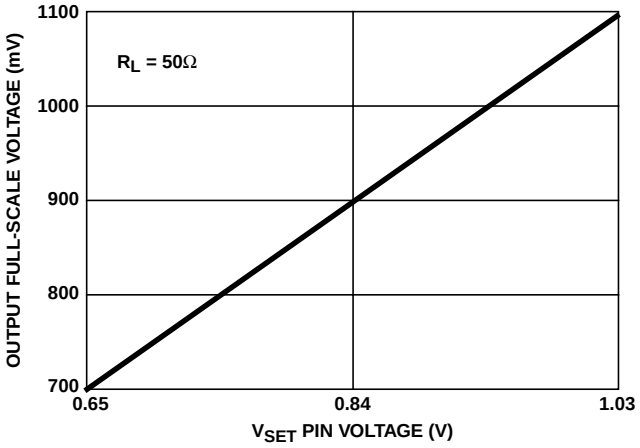


FIGURE 15. OUTPUT FULL-SCALE VOLTAGE vs V_{SET} PIN VOLTAGE

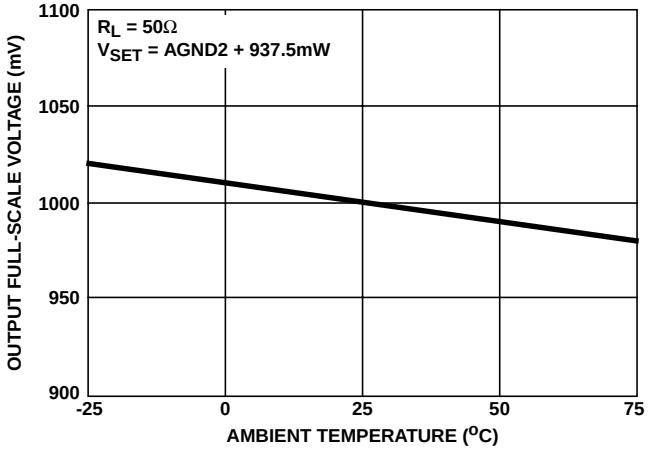


FIGURE 16. OUTPUT FULL-SCALE VOLTAGE vs AMBIENT TEMPERATURE

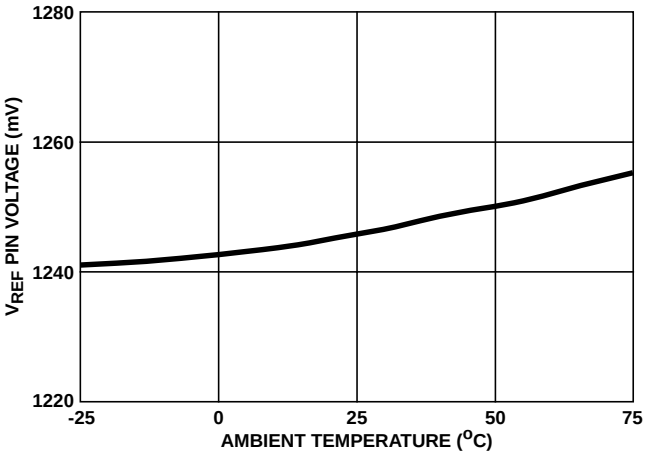


FIGURE 17. V_{REF} PIN VOLTAGE vs AMBIENT TEMPERATURE

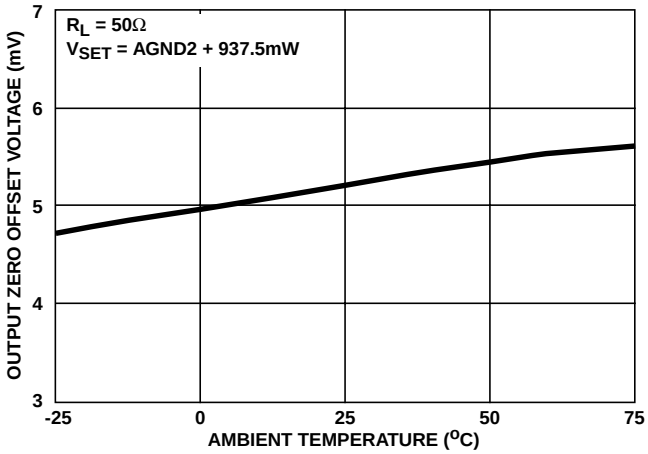


FIGURE 18. OUTPUT ZERO OFFSET VOLTAGE vs AMBIENT TEMPERATURE

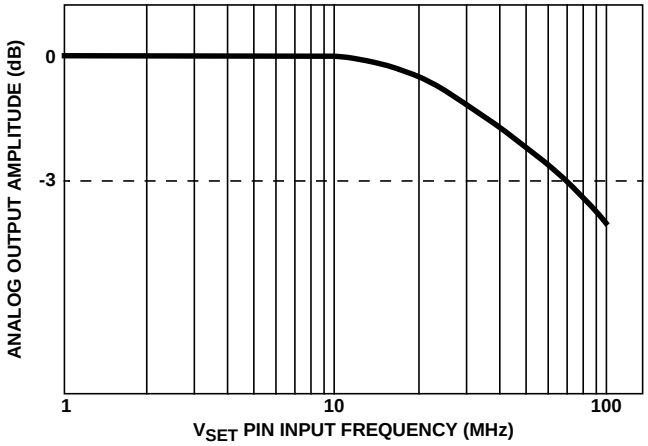


FIGURE 19. MULTIPLYING BANDWIDTH

Application Circuit

The circuit shown below is the basic circuit when the analog output is terminated with the external resistance of 50Ω in the dual ±5V power supplies for MUX.2 mode.

The analog output full scale voltage V_{FS} is obtained with the following equation:

$$V_{FS} = \frac{V_{SET}}{375} \times \left(15 + \frac{63}{64}\right) \times R$$

$R = R_O // R_L$

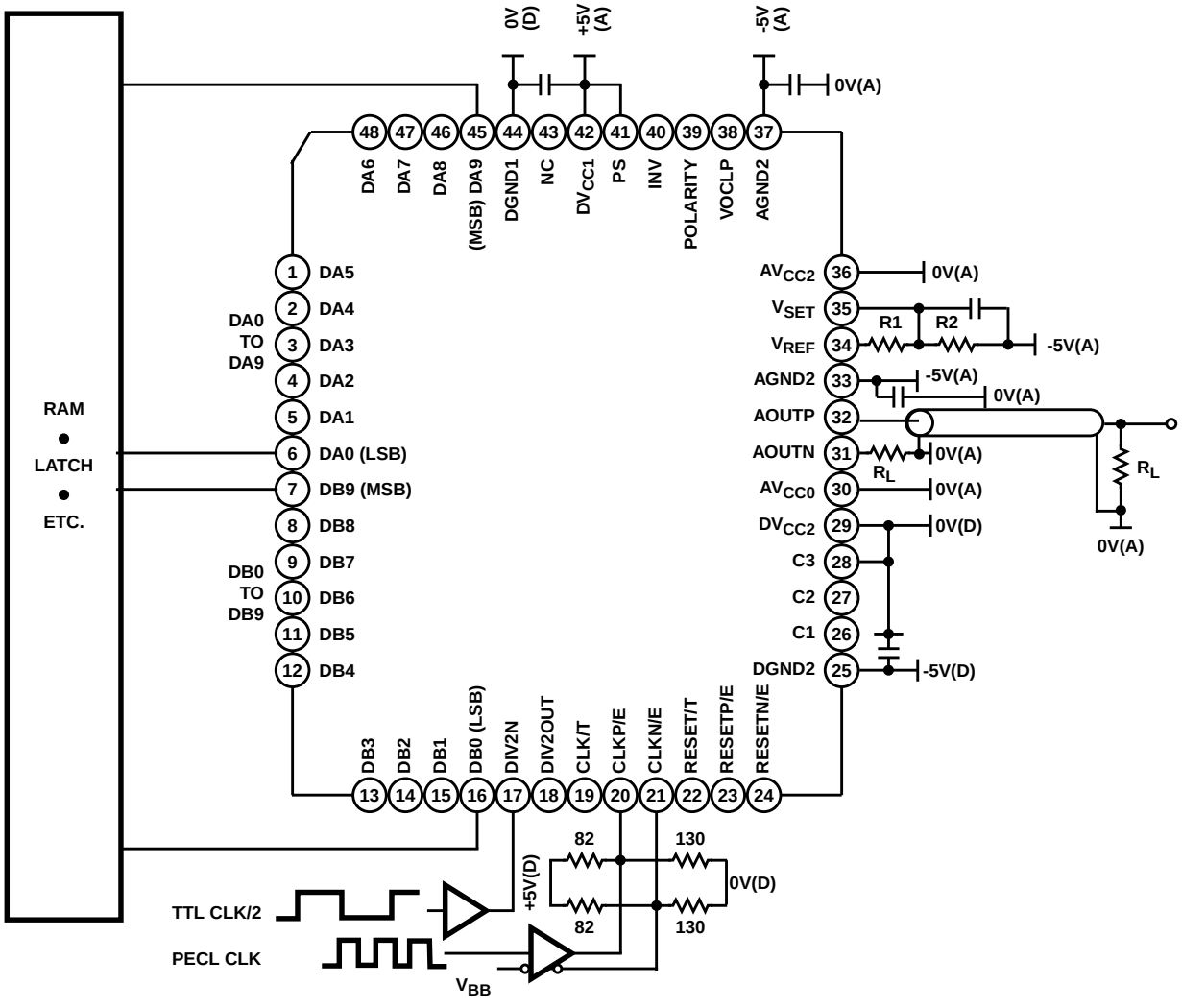
R_O : Output impedance (= 50Ω)

R_L : External termination resistance

Here, $V_{SET} = \frac{R2}{R1 + R2} V_{REF}$

($V_{REF} \approx 1.2V$)

($R1 + R2 \geq 1.2k\Omega$)

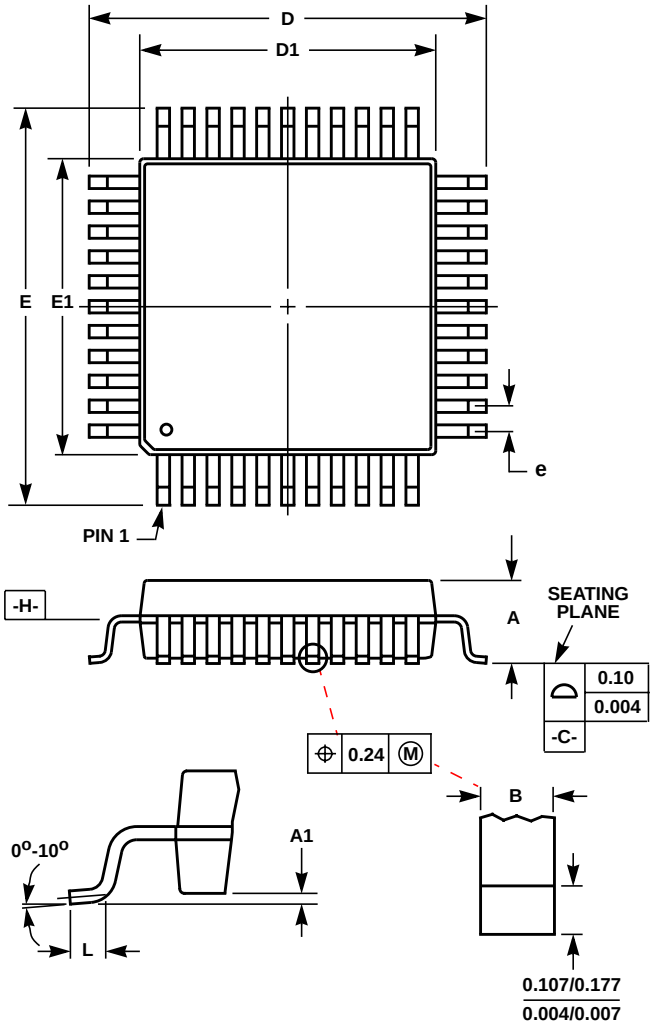


NOTE: Application circuits shown are typical examples illustrating the operation of the devices. Intersil Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Use

- The HI3197 has PECL and TTL input pins for the clock and reset inputs. When the clock is input at PECL level, it is recommended to also input the reset signal at PECL level. Likewise, when the clock is input at TTL level, it is recommended to also input the reset signal at TTL level.
- The input signal impedance should be properly matched to ensure the stable HI3197 operation at high speed. Particularly when ringing appears in the input clock in the MUX.1A and MUX.1B modes. If this ringing exceeds the clock input threshold value, the internal 1/2 frequency divider circuit may misoperate.
- All TTL input pins of the HI3197 except for the PS pin go to High level when left open, and only the PS pin goes to Low level when left open. Set the PS pin to High level to operate the IC. When the PECL input pins are left open, the P (positive) side goes to High level and the N (negative) side goes to Low level. The PECL input pins are complementary, so be sure to use the P and N sides together.
- When the clock and reset input signal level is TTL, ***/T pins should be used and ***/E pins left open. When the clock and reset input signal level is PECL, ***/E pins should be used and ***/T pins left open.
- The power supply and grounding have a profound influence on converter characteristics. The power supply and grounding method are particularly important during high-speed operation.
  General points for caution are as follows:
  - The ground pattern should be as wide as possible. It is recommended to make the power supply and ground wider at an inner layer using a multi-layer board. To prevent a DC offset from being generated between the analog and digital power supply patterns, it is recommended to connect the patterns at one point via a ferrite-bead filter, etc.
  - When using the HI3197 with a single power supply, connect DGND1 and DGND2 to a common digital ground, and AGND2 to an analog ground. Also, DV_{CC1} and DV_{CC2} should use a common digital power supply, and AV_{CC2} should be connected to an analog power supply. AV_{CC0} serves as the analog output reference, so while it does not need to share the analog power supply, it should be used within the range that satisfies the analog output compliance voltage.
  - When using the HI3197 with dual power supply, connect DGND1 and DV_{CC2} to the digital ground, and AV_{CC2} to the analog ground. DV_{CC1} uses a positive digital power supply (+5V, typ.), DGND2 uses a negative digital power supply (-5V, typ.), and AGND2 uses a negative analog power supply (-5V, typ.). Like when using a single power supply, the AV_{CC0} pin can be used within the range that satisfies the analog output compliance voltage. However, connecting it to the analog ground and using the analog ground as the reference for the analog output is recommended.
- Ground the power supply pins as close to each pin as possible with a 0.1µF or more ceramic chip capacitor. When using a single power supply, connect DV_{CC1} and DV_{CC2} to the digital ground, and AV_{CC2} and AV_{CC0} to the analog ground. When using dual power supply, connect DV_{CC1} and DGND2 to the digital ground, and AGND2 to the analog ground. In this case, when using AV_{CC0} within the range that satisfies the compliance voltage, be sure to also connect the AV_{CC0} pin to the analog ground using a ceramic chip capacitor.
- The HI3197 is designed with an analog output impedance of 50Ω. The analog outputs are wired with a characteristic impedance of 50Ω, and waveforms free of reflection can be obtained by terminating the analog outputs with 50Ω. Even when using only one of either AOUTP or AOUTN, if one analog output is terminated with 50Ω, be sure to also terminate the other analog output with 50Ω. (See Application Circuit Diagram)

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q48.7x7-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. “N” is the number of terminal positions.

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