Data Sheet July 1999 File Number 4620.1

CMOS Quad 2-Input NAND Gate

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The CD4011BT, Quad 2-Input NAND gate provides the system designer with direct implementation of the NAND function and supplements the existing family of CMOS gates. All inputs and outputs are buffered.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the CD4011BT are contained in SMD 5962-96621. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/quality/manuals.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9662101TCC	CD4011BDTR	-55 to 125
5962R9662101TXC	CD4011BKTR	-55 to 125

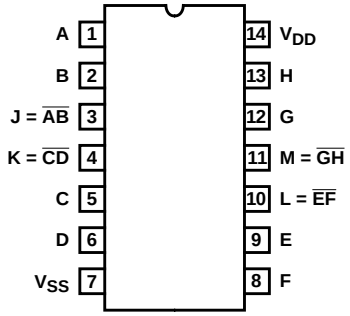
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

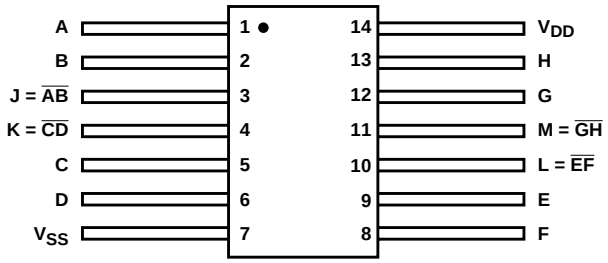
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - SEP Effective LET > 75 MEV/gm/cm^2
- Propagation Delay Time = 60ns (typ.) at CL = 50pF, V_{DD} = 10V
- Buffered Inputs and Outputs
- Standardized Symmetrical Output Characteristics
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings

Pinouts

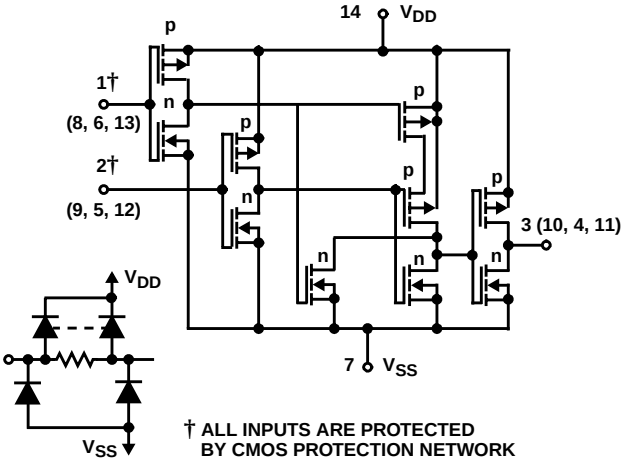
CD4011BT (SBDIP), CDIP2-T14
TOP VIEW

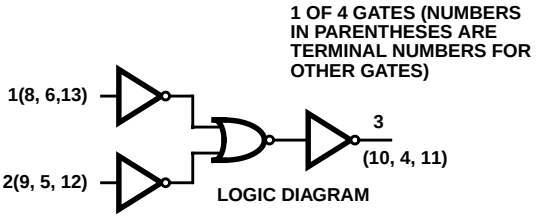


CD4011BT (FLATPACK), CDFP3-F14
TOP VIEW



Schematic and Logic Diagram





Die Characteristics

DIE DIMENSIONS:

(1143µm x 1626µm x 533µm ±25.4µm)

45 x 64 x 21mils ±1mil

METALLIZATION:

Type: Al

Thickness: 12.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL:

Leave Floating or Tie to V_{DD}

Bond Pad #14 (V_{DD}) First

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Phosphorus Doped Silox (S_iO_2)

Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

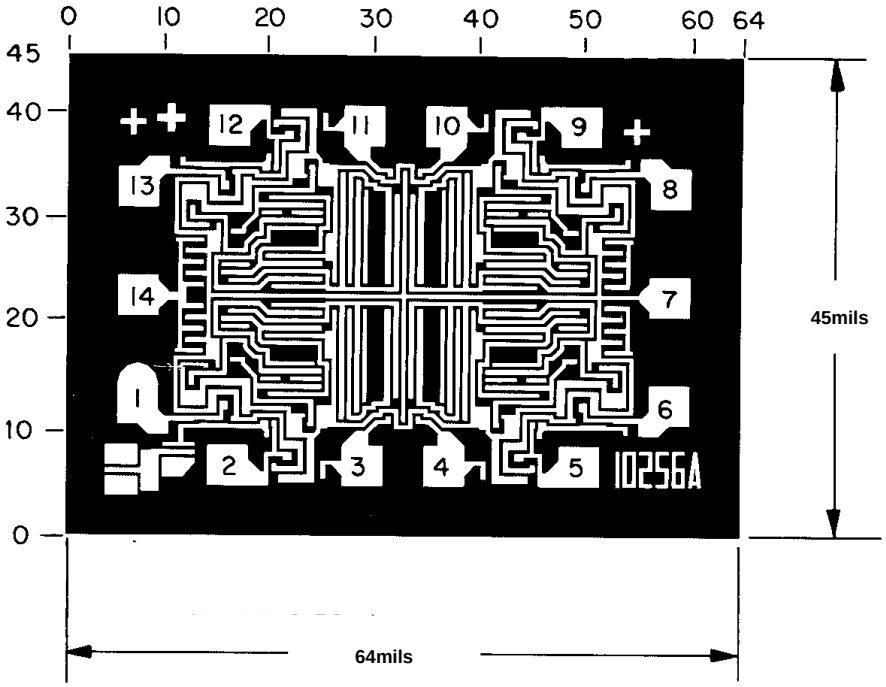
10

PROCESS:

Bulk CMOS

Metallization Mask Layout

CD4011BT



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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