PRELIMINARY | Data Sheet | January 2000 | File Number 4661.2

## Wireless LAN Medium Access Controller


The Intersil HFA3841 Wireless LAN Medium Access Controller is part of the PRISM® Enterprise 2.4GHz WLAN chip set. The HFA3841 directly interfaces with the Intersil HFA386x family of Baseband Processors, offering a complete end-to-end chip set solution for wireless LAN products. Protocol and PHY support are implemented in firmware to allow custom protocol and different PHY transceivers.

The HFA3841 is designed to provide maximum performance with minimum power consumption. External pin layout is organized to provide optimal PC board layout to all user interfaces.

Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgement, fragmentation and de-fragmentation, and automatic beacon monitoring are handed without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers. Additional firmware functions specific to access point applications are also available.

Designing wireless protocol systems using the HFA3841 is made easier with the availability of evaluation board, firmware, software device drivers, and complete documentation.

## Features

- IEEE802.11 Standard Data Rates: 1, 2, 5.5 and 11Mbps
- Part of the Intersil PRISM Wireless LAN Chip Set
- Full Implementation of the MAC Protocol Specified in IEEE Std. 802.11-1999 and the 802.11b Draft Standard
- Host Interface Supports Full 16-Bit Implementation of PC Card 95, also ISA PnP with Additional Chip
- Host Interface Provides Dual Buffer Access Paths
- External Memory Interface Supports up to 4M bytes RAM
- Internal Encryption Engine Executes IEEE802.11 WEP
- Low Power Operation; 25mA Active, 8mA Doze, <1mA Sleep
- Operation at 2.7V to 3.6V Supply
- 3V to 5V Tolerant Input/Outputs
- 128 Pin LQFP Package Targeted for Type II PC Cards
- IEEE802.11 Wireless LAN MAC Protocol Firmware and Microsoft® Windows® Software Drivers

## Applications

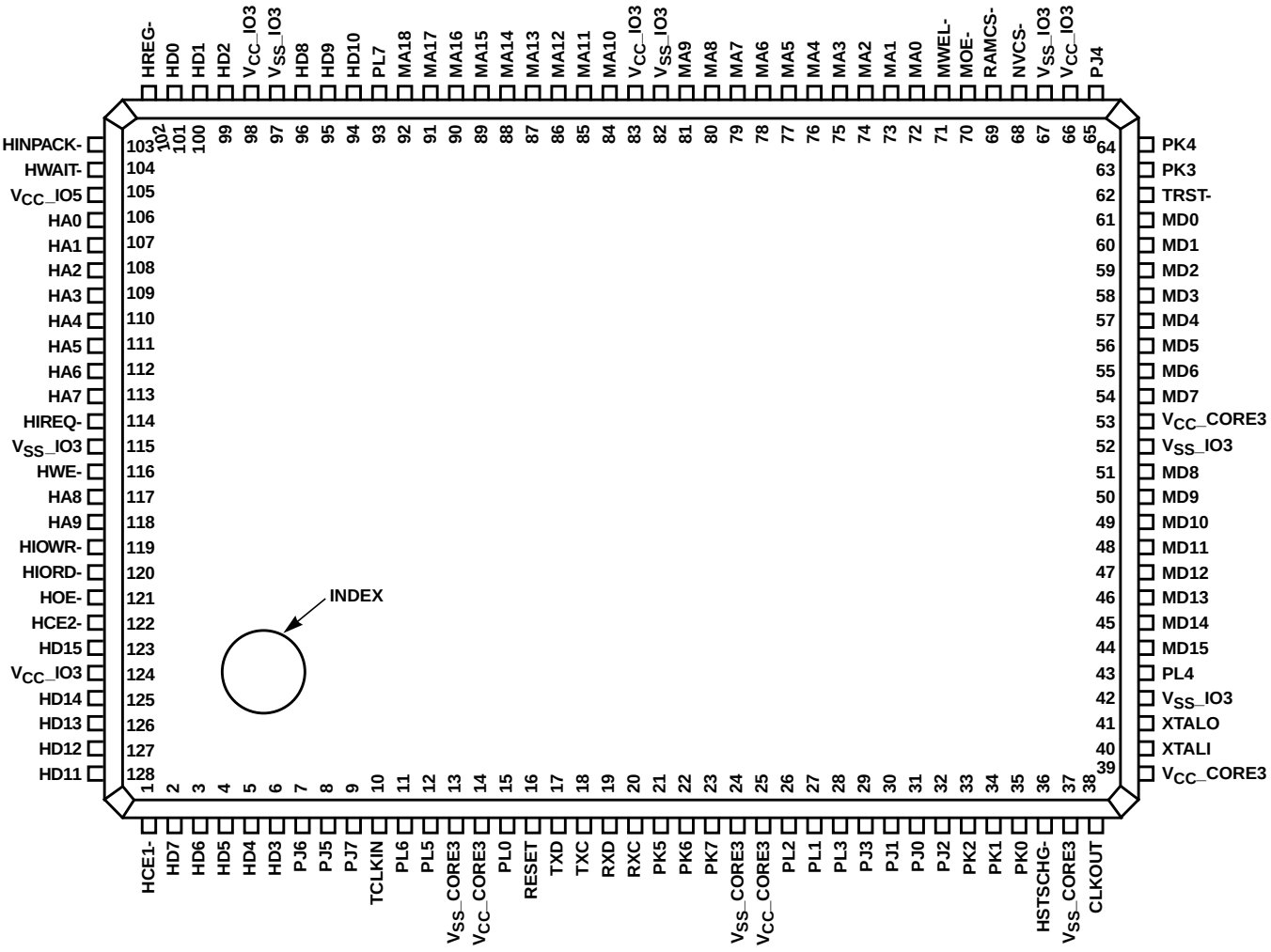
- High Data Rate Wireless LAN
- PC Card Wireless LAN Adapters
- ISA, ISA PnP WLAN Cards
- PCI Wireless LAN Cards (Using Ext. Bridge Chip)
- Wireless LAN Modules
- Wireless LAN Access Points
- Wireless Bridge Products
- Wireless Point-to-Multipoint Systems

## Ordering Information

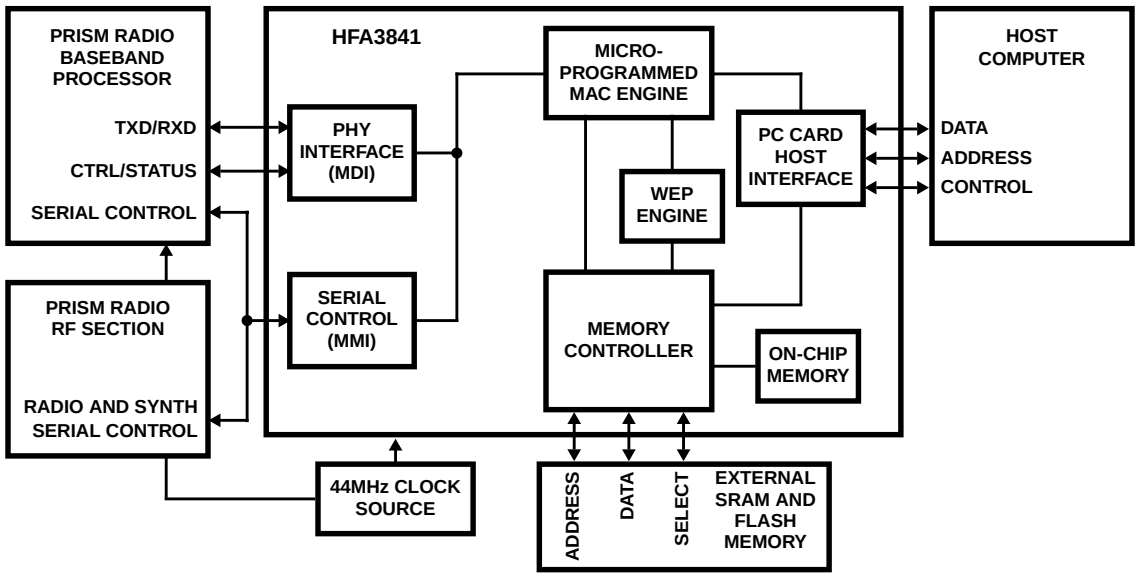
| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HFA3841CN | 0 to 70 | 128 Ld LQFP | Q128.14x20 |
| HFA3841CN96 | 0 to 70 | Tape and Reel | |

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

## Pinout




## Simplified Block Diagram



## HFA3841 Pin Descriptions

### Host Interface Pins

| PIN NAME | PIN NUMBER | PIN I/O TYPE | DESCRIPTION |
|---|---|---|---|
| HA0-9 | 106-113, 117, 118 | 5V tol, CMOS, Input, 50K Pull Down | PC Card address input, bits 0 to 9 |
| HCE1- | 1 | 5V tol, CMOS, Input, 50K Pull Up | PC Card card select, low byte |
| HCE2- | 122 | 5V tol, CMOS, Input, 50K Pull Up | PC Card card select, high byte |
| HD0-15 | 101-99, 6-2, 96-94, 128-125, 123 | 5V tol, BiDir, 2mA, 50K Pull Down | PC Card data bus, bit 0 to 15 |
| HINPACK- | 103 | CMOS Output, 2mA | PC Card I/O decode confirmation |
| HIORD- | 120 | 5V tol, CMOS, Input, 50K Pull Up | PC Card I/O space read |
| HIOWR- | 119 | 5V tol, CMOS, Input, 50K Pull Up | PC Card I/O space write |
| HRDY/HIREQ- | 114 | CMOS Output, 4mA | PC Card interrupt request (I/O mode) Card ready (memory mode) |
| HOE- | 121 | 5V tol, CMOS, Input, 50K Pull Up | PC Card memory attribute space output enable |
| HREG- | 102 | 5V tol, CMOS, Input, 50K Pull Up | PC Card attribute space select |
| HRESET | 16 | 5V tol, CMOS, ST Input, 50K Pull Up Hardware Reset | |
| HSTSCHG- | 36 | CMOS Output, 4mA | PC Card status change |
| HWAIT- | 104 | CMOS Output, 4mA | PC Card not ready (force host wait state) |
| HWE- | 116 | 5V tol, CMOS Input, 50K Pull Up | PC Card memory attribute space write enable |

### Memory Interface Pins

| PIN NAME | PIN NUMBER | PIN I/O TYPE | DESCRIPTION |
|---|---|---|---|
| MA0 MWEH- | 72 | CMOS TS Output, 2mA | MBUS address bit 0 (byte) for x8 memory High byte write enable for x16 memory |
| MA1-18 | 73-81, 84-92 | CMOS TS Output, 2mA | MBUS address bits 1 to 18 |
| PL4 | 43 | CMOS BiDir, 2mA | MBUS address bit 19 |
| PL5 | 12 | CMOS BiDir, 2mA, 50K Pull Up | MBUS address bit 20 |
| PL6 | 11 | CMOS BiDir, 2mA | MBUS address bit 21 |
| MOE- | 70 | CMOS TS Output, 2mA | Memory output enable |
| MWEL- | 71 | CMOS TS Output, 2mA | Low (or only) byte memory write enable |
| RAMCS- | 69 | CMOS TS Output, 2mA | RAM select |
| NVCS- | 68 | CMOS TS Output, 2mA | NV memory select |
| MD0-7 | 61-54 | 5V tol, CMOS, BiDir, 2mA, 100K Pull Up | MBUS low data byte, bits 0 to 7 |
| MD8-15 | 51-44 | 5V tol, CMOS, BiDir, 2mA 50K Pull Down | MBUS high data byte, bits 8 to 15 |

### Radio Interface and General Purpose Port Pins

| PIN NAME | PIN NUMBER | PIN I/O TYPE | DESCRIPTION OF FUNCTION (IF OTHER THAN IO PORT) |
|---|---|---|---|
| TXD | 17 | CMOS Output, 2mA, 50K Pull Down | Transmit data out |
| TXC | 18 | 5V tol, CMOS, BiDir 2mA, ST | Transmit clock in/out |
| RXD | 19 | CMOS Input | Receive data in |
| RXC | 20 | CMOS Input, ST | Receive clock in |
| PJ0 | 31 | CMOS BiDir, 2mA, ST, 50K Pull Down | MMI serial clock in/out |
| PJ1 | 30 | CMOS BiDir, 2mA, 50K Pull Down | MMI serial data in/out |
| PJ2 | 32 | CMOS BiDir, 2mA, 50K Pull Down | MMI serial data read/write control, or data output |
| PJ3 | 29 | CMOS BiDir, 2mA | MMI device enable |
| PJ4 | 65 | CMOS BiDir, 2mA | |
| PJ5 | 8 | CMOS BiDir, 2mA, 50K Pull Up | |
| PJ6 | 7 | CMOS BiDir, 2mA | |
| PJ7 | 9 | CMOS BiDir, 2mA, 50K Pull Up | |
| PK0 | 35 | CMOS BiDir, 2mA, ST, 50K Pull Down | |
| PK1 | 34 | CMOS BiDir, 2mA, 50K Pull Down | |
| PK2 | 33 | CMOS BiDir, 2mA, 50K Pull Down | |
| PK3 | 63 | CMOS BiDir, 2mA | |
| PK4 | 64 | CMOS BiDir, 2mA | |
| PK5 | 21 | CMOS BiDir, 2mA | MDREADY - PHY or MAC data available (in) |
| PK6 | 22 | CMOS BiDir, 2mA | Medium busy (CCA from PHY) |
| PK7 | 23 | CMOS BiDir, 2mA | |
| PL0 | 15 | CMOS BiDir, 2mA | Transmitter enable |
| PL1 | 27 | CMOS BiDir, 2mA | Receiver enable (or PHY sleep control) |
| PL2 | 26 | CMOS BiDir, 2mA | |
| PL3 | 28 | CMOS BiDir, 2mA | |
| PL4 | 43 | CMOS BiDir, 2mA | MBUS address bit 19 |
| PL5 | 12 | CMOS BiDir, 2mA, 50K Pull Up MBUS address bit 20 | |
| PL6 | 11 | CMOS BiDir, 2mA | MBUS address bit 21 or PHY control I/O |
| PL7 | 93 | CMOS BiDir, 2mA | Transmitter ready |

### Clocks

| PIN NAME | PIN NUMBER | PIN I/O TYPE | DESCRIPTION |
|---|---|---|---|
| XTALI | 40 | CMOS Input, ST | Crystal or external clock input (at >= 2X desired MCLK frequency) |
| XTALO | 41 | CMOS Output, 2mA | Crystal output |
| CLKOUT | 38 | CMOS, TS Output, 2mA | Clock output (selectable as OSC or MCLK) |
| TCLKIN | 10 | CMOS Input, ST, 50K Pull Down | Timebase Reference Clock Input |

### Power

| PIN NAME | PIN NUMBER | PIN I/O TYPE | DESCRIPTION |
|---|---|---|---|
| VCC_CORE3 | 14, 25, 39, 53 | 3.3V Core Supply | |
| VCC_IO3 | 66, 83, 98. 124 | 3.3V I/O Supply | |
| VCC_IO5 | 105 | 5V Tolerance Supply | |
| VSS_CORE3 | 13, 24, 37 | Core $V_{SS}$ | |
| VSS_IO3 | 42, 52, 67, 82, 97, 115 | I/O $V_{SS}$ | |
| TRST- | 62 | CMOS Input | Reserved - Must be tied low through 1K |

ST = Schmitt Trigger (Hysteresis), TS = Three-State. Signals ending with “-” are active low.

NOTE: Output pins typically drive to positive voltage rail less 0.1V. Hence with a supply of 2.7V the output will just meet 5V TTL signal levels at rated loads.

### Port Pin Uses for PRISM Application

| PIN | NAME | PRISM I USE | PRISM II™ USE |
|---|---|---|---|
| 20 | RXC | RXC - Receive clock | RXC - Receive clock |
| 19 | RXD | RXD - Receive data | RXD - Receive data |
| 18 | TXC | TXC - Transmit clock | TXC - Transmit clock |
| 17 | TXD | TXD - Transmit data | TXD - Transmit data |
| 31 | PJ0 | SCLK - Clock for the SD serial bus. | SCLK - Clock for the SD serial bus. |
| 30 | PJ1 | SD - Serial bi-directional data bus | SD - Serial bi-directional data bus |
| 32 | PJ2 | R/W - An input to the HFA3860A used to change the direction of the SD bus when reading or writing data on the SD bus. | Not Used |
| 29 | PJ3 | CS - A Chip select for the device to activate the serial control port. (active low) | CS_BAR - Chip select for HFA3861 baseband (active low) |
| 65 | PJ4 | Not Used | PE1 - Power Enable 1 |
| 8 | PJ5 | SYNTH_LE - Latches a frame of 22 bits after it has been shifted by the SCLK into the synthesizer registers. | LE_IF - Load enable for HFA3783 Quad IF |
| 7 | PJ6 | LED - Activity indicator | LED - Activity indicator |
| 9 | PJ7 | Not Used | RADIO_PE - RF power enable |
| 35 | PK0 | Not Used | LE_RF - Load enable for HFA3983 RF chip |
| 34 | PK1 | Not Used | SYNTHCLK - Serial clock to front end chips |
| 33 | PK2 | Not Used | SYNTHDATA - Serial data to front end chips |
| 63 | PK3 | TX_PE_RF - Power Enable | PA_PE - Transmit PA power enable |
| 64 | PK4 | RX_PE_RF - Power Enable | PE2 - Power Enable 2 |
| 21 | PK5 | MD_RDY - Header data and data packet are ready to be transferred from Baseband on RXD | MDREADY - Header data and data packet are ready to be transferred from Baseband on RXD |
| 22 | PK6 | CCA - Signal that the channel is clear to transmit. | CCA - Signal that the channel is clear to transmit. |
| 23 | PK7 | RADIO_PE - Master power control for the RF section | CAL_EN - Calibration mode enable |
| 15 | PL0 | TX_PE and PA_PE - Transmit Enable to Baseband | TX_PE - Transmit Enable to Baseband |
| 27 | PL1 | RX_PE - Receive Enable to Baseband | RX_PE - Receive Enable to Baseband |
| 26 | PL2 | RESET - Reset to Baseband | RESET_BB - Reset Baseband |
| 28 | PL3 | Not Used | T/R-SW_BAR - Transient/Receive Control (Inverted) |
| 43 | PL4 | MA19 (if required) | MA19 (if required) |
| 12 | PL5 | MA20 (if required) | MA20 (if required) |
| 11 | PL6 | MA21 (if required) | Reserved |
| 93 | PL7 | TX_RDY - Baseband ready to receive data on TXD (not used by firmware) | T/R_SW - Transmit/Receive Control |

### Special Hardware Functions for Port Pins

| | | | |
|---|---|---|---|
| PJ0 | SCK | MMI serial clock in or out | |
| PJ1 | SDO/SDIO | MMI serial data out or I/O | |
| | MOSI | SPI Master Out/Slave In | Also for MicroWire |
| PJ2 | SDI/MISO | MMI serial data in | Or SPI Master In/Slave Out |
| | SDDIR | MMI (SDIO) data direction | Low while SDIO is driven as an output |
| PJ3 | SDE0 | MMI serial device enable 0 | Generally selects PHY controller |
| | PCS- | SPI/MMI transfer qualifier | Asserted by hardware during transfer |
| | PHYCS- | PHY chip select (3-3.5MB) | For memory-mapped PHY controllers |
| PJ4 | SDE1 | MMI serial device enable 1 | For serial EPROM, synthesizer, etc. |
| | SDDQ | MMI data delivery qualifier | Low for data on SDIO, high for address |
| | SS- | SPI slave select | In slave mode SCK is serial clock input |
| PJ5 | MREQ- | MBUS request | |
| PJ6 | MGNT- | MBUS grant | |
| | LED2 | LED 2 driver | (Directly from I/O port) |
| PJ7 | LED1 | LED 1 driver | (Directly from I/O port) |
| PK0 | GPCK | GP serial port clock in or out | |
| | UHSIn | Async handshake in | Indicates external async Rx ready |
| PK1 | GPDO | GP serial port data output | |
| | UTXD | Async transmit data | |
| PK2 | GPDI | GP serial port data input | |
| | URXD | Async receive data | |
| PK3 | GPDS0 | GP device select 0 | |
| | UHSOut | Async handshake out | Indicates GP port async Rx ready |
| PK4 | GPDS1 | GP device select 1 | |
| PK5 | PDA | PHY (or MAC) data available | Qualifies RXD input to MAC controller |
| | UWDET | Unique word detected | Output from MAC controller |
| PK6 | MBUSY | Medium busy | CCA status (PHY-dependent source) |
| | RATE0 | Data Rate select 0 | |
| PK7 | EDET | Energy (or modulation) detect | |
| | RATE1 | Data Rate select 1 | |
| PL0 | TXE | Transmitter enable | |
| PL1 | RXE | Receiver enable | Can drive “awake” LED |
| | PHYSLP | PHY sleep | (Directly from I/O port) |
| PL2 | PHYRES | PHY reset | (Directly from I/O port) |
| PL3 | SLOT | Slot time reference (in or out) | |
| | ANTSEL | Antenna select | (Directly from I/O port) |
| PL4 | MA19 | MBUS address bit 19 | For 1M byte SRAM |
| | LED0 | LED 0 driver | (Directly from I/O port) |
| PL5 | MA20 | MBUS address bit 20 | For 2M byte SRAM |
| PL6 | MA21 | MBUS address bit 21 | For 4M byte SRAM |
| PL7 | TXR | Transmitter ready | |

## Absolute Maximum Ratings

Supply Voltage . . . . . .4V
Input, Output or I/O Voltage . . . . . .GND -0.5V to $V_{CC}$ +0.5V
ESD Classification . . . . . .Class 2

## Operating Conditions

Voltage Range . . . . . .+2.70V to +3.60V
Ambient Temperature Range . . . . . .$0^oC$ to $70^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| LQFP Package | 56 |

Maximum Storage Temperature Range . . . . . -$65^oC$ to $150^oC$
Maximum Junction Temperature . . . . . .$100^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . .$300^oC$
(Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

Maximum test temperature = $100^oC$, $V_{CC}$ = 3.0V to 3.3V ±10%, $T_A$ = -$40^oC$ to $85^oC$

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{CCOP}$ | $V_{CC}$ = 3.6V, CLK Frequency 44MHz | - | 35 | 45 | mA |
| Standby Power Supply Current | $I_{CCSB}$ | $V_{CC}$ = Max, Outputs not Loaded | - | 0.5 | 1 | mA |
| Input Leakage Current | $I_I$ | $V_{CC}$ = Max, Input = 0V or $V_{CC}$ | -10 | 1 | 10 | mA |
| Output Leakage Current | $I_O$ | $V_{CC}$ = Max, Input = 0V or $V_{CC}$ | -10 | 1 | 10 | mA |
| Logical One Input Voltage | $V_{IH}$ | $V_{CC}$ = Max, Min | $0.7V_{CC}$ | - | - | V |
| Logical Zero Input Voltage | $V_{IL}$ | $V_{CC}$ = Min, Max | - | - | $V_{CC}/3$ | V |
| Logical One Output Voltage | $V_{OH}$ | $I_{OH}$ = -1mA, $V_{CC}$ = Min | $V_{CC}$-0.2 | - | - | V |
| Logical Zero Output Voltage | $V_{OL}$ | $I_{OL}$ = 2mA, $V_{CC}$ = Min | - | 0.2 | 0.2 | V |
| Input Capacitance | $C_{IN}$ | CLK Frequency 1MHz. All measurements referenced to GND. $T_A = 25^oC$ | - | 5 | 10 | pF |
| Output Capacitance | $C_{OUT}$ | CLK Frequency 1MHz. All measurements referenced to GND. $T_A = 25^oC$ | - | 5 | 10 | pF |

NOTE: All values in this table have not been measured and are only estimates of the performance at this time.

## AC Electrical Specifications

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **CLOCK SIGNAL TIMING** | | | | | |
| OSC Clock Period (Typ. 44MHz) | $t_{CYC}$ | 22 | 22.7 | 200 | |
| High Period | $t_{H1}$ | 15 | 11.36 | - | |
| Low Period | $t_{L1}$ | 15 | 11.36 | - | |
| Delay from OSC Edge to MCLK Edge | $t_{D1}$ | - | 10 | - | |
| **EXTERNAL MEMORY INTERFACE** | | | | | |
| Rising Edge MCLK to EMA[15:0], EMCSxN, EMOEN, EMWRN | $t_{D1}$ | 0 | - | 10 | ns |
| Width EMOEN | $t_{D2}$ | $2*t_{MCLK}$ - 10 | - | $9*t_{MCLK}$ + 10 | ns |
| EMD[15:0] Read Data Setup | $t_{S1}$ | 10 | - | - | ns |
| EMD[15:0] Read Data Hold | $t_{H1}$ | - | - | 0 | ns |
| Minimum Width between Read and Write | $t_{D3}$ | $t_{MCLK}$ - 10 | $t_{MCLK}$ | $t_{MCLK}$ + 10 | ns |
| Width EMWRN | $t_{D4}$ | $2*t_{MCLK}$ - 10 | - | $9*t_{MCLK}$ + 10 | ns |
| EMWRN Rising to EMCSxN Rising | $t_{D5}$ | $1*t_{MCLK}$ - 10 | $1*t_{MCLK}$ | $1*t_{MCLK}$ + 10 | ns |
| EMD[15:0] Write Data Hold Time to Rising Edge EMWRN | $t_{D6}$ | $1*t_{MCLK}$ - 10 | $1*t_{MCLK}$ | $1*t_{MCLK}$ + 10 | ns |

## AC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SYNTHESIZER** | | | | | |
| SPCLK Period | $t_{CYC}$ | 90 | - | 4,000 | ns |
| SPCLK Width Hi | $t_{H1}$ | $t_{CYC}/2$ - 10 | - | $t_{CYC}/2$ + 10 | ns |
| SPCLK Width Lo | $t_{L1}$ | $t_{CYC}/2$ - 10 | - | $t_{CYC}/2$ + 10 | ns |
| SYNCLE to Rising Edge SPCLK | $t_{D1}$ | 35 | - | - | ns |
| SPDATA Hold Time from Falling Edge of SPCLK | $t_{D2}$ | 0 | - | - | ns |
| SPCLK Falling Edge to SYNLE Inactive | $t_{D3}$ | 35 | - | - | ns |
| **SERIAL PORT - HFA3824A/HFA3860B** | | | | | |
| SPCLK Clock Period | $t_{CYC}$ | 90ns | - | 4µs | |
| High Period | $t_{H1}$, $t_{L1}$ | $t_{CYC}/2$ -10 | - | $t_{CYC}/2$ + 10 | |
| Delay from Clock Falling Edge to SPCSx, SPAS, SPREAD, SPDATA Outputs | $t_{CD}$ | - | 10 | - | ns |
| Setup Time of SPDATA Read to SPCLK Falling Edge | $t_{DRS}$ | 15 | - | - | ns |
| Hold Time of SPDATA Read from SPCLK Falling Edge | $t_{DRH}$ | 0 | - | - | |
| Hold Time of SPDATA Write from SPCLK Falling Edge | $t_{DWH}$ | 0 | - | - | |
| **SYSTEM INTERFACE - PC CARD IO READ 16** | | | | | |
| Data Delay After SIORDN | $t_{DIORD}$ | - | - | 100 | ns |
| Data Hold Following SIORDN | $t_{HIORD}$ | 0 | - | - | ns |
| SIORDN Width Time | $t_{WIORD}$ | 165 | - | - | ns |
| Address Setup Before SIORDN | $t_{SUA}$ | 70 | - | - | ns |
| SCE(1,2)N Setup Before SIORDN | $t_{SUCE}$ | 5 | - | - | ns |
| SCE(1,2)N Hold After SIORDN | $t_{HCE}$ | 20 | - | - | ns |
| SREGN Setup Before SIORDN | $t_{SUREG}$ | 5 | - | - | ns |
| SREGN Hold Following SIORDN | $t_{HREG}$ | 0 | - | - | ns |
| SINPACKN Delay Falling from SIORDN | $t_{DFINPACK}$ | 0 | - | 45 | ns |
| SINPACKN Delay Rising from SIORDN | $d_{DRINPACK}$ | - | - | 45 | ns |
| SIOIS16N Delay Falling from Address | $t_{DFIOIS16}$ | - | - | 35 | ns |
| SIOIS16N Delay Rising from Address | $t_{DRIOIS16}$ | - | - | 35 | ns |
| SWAITN | $t_{DFWT}$ | - | - | 35 | ns |
| Data Delay from SWAITN Rising | $t_{DRWT}$ | - | - | 0 | ns |
| SWAITN Width Time | $t_{WWT}$ | - | - | 12,000 | ns |
| **SYSTEM INTERFACE - PC CARD IO WRITE 16** | | | | | |
| Data Setup Before SIOWRN | $t_{SUIOWR}$ | 60 | - | - | ns |
| Data Hold Following SIOWRN | $t_{HIOWR}$ | 30 | - | - | ns |
| SIOWRN Width Time | $t_{WIOWR}$ | 165 | - | - | ns |
| Address Setup Before SIOWRN | $t_{SUA}$ | 70 | - | - | ns |
| Address Hold Following SIOWRN | $t_{HA}$ | 20 | - | - | ns |
| SCE(1,2)N Setup Before SIOWRN | $t_{SUCE}$ | 5 | - | - | ns |
| SCE(1,2)N Hold Following SIOWRN | $t_{HCE}$ | 20 | - | - | ns |
| SREGN Setup Before SIOWRN | $t_{SUREG}$ | 5 | - | - | ns |
| SREGN Hold Following SIOWRN | $t_{HREG}$ | 0 | - | - | ns |

## AC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SIOIS16N Delay Falling from Address | $t_{DFIOIS16}$ | - | - | 35 | ns |
| SIOIS16N Delay Rising from Address | $t_{DRIOIS16}$ | - | - | 35 | ns |
| SWAITN Delay Falling from IOWRN | $t_{DFWT}$ | - | - | 35 | ns |
| SWAITN Width Time | $t_{WWT}$ | - | - | 12,000 | ns |
| SIOWRN High from SWAITN High | $t_{DRIOWR}$ | 0 | - | - | ns |
| **RADIO TX DATA - TX PATH** | | | | | |
| TXC Rising to TXD | $t_{DTXD}$ | - | - | 10 | ns |
| TXC Period | $t_{TXC}$ | 4* $t_{TMCK}$ | - | - | ns |
| TXC Width Hi | $t_{CHM}$ | 31 | - | - | ns |
| TXC Width Lo | $t_{CLM}$ | 31 | - | - | ns |
| MCLK Period | $t_{tMCK}$ | 22.7 | - | - | ns |
| TXC Rising to TX_PE2 Deassert (See Note 9) | $t_{DTX\_PE2}$ | - | TBD | TBD | ns |
| TX_RDY Assert Before TXC Rising | $t_{TX\_RDY}$ | 10 | - | - | ns |
| TX_RDY Hold After TXC Rising (See Note 2) | $t_{TX\_RDYH}$ | 0 | - | - | |
| **RADIO RX DATA - RX PATH** | | | | | |
| RX_RDY Setup Time to RXC Positive Edge (See Note 3) | $t_{SURX\_RDY}$ | 10 | - | - | ns |
| RX_RDY Hold Time from RXC Positive Edge (See Note 4) | $t_{HRX\_RDY}$ | 45 | - | - | ns |
| RX_PE2 Delay from RX_RDY deAssert (See Note 8) | $t_{DRX\_PE2}$ | - | 3 * $t_{MCLK}$ | - | ns |
| RX_PE2 Low Pulse Width (See Note 7) | $t_{WRX\_PE2}$ | - | 4 * $t_{MCLK}$ | - | ns |
| RXD Setup Time to RXC Positive Edge (See Note 5) | $t_{SURXD}$ | 10 | - | - | ns |
| RXD Hold Time from RXC Positive Edge (See Note 5) | $t_{HRXD}$ | 0 | - | - | ns |
| RXC Period (See Note 9) | $t_{RXC}$ | - | 3 * $t_{MCLK}$ | - | ns |
| MCLK Period | $t_{MCLK}$ | 22.7 | - | - | ns |
| RXC Width Hi | $t_{RCHM}$ | 31 | - | - | ns |
| RXC Width Lo | $t_{RCLM}$ | 31 | - | - | ns |

NOTES:

2. TX_RDY is and'd with TXC_ONE_SHOT to shift data in shift register. However, once the last data bit is put on TXD output pin no further shifting of bits is required. In addition, TX_RDY remains asserted until TX_PE2 is de-asserted which occurs several MAC MCLK's after the last data bit is shifted into the BBP TX_PORT. Therefore, 0ns hold time is required for this signal.
   TX_RDY is used by the BBP to signal that the PLCP header and preamble have been generated and the MAC must provide the MPDU data. TX_RDY will remain asserted until TX_PE2 is deasserted by the MAC.
   TX_PE2 is async to the TX_PORT.
3. MD_RDY is and'd with RXC_ONE_SHOT (RXDAV) to shift data in shift register. RX_RDY is not required to be valid until 1 MCLK after RXC is sampled high. Therefore, a negative setup time could be used. Since this is an unlikely scenario, we will leave it at a nominal 10ns setup time.
4. MD_RDY is and'd with RXC_ONE_SHOT (RXDAV) to shift data in shift register. Therefore, for the last data bit, the MD_RDY must be held active until RXC_ONE_SHOT is sampled high by MAC's MCLK. However, it is assumed that BBP will be used in a mode that keeps RX_RDY (MD_RDY) and RXC running until RX_PE2 is de-asserted. The MAC will stop processing data after the number of bits retrieved from the PLCP header length field are received. THEREFORE, the RX_RDY hold time with respect to RXC does not matter. However, should the RX_RDY signal be cleared when the last RXD bit is received the hold time w/r RXC must be honored.
5. RXC positive edge clocks a flop which stores the RXD for internal usage.
6. RXC period (and Hi/Lo times) must be long enough for flops clocked by MAC MCLK to see 1 RXC high and 1 RXC low. Since RXC can be async to MAC MCLK it is assumed that 3 MCLK periods will suffice.
7. RX_PE inactive width at BBP is 3 BBP MCLK's. Since BBP MCLK and MAC MCLK can be async minimum should be 4 MAC MCLK's.
8. Not yet verified, but seems reasonable. When RX_RDY drops before expected number of RXD bits is received, then Tx/Rx FSM in mpctl.v signals timers which clear rx_pe2_int. More of a functional spec than a timing spec.
9. Need to sample 1 RXC high and 1 RXC low with MAC MCLK.

## Waveforms

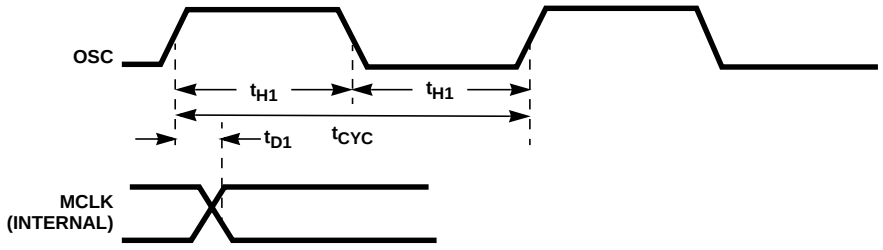
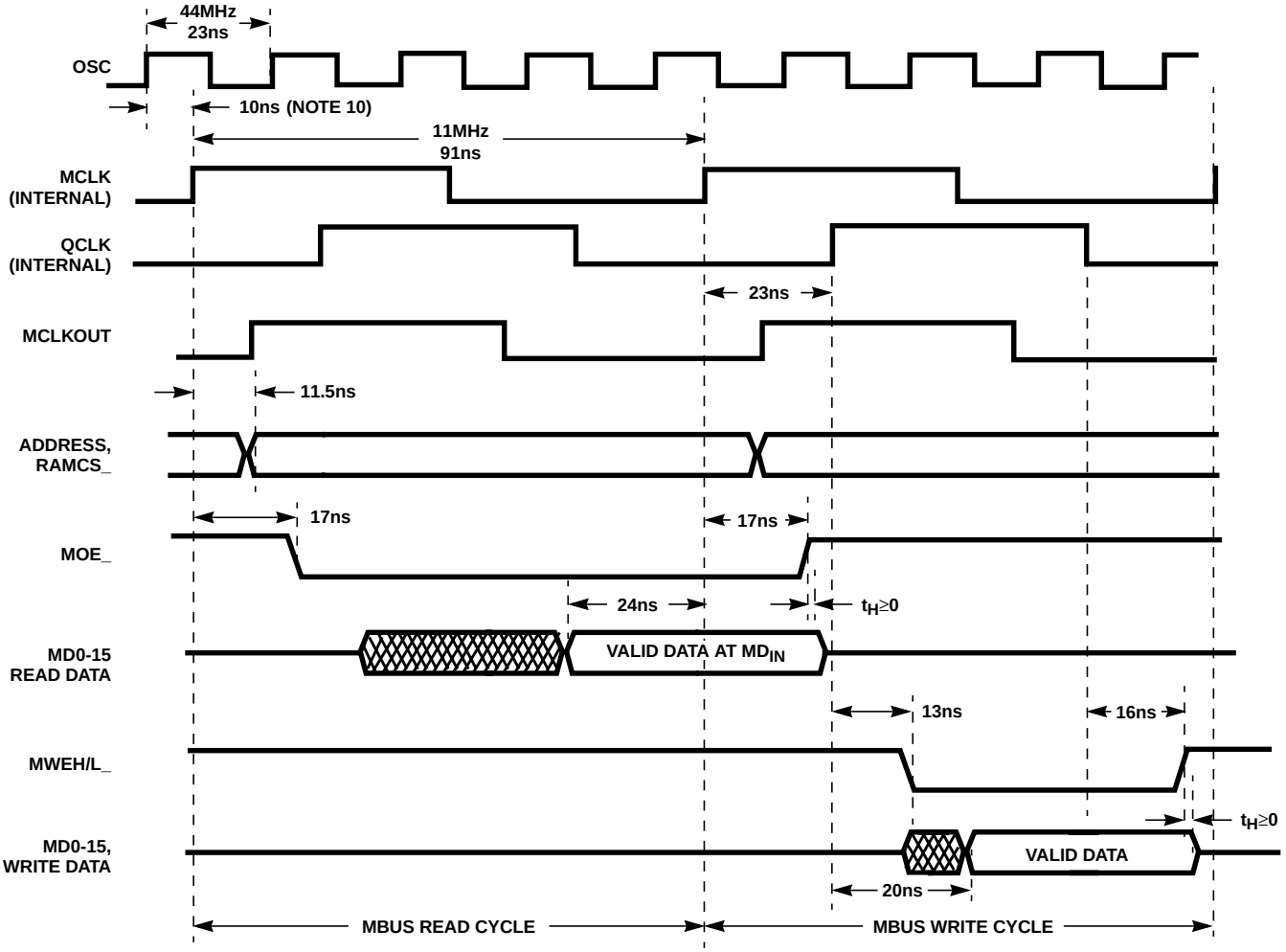



FIGURE 1. CLOCK SIGNAL TIMING

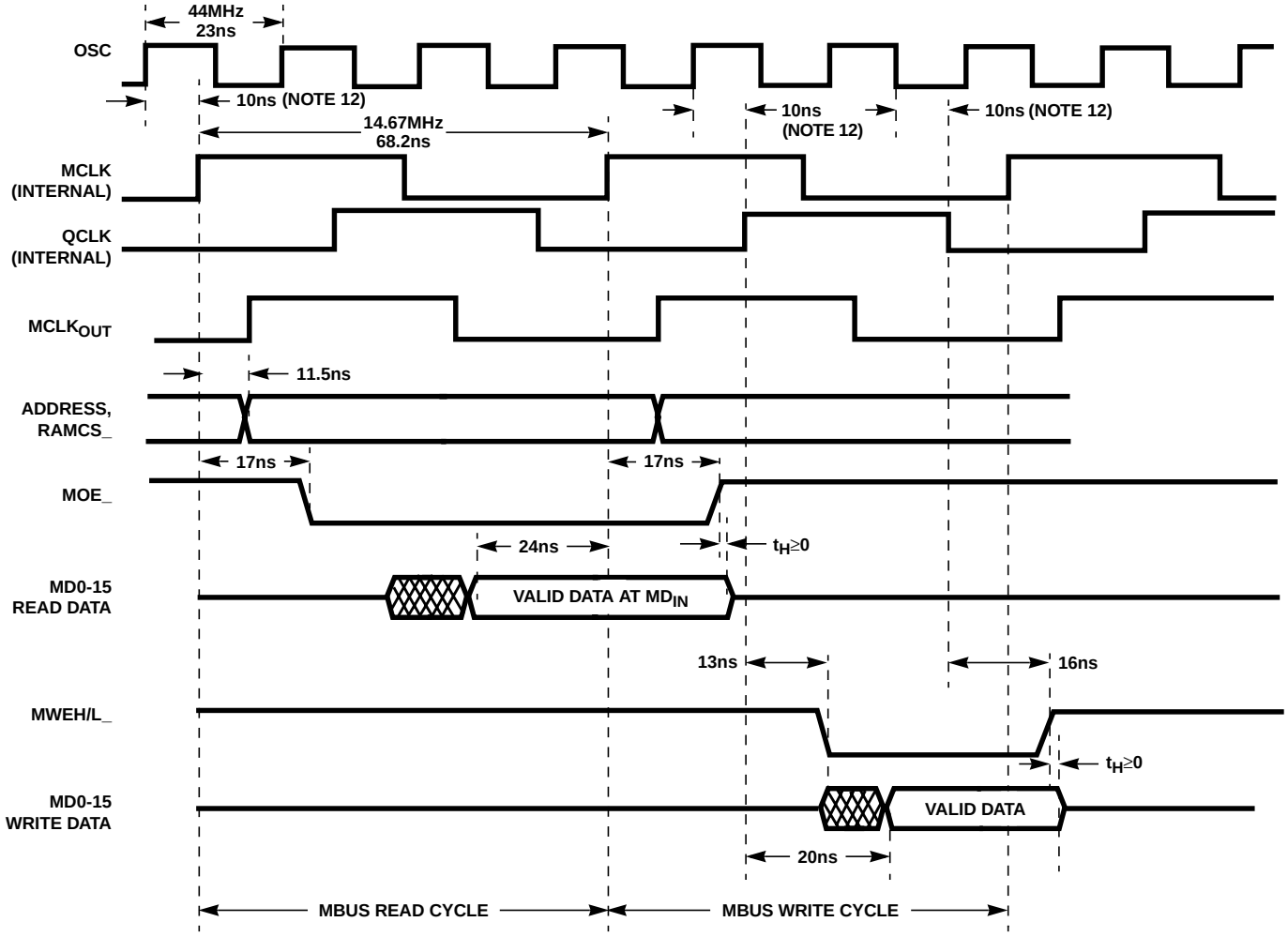



NOTE:

10. Timing delays between OSC and internal clocks are shown for information purposes only.

FIGURE 2. MBUS MEMORY TIMING - 11MHz MCLK

## Waveforms (Continued)




NOTES:

11. 14.67MHz requires an odd divisor in the prescaler. Note that both edges of OSC are used to create MCLK and QCLK, thus a deviation from 50% duty cycle in OSC will result in corresponding changes in MBUS timing.

12. Timing delays between OSC and internal clocks are shown for information purposes only.

**FIGURE 3. MBUS MEMORY TIMING - 14.67MHz MCLK**

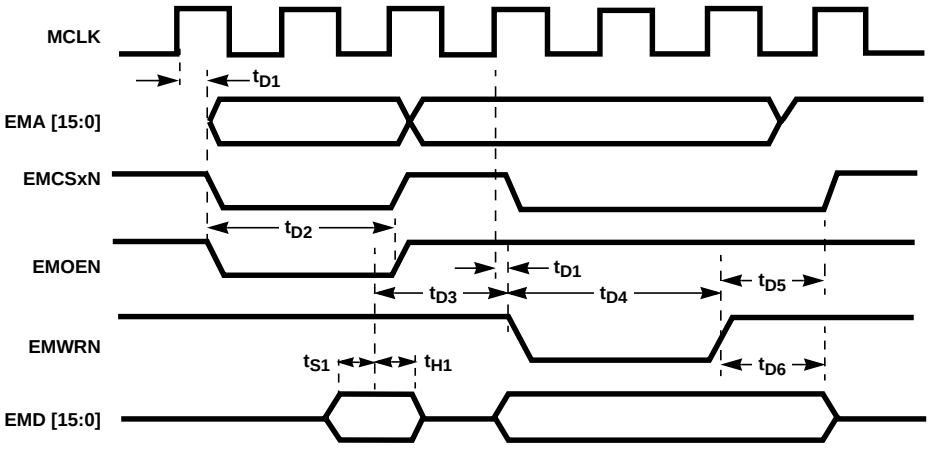



**FIGURE 4.**

## Waveforms (Continued)

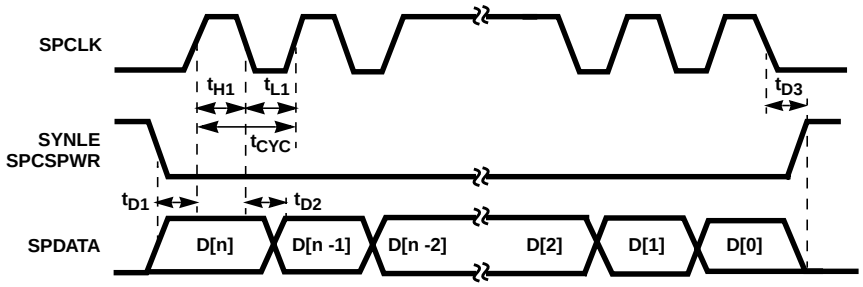



FIGURE 5. SYNTHESIZER

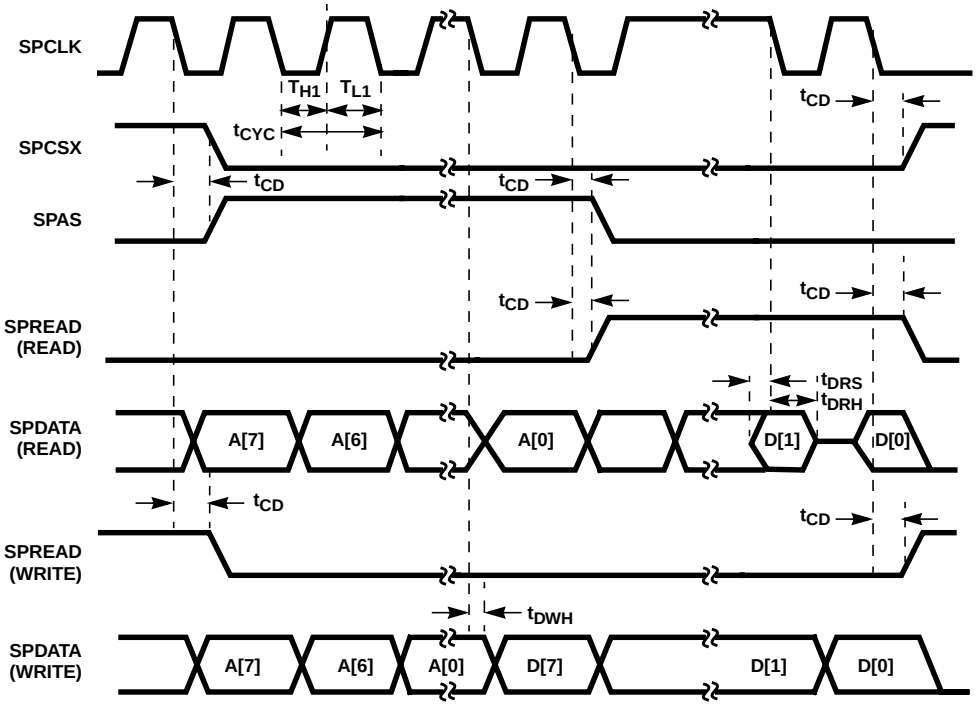



FIGURE 6. SERIAL PORT - HFA3824A/HFA3860B

## Waveforms (Continued)

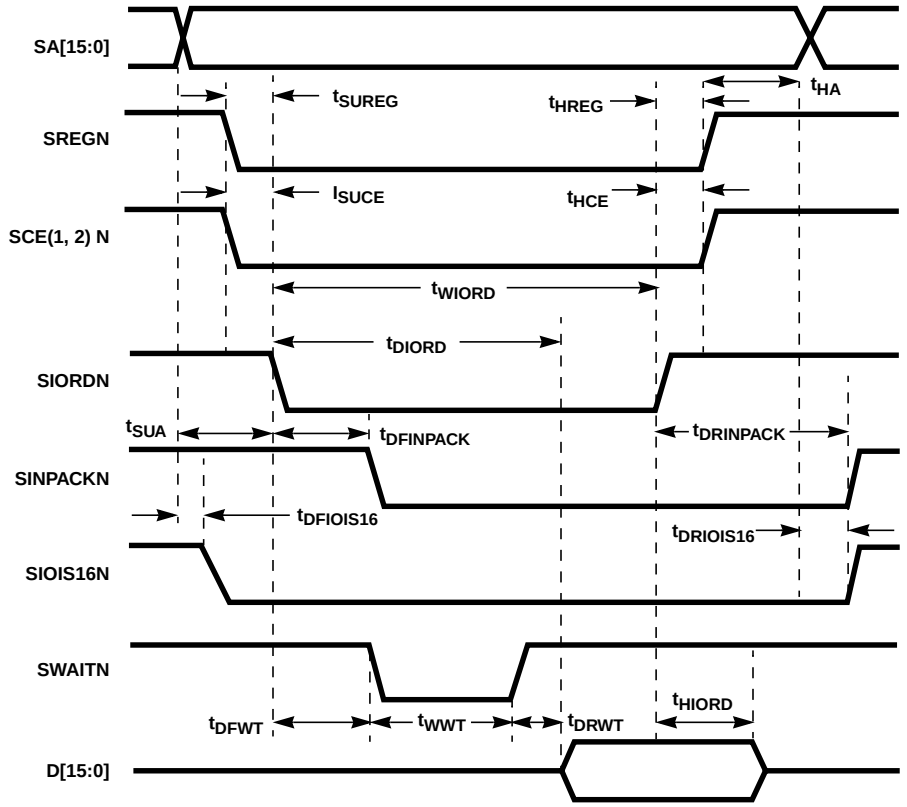



FIGURE 7. PC CARD IO READ 16

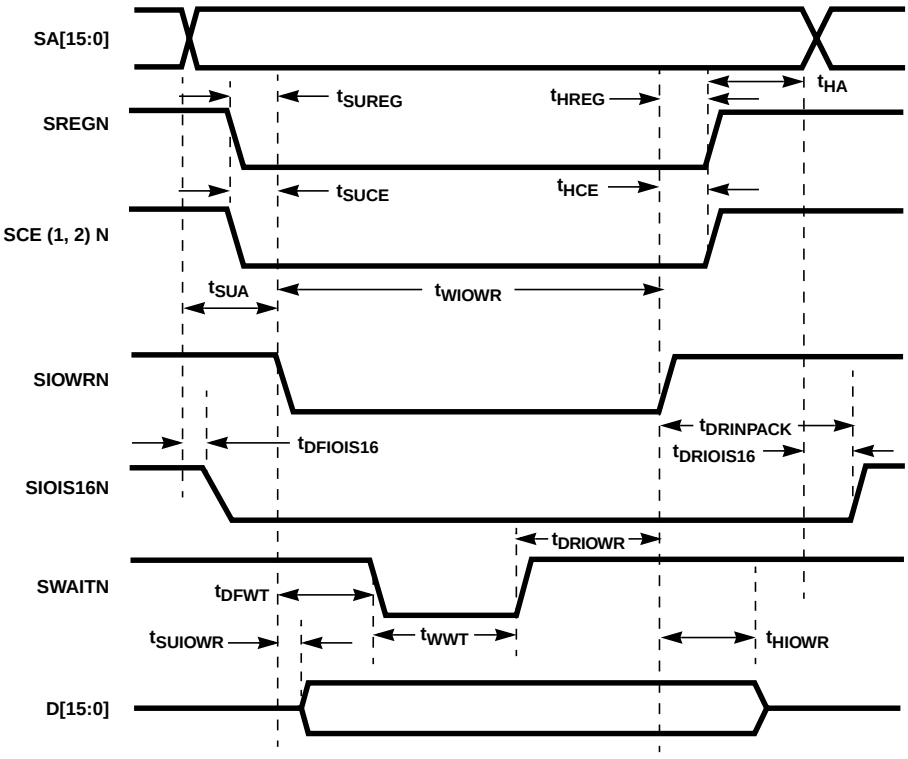



FIGURE 8. PC CARD IO WRITE 16

## Waveforms (Continued)

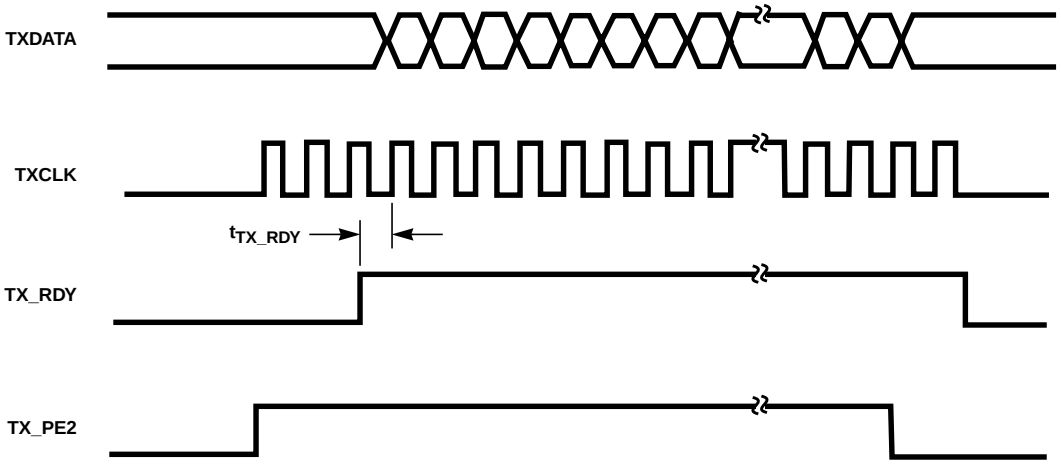



FIGURE 9. TX PATH

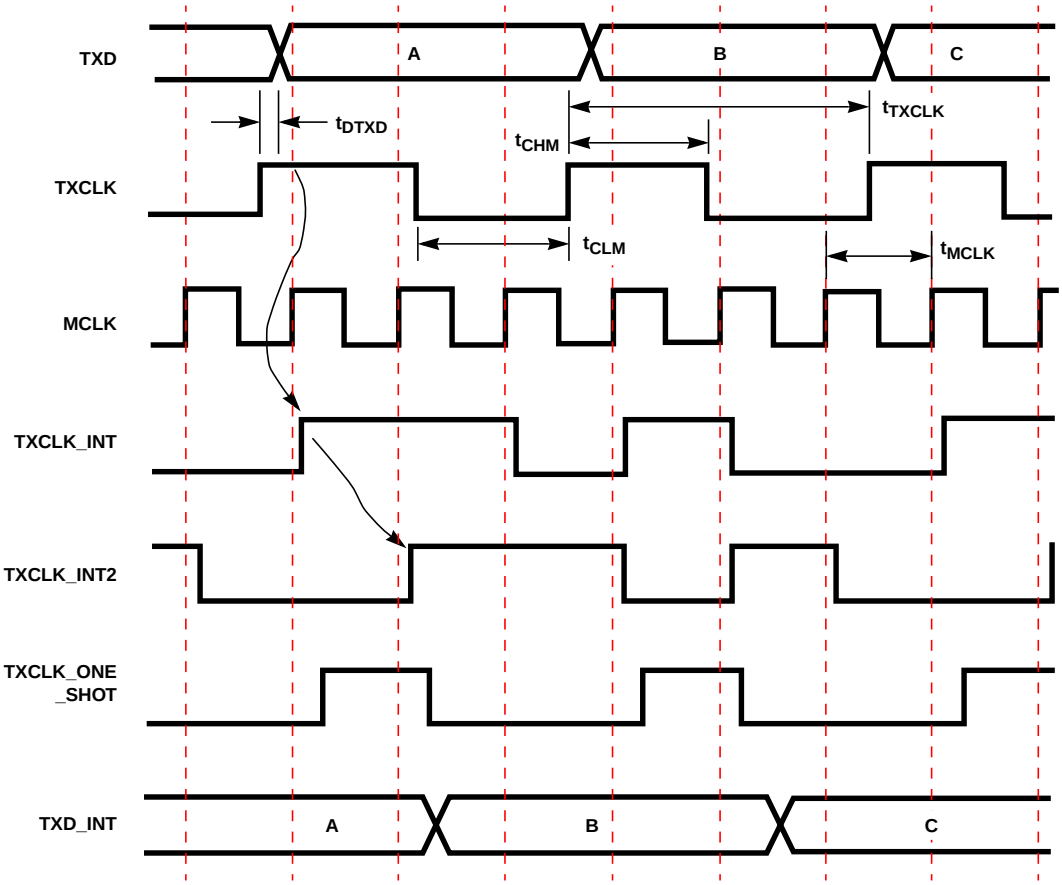



FIGURE 10.

## Waveforms (Continued)

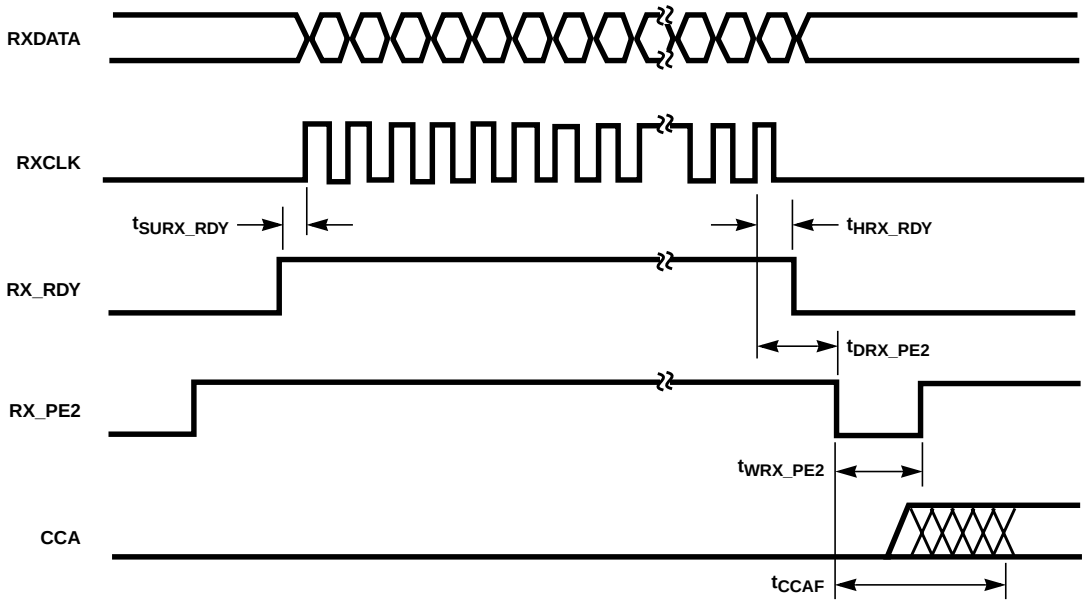



FIGURE 11. RX PATH

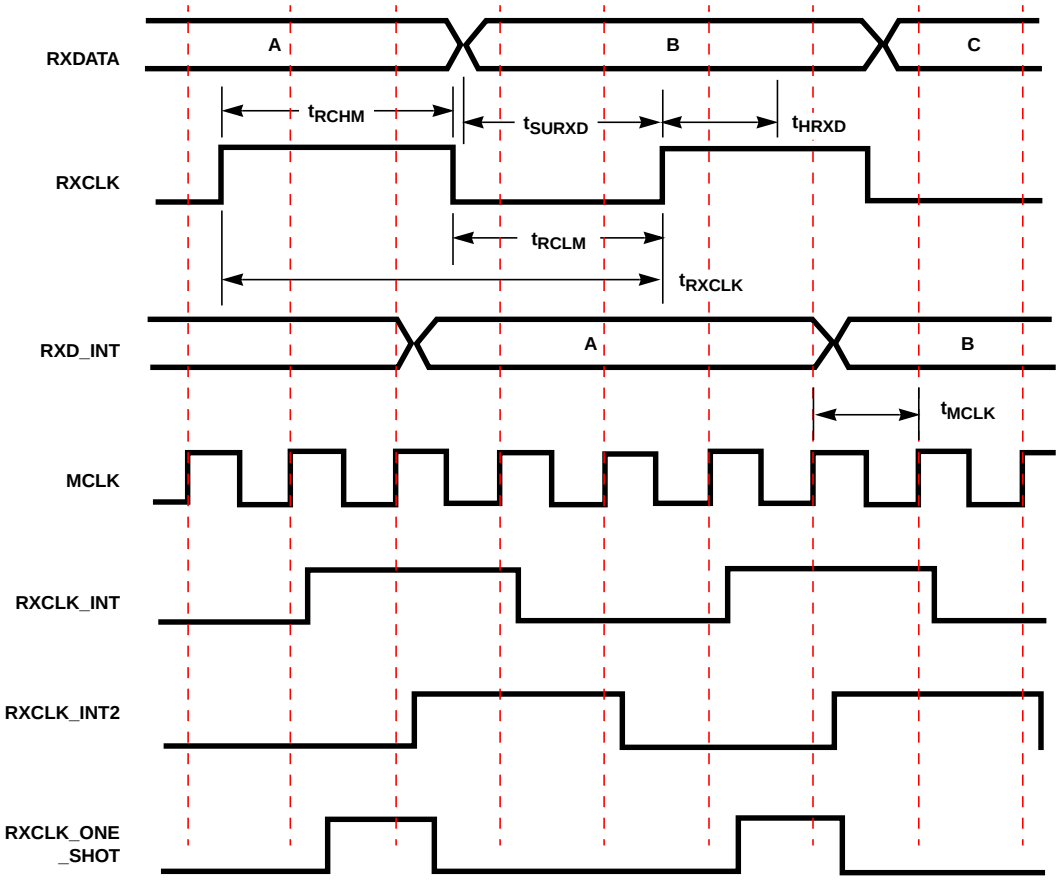



FIGURE 12.

## HFA3841 System Overview

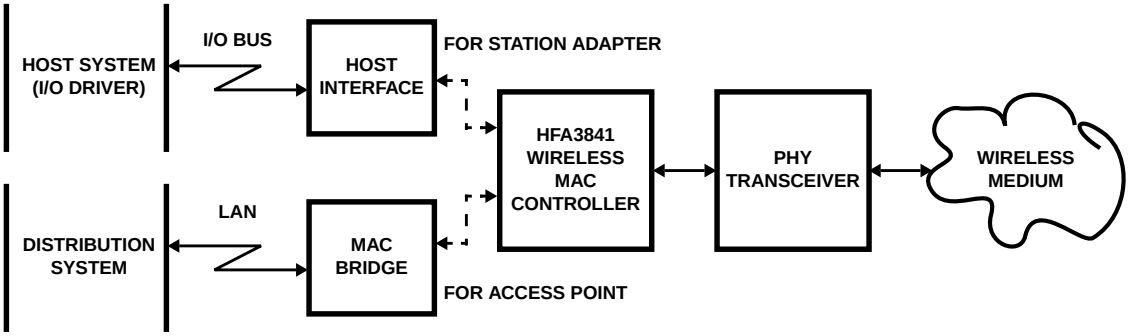



FIGURE 13. TYPICAL APPLICATION

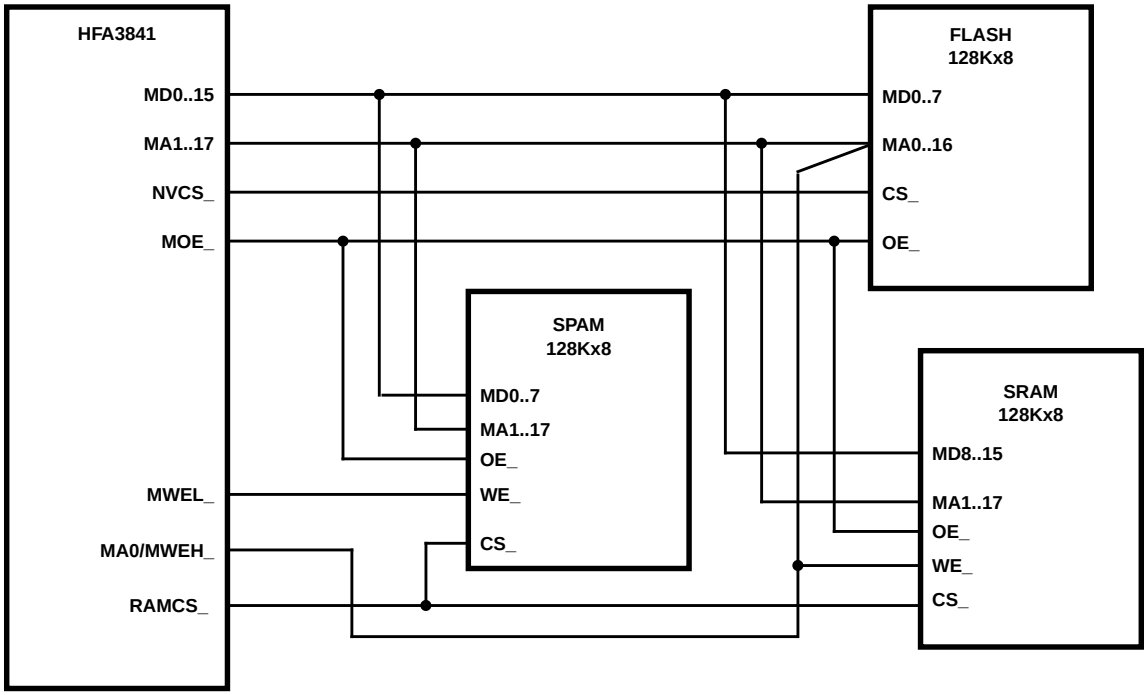



FIGURE 14.

## External Memory Interface

An external memory space is provided for firmware and for buffers that are used for temporary storage of received and transmitted frames.

The total memory space is 4M bytes. 64K words are used for control store, where firmware is located. The high data bus has weak pull-up resistors so that external pull-down resistors can set the configuration of the HFA3841 during reset.

NVCS- is the enable to the Flash memory device. Typically the contents of the Flash are copied entirely into SRAM at initialization, and then rarely if ever accessed during normal operation. For this reason, it is acceptable to use low cost, slow Flash devices. During initialization, the clock prescaler is set to produce a longer cycle time while the Flash is accessed. Once all the data has been copied, execution jumps into SRAM and the clock is raised to the normal operating frequency.

It is possible to operate without a Flash device. In such a system, the firmware must be downloaded through the host interface before operation can commence.

The external SRAM memory must be organized in a 16-bit width to provide adequate performance to implement the 802.11 protocol at 11Mb/s rates. Systems designed for lower performance applications may be able to use 8-bit wide memory.

The minimum implementation of external memory consists of 128K bytes of SRAM organized as 64K x 16. Typical applications will use 256K bytes organized as 128K x 16. An access point application could make use of the full address space of the device with 4M bytes organized as 2M x 16.

The HFA3841 was designed to implement 16-bit wide memory by using two 8-bit RAM chips. The HFA3841 provides high and low write enable signals (MWEH_ and MWEL_), and a single output enable (MOE_). This allows a direct connection, enabling a pair of 8-bit SRAMs to function as a 16-bit device. MA0 functions as Address 0 for 8-bit access (such as Flash), and as MWEH (High Byte Write Enable) for 16-bit access (such as SRAM), since address bit 0 is not used for 16-bit accesses.

Some single chip 16-bit SRAMs use an alternate connection scheme with five pins: a Chip Select, an Output Enable, a single Write Enable, and Upper and Lower byte enables, which control both read and write cycles. Thus, external logic is required to generate the required signals.

See Application Note AN9844, "HFA3841 to PRISMII Connections" for important information regarding the connection of these types of 16-bit SRAM chips to the HFA3841.

## Host Interface

### PC Card Physical Interface

The Host interface is compatible to the PC Card 95 Standard (PCMCIA v2.1). The HFA3841 Host Interface pins connect directly to the correspondingly named pins on the PC Card connector with no external components (other than resistors) required. The HFA3841 operates as an I/O card using less than 64 octet locations. Reads and writes to internal registers and buffer memory are performed by I/O accesses. Attribute memory (256 octets) is provided for the CIS table which is located in external memory. Common memory is not used.

The following describes specific features of various pins:

**HA[9:0]**

Decoding of the system address space is performed by the HCEx-. During I/O accesses HA[5:0] decode the register. HA[9:6] are ignored when the internal HAMASK register is set to the defaults used by the standard firmware. During attribute memory accesses HA[9:1] are used.

**HD[15:0]**

The host interface is primarily designed for word accesses, although all byte access modes are fully supported. See HCE1-, HCE2- for a further description. Note that attribute memory is specified for and operates with even bytes accesses only.

**HCE1-, HCE2-**

The PC Card cycle type and width are controlled with the CE signals. Word and Byte wide accesses are supported, using the combinations of HCE1-, HCE2-, and HA0 as specified in the PC Card standard.

**HWE-, HOE-**

HOE- and HWE- are only used to access attribute memory. Common Memory, as specified in the PC Card standard, is not used in the HFA3841. HOE- is the strobe that enables an attribute memory read cycle. HWE- is the corresponding strobe for the attribute memory write cycle. The attribute space contains the Card Information Structure (CIS) as well as the Function Configuration Registers (FCR).

**HIORD-, HIOWR-**

HIORD- and HIOWR- are the enabling strobes for register access cycles to the HFA3841. These cycles can only be performed once the initialization procedure is complete and the HFA3841 has been put into IO mode.

**HREG-**

This signal must be asserted for I/O or attribute cycles. A cycle with HREG- unasserted will be ignored as the HFA3841 does not support common memory.

**HINPACK-**

This signal is asserted by the HFA3841 whenever a valid I/O read cycle takes place. A valid cycle is when HCE1-, HCE2-, HREG-, and HIORD- are asserted, once the initialization procedure is complete.

**HWAIT-**

Wait states are inserted in accesses using HWAIT-. The host interface synchronizes all PC Card cycles to the internal HFA3841 clock. The following wait states should be expected:

**Direct Read or Write to Hardware Register**

- 1/2 to 1 MCLK assertion of HWAIT- for internal synchronization.

**Write to Memory Mapped Register, Buffer Access Path, or Attribute Space (Post-Write)**

- The data required for the write cycle will be latched and therefore only the synchronizing wait state will occur.
- Until the queued cycle has actually written to the memory, any subsequent access by the Host will result in a WAIT.

**Read to Attribute Space and Memory Mapped Registers**

- WAIT will assert until the memory arbitration and access have completed.

**Buffer Access Paths, BAP0 and BAP1**

- An internal Pre-Read cycle to memory is initiated by a host Buffer Read cycle, after the internal address pointer has auto-incremented. If the next host cycle is a read to the same buffer, the data will be available without a memory arbitration delay.
- A single register holds the pre-read data. Thus, any read access to any other memory-mapped register (or the other

buffer access path) will result in the pre-read data becoming invalidated.

- If another read cycle has invalidated the pre-read, then a memory arbitration delay will occur on the next buffer access path read cycle.

**HIREQ-**

Immediately after reset, the HIREQ- signal serves as the RDY/BSY (per the PC Card standard). Once the HFA3841 firmware initialization procedure is complete, HIREQ- is configured to operate as the interrupt to the PC Card socket controller. Both Level Mode and Pulse Mode interrupts are supported. By default, Level mode interrupts are used, so the interrupt source must be specifically acknowledged or disabled before the interrupt will be removed.

**HRESET**

When reset is removed, the CIS table is initialized and, once complete, HIREQ- is set high (HIREQ- acts as RDY/BSY from reset and is set high to indicate the card is ready for use). The CIS table resides in Flash memory and is copied to RAM during firmware initialization. The host system can then initialize the card by reading the CIS information and writing to the configuration register.

### *ISA PnP*

The HFA3841 can be connected to the ISA bus and operate in a Plug and Play environment with an additional chip such as the Fujitsu MB86703, Texas Instruments TL16PNP200A, or Fairchild Semiconductor NM95MS15. See the Application Note AN9874, "ISA Plug and Play with the HFA3841" for more details.

### *Register Interface*

The logical view of the HFA3841 from the host is a block of 32 word wide registers. These appear in IO space starting at the base address determined by the socket controller. There are three types of registers.

**HARDWARE REGISTERS (HW)**

- 1 to 1 correspondence between addresses and registers.
- No memory arbitration delay, data transfer directly to/from registers.
- AUX base and offset are write-only, to set up access through AUX data port.
- Note: All register cycles, including hardware registers, incur a short wait state on the PC Card bus to insure the host cycle is synchronized with the HFA3841's internal MCLK.

**MEMORY MAPPED REGISTERS IN DATA RAM (MM)**

- 1 to 1 correspondence.
- Requires memory arbitration, since registers are actually locations in HFA3841 memory.
- Attribute memory access is mapped into RAM as Base-address + 0x400.
- AUX port provides host access to any location in HFA3841 RAM (reserved).

**BUFFER ACCESS PATH (BAP)**

- No 1 to 1 correspondence between register address and memory address (due to indirect access through buffer address pointer registers).
- Auto increment of pointer registers after each access.
- Require memory arbitration since buffers are located in HFA3841 memory.
- Buffer access may incur additional delay for Hardware Buffer Chaining.

| I/O OFFSET | NAME | TYPE |
|---|---|---|
| 00 | Command | MM |
| 02 | Param0 | MM |
| 04 | Param1 | MM |
| 06 | Param2 | MM |
| 08 | Status | MM |
| 0A | Resp0 | MM |
| 0C | Resp1 | MM |
| 0E | Resp2 | MM |
| 10 | InfoFID | MM |
| 20 | RxFID | MM |
| 22 | AllocFID | MM |
| 24 | TxComplFID | MM |
| 18 | BAP Select0 | MM |
| 1C | BAP Offset0 | MM |
| 36 | BAP Data0 | BAP |
| 1A | BAP Select1 | MM |
| 1E | BAP Offset1 | MM |
| 38 | BAP Data1 | BAP |
| 30 | EvStat | HW |
| 32 | IntEn | HW |
| 34 | EvAck | HW |
| 14 | Control | MM |
| 28 | SwSupport0 | MM |
| 2A | SwSupport1 | MM |
| 2C | SwSupport2 | MM |
| 3A | AuxBase | HW |
| 3C | AuxOffset | HW |
| 3E | AuxData | (reserved) |

### Buffer Access Paths

The HFA3841 has two independent buffer access paths, which permits concurrent read and write transfers. The firmware provides dynamic memory allocation between Transmit and Receive, allowing efficient memory utilization. On-the-fly allocation of (128-byte) memory blocks as needed for reception wastes minimal space when receiving fragments. The HFA3841 hides management of free memory from the driver, and allows fast response and minimum data copying for low latency. The firmware provides direct access to TX and RX buffers based on Frame ID (FID). This facilitates Power Management queuing, and allows dynamic fragmentation and defragmentation by controller. Simple Allocate/Deallocate commands insure low host CPU overhead for memory management.

Hardware buffer chaining provides high performance while reading and writing buffers. Data is transferred between the host driver and the HFA3841 by writing or reading a single register location (The Buffer Access Path, or BAP). Each access increments the address in the buffer memory. Internally, the firmware allocates blocks of memory as needed to provide the requested buffer size. These blocks may not be contiguous, but the firmware builds a linked list of pointers between them. When the host driver is transferring data through a buffer access path and reaches the end of a physical memory block, hardware in the host interface follows the linked list so that the buffer access path points to the beginning of the next memory block. This process is completely transparent to the host driver, which simply writes or reads all buffer data to the same register. If the host driver attempts to access beyond the end of the allocated buffer, subsequent writes are ignored, and reads will be undefined.

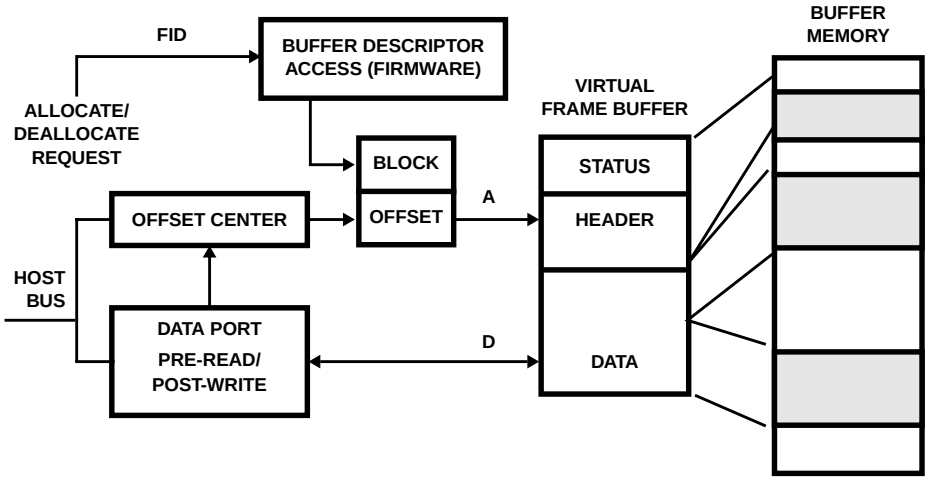



FIGURE 15. BLOCK DIAGRAM OF A BUFFER ACCESS PATH

## PHY Interface

The HFA3841 is intended to support the PRISM family of Baseband processors with no additional components. This family currently includes the HFA3860B and HFA3861 DSSS baseband processors and the other ICs in the PRISM WLAN chip set. (Other baseband processors may be supported with custom firmware. See your sales representative for more information). The HFA3841 interfaces to the HFA386X baseband processors through two serial interfaces. The Modem Management Interface (MMI) is used to read and write internal registers in the baseband processor and access per-packet PLCP information. The Modem Data Interface (MDI) provides the receive and transmit data paths which transfer the actual MPDU data.

### Serial Control Port (MMI)

The HFA3841 has a serial port that is used to program the baseband processor. There are individual chip selects and shared clock and data lines.

The MMI is used to program the registers and functionality of the PHY baseband processor.

#### PHY BASEBAND PROCESSOR

The PHY baseband processor is programmed by HFA3841 firmware.

The PRISM II baseband processor mode works as follows:

The Control Port consists of 4 signals: SD (serial data), SCLK (serial clock), R/W (read/write) and CS_BAR (active-low chip select).

Control Port signaling for read and write operations is illustrated in Figures 16 and 17 respectively. Detailed timing relationships appear in Figure 18 and timing specifications are contained in Table 1.

The BBP always uses the rising edge when clocking data on the Control Port. This means that when the BBP is receiving data it uses the rising edge of clock to sample; when driving data, transitions occur on the rising edge.

Address bits 6 through 1 are significant for selecting configuration registers. Address bits 7 and 0 are unused. See the BBP Programming section for register addresses and suggested values.

For read operations, the rising edge of R/W must occur after the 7th but prior to the 8th rising edge of SCLK. This ensures that the first data bit is clocked out of the BBP prior to the edge used to clock it into the MAC.

For more detailed information on the Control Port and BBP register programming see the HFA386x data sheets.

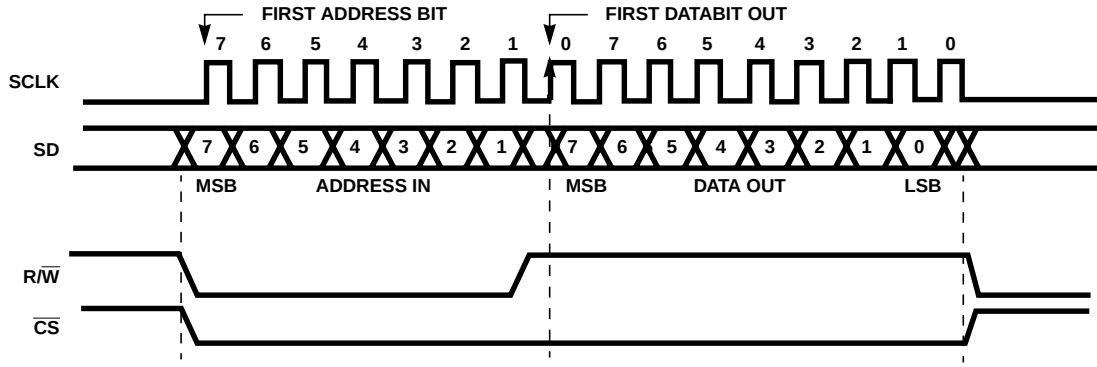



FIGURE 16. PRISM II BASEBAND PROCESSOR CONTROL PORT READ TIMING

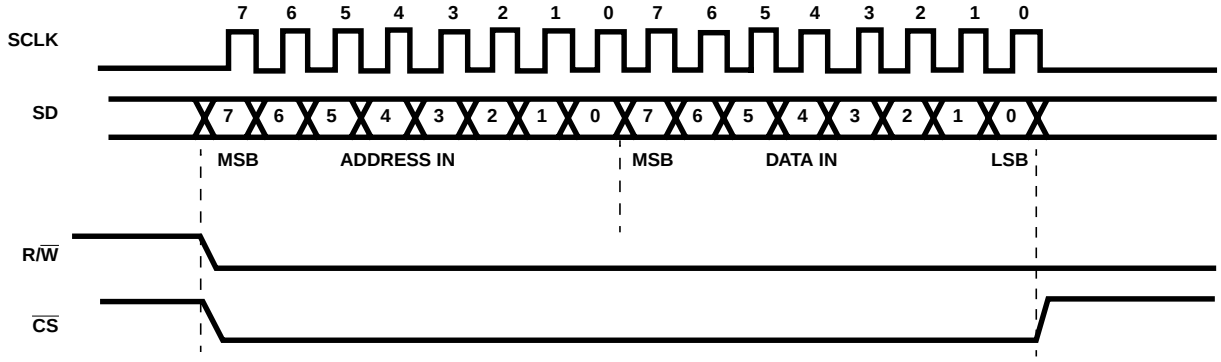



FIGURE 17. PRISM II BASEBAND PROCESSOR SERIAL CONTROL PORT WRITE TIMING

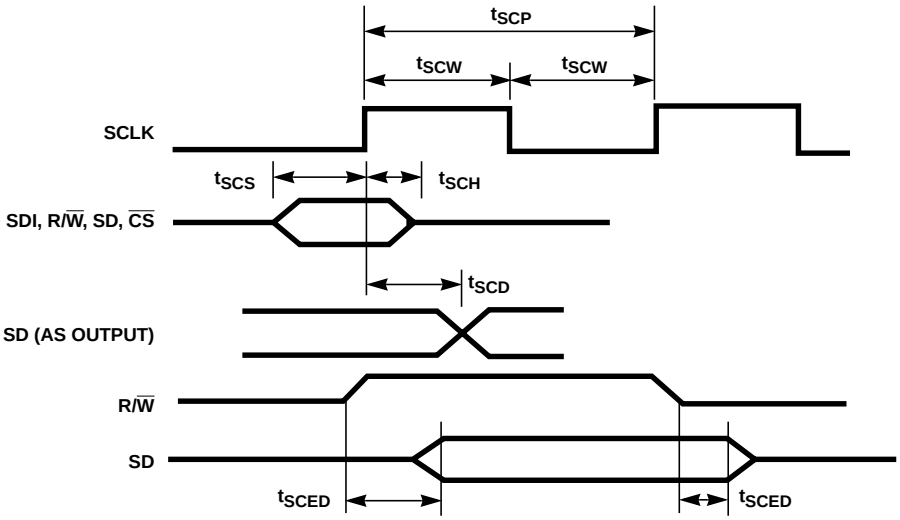



FIGURE 18. BBP CONTROL PORT SIGNAL TIMING

TABLE 1. BBP CONTROL PORT AC ELECTRICAL SPECIFICATIONS

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| SCLK Clock Period | $t_{SCP}$ | 90 | - | ns |
| SCLK Width Hi or Low | $t_{SCW}$ | 20 | - | ns |
| Setup to SCLK + Edge (SD, SDI, R/W, CS) | $t_{SCS}$ | 30 | - | ns |
| Hold Time from SCLK + Edge (SD, SDI, R/W, CS) | $t_{SCH}$ | 0 | - | ns |
| SD Out Delay from SCLK + Edge | $t_{SCD}$ | - | 30 | ns |
| SD Out Enable/Disable from R/W | $t_{SCED}$ | - | 15 | ns |

## SYNTHESIZER

For the PRISM II, the synthesizer is programmed by firmware using different pins than the MMI. The HFA3841 will exchange data with the baseband during transmit and receive operations over the MMI interface. If the MMI interface was connected to the front end chips, the transitions on SCLK and SD could couple noise into them. The synthesizer serial bus consists of SYNTHDATA, SYNTHCLK, LE_IF and LE_RF. SYNTHDATA is on pin PK2, SYNTHCLK is on PK1, LE_IF is the enable for the HFA3783 Quad IF chip, and LE_RF is the enable for the HFA3683 synthesizer.

Data is provided on SYNTHDATA and clock on SYNTHCLK. The data is updated the falling edge of SYNTHCLK and expected to be latched into the synthesizer on the rising edge. The enable signal LE_RF is asserted while data is clocked out.

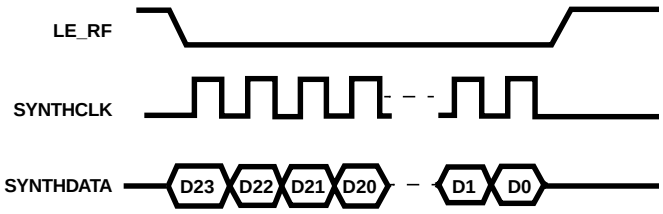



FIGURE 19. SYNTHESIZER DATA FORMAT

### *PHY Data Interface (MDI)*

The HFA3841 has a dedicated serial port to provide the data interface to the baseband processor. This is referred to as the Modem Data Interface (MDI). The MDI operates on the data being transferred to and from the baseband on a word by word basis. There are no FIFOs needed, since the firmware is able to control the protocol in real time.

The MDI performs the following functions:

- Serial to parallel conversion of received data from the baseband, with synchronization between the incoming RX clock to the internal HFA3841 clock.
- Generating CRCs (HEC and FCS) from the received data stream to verify correct reception.
- Decrypt the received data when WEP is enabled.
- Parallel to serial conversion of transmit data, with the serial timing synchronized with the TX clock.
- Insertion of the CRCs (HEC and FCS) at the appropriate point during transmission.
- Encrypt the transmitted data when WEP is enabled.

The receive data path uses RX_RDY, RXC, RXD. The transmit data path uses TX_RDY, TXC, TXD and the CCA input to determine (under the IEEE802.11 protocol) whether to transmit.

In transmit mode, the HFA386X is used in the mode where it generates the PLCP header internally and only the MPDU is passed from HFA3841. In receive, the HFA386X is used in the mode where it passes the PLCP header and the MPDU to the HFA3841.

**BBP Packet Reception**

There are 4 signals associated with the BBP Receive Port: RX_PE (receive enable), MDRDY (receive ready), RXD (receive data), and RXCLK (receive clock). These connect to the HFA3841 on pins PL1, PK5, RXD, and RXC, respectively.

The receive demodulator in the BBP is activated via RX_PE. When RX_PE goes active the demodulator scrutinizes I and Q for packet activity. When a packet arrives at a valid signal level the demodulator acquires and tracks the incoming signal. It then sifts through the demodulator data for the Start Frame Delimiter (SFD). Normally, MDRDY is programmed to go active after SFD is detected. This signals the HFA3841, allowing it to pick off the needed header fields from the real-time demodulated bitstream rather than having to read these fields through the BBP Control Port.

Assuming all is well with the header, the BBP decodes the signal field in the header and switches to the appropriate data rate. If the signal field is not recognized, or the CRC16 is in error, then MDRDY will go inactive shortly after CRC16 and the demodulator will return to acquisition mode looking for another packet. If all is well with the header, and after the demodulator has switched to the appropriate data rate, then the demodulator will continue to provide data to the HFA3841 indefinitely.

Receive Port exchange details are depicted in Figure 20. Detailed timing is related in Figure 21 and Table 2.

For more detailed information concerning BBP packet reception see the HFA386x data sheets.

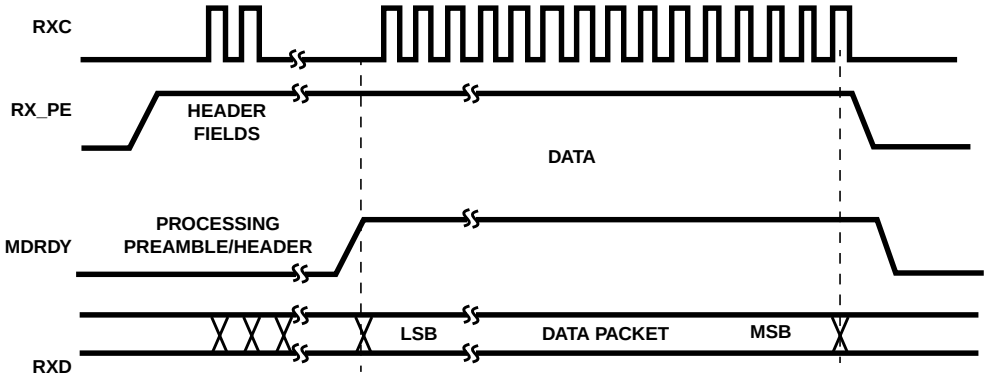



**FIGURE 20. BBP RECEIVE PORT TIMING**

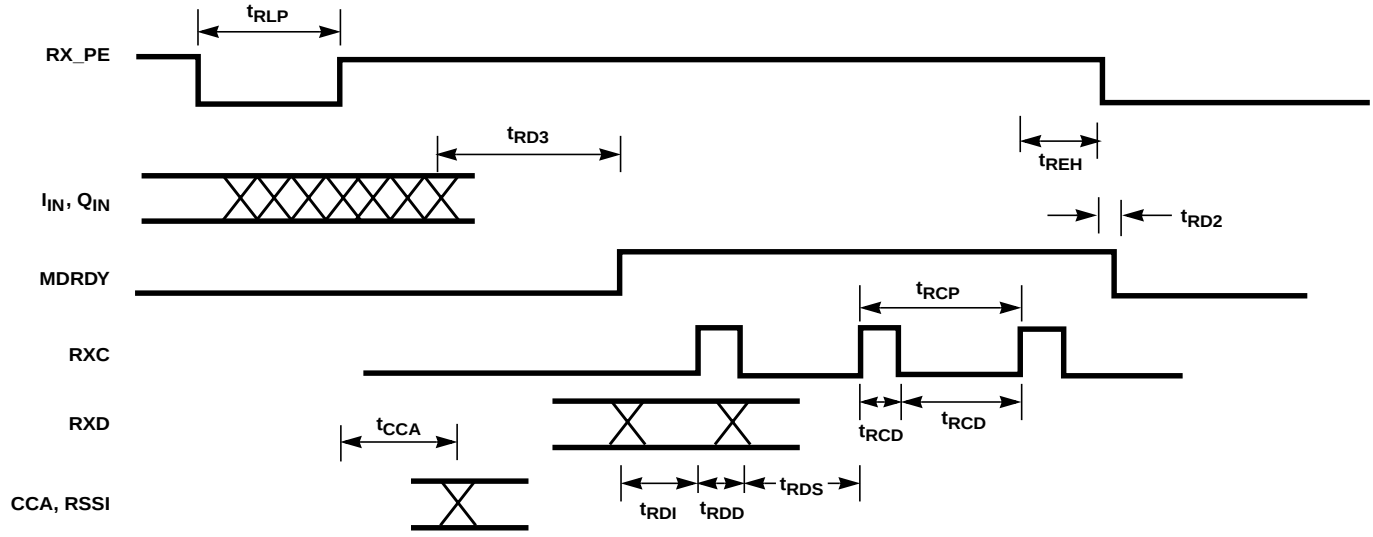



**FIGURE 21. BBP RECEIVE PORT SIGNAL TIMING**

NOTE: RXD, MDRDY is output two MCLK after RXC rising to provide hold time. RSSI output on TEST (5:0).

**TABLE 2. BBP RECEIVE PORT AC ELECTRICAL SPECIFICATIONS**

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| RX_PE Inactive Width | $t_{RLP}$ | 70 | - | ns (Note 13) |
| RXC Period (11MBps Mode) | $t_{RCP}$ | 77 | - | ns |
| RXC Width Hi or Low (11MBps Mode) | $t_{RCD}$ | 31 | - | ns |
| RXC to RXD | $t_{RDD}$ | 20 | 60 | ns |
| MD_RDY to 1st RXC | $t_{RD1}$ | 940 | - | ns (Note 14) |
| RXD to 1st RXC | $t_{RD!}$ | 940 | - | ns |
| Setup RXD to RXC | $t_{RDS}$ | 31 | - | ns |
| RXC to RX_PE Inactive (1MBps) | $t_{REH}$ | 0 | 925 | ns (Note 15) |
| RXC to RX_PE Inactive (2MBps) | $t_{REH}$ | 0 | 380 | ns (Note 15) |
| RXC to RX_PE Inactive (5.5MBps) | $t_{REH}$ | 0 | 140 | ns (Note 15) |
| RXC to RX_PE Inactive (11MBps) | $t_{REH}$ | 0 | 50 | ns (Note 15) |
| RX_PE inactive to MD_RDY Inactive | $t_{RD2}$ | 5 | 30 | ns (Note 16) |
| Last Chip of SFD in to MD_RDY Active | $t_{RD3}$ | 2.77 | 2.86 | µs (Note 14) |
| RX Delay | | 2.77 | 2.86 | µs (Note 17) |
| RX_PE to CCA Valid | $t_{CCA}$ | - | 10 | µs (Note 18) |
| RX_PE to RSSI Valid | $t_{CCA}$ | - | 10 | µs (Note 18) |

NOTES:

13. RX_PE must be inactive at least 3 MCLKs before going active to start a new CCA or acquisition.
14. MD_RDY programmed to go active after SFD detect (measured from $I_{IN}$, $Q_{IN}$).
15. RX_PE active to inactive delay to prevent next RXC.
16. Assumes RX_PE inactive after last RXC.
17. MD_RDY programmed to go active at MPDU start. Measured from first chip of first MPDU symbol at $I_{IN}$, $Q_{IN}$ to MD_RDY active.
18. CCA and RSSI are measured once during the first 10µs interval following RX_PE going active. RX_PE must be pulsed to initiate a new measurement. RSSI may be read via serial port or from Test Bus.

### BBP Packet Transmission

There are 4 signals associated with the BBP Transmit Port: TX_PE (transmit enable), TXRDY (transmit ready), TXD (transmit data), and TXCLK (transmit clock). These connect to the HFA3841 on PL0, PL7, TXD, and TXC, respectively.

State machines within the BBP control packet transmission and reception. In the case of a transmission, the MAC signals the BBP with the signal TX_PE. The BBP forms the preamble and header and then signals the MAC to begin transferring data with the signal TXRDY. This sequence is illustrated in Figure 22 with detailed signal timing shown in Figure 23 and specified delays contained in Table 3. Note that if the MAC deactivates TX_PE too early it may cut off modulation of the final symbol. For this reason, when TX_PE is de-asserted the BBP will hold TXRDY active until the last symbol containing data is modulated. This is important for power sequencing and is discussed in more detail in that section.

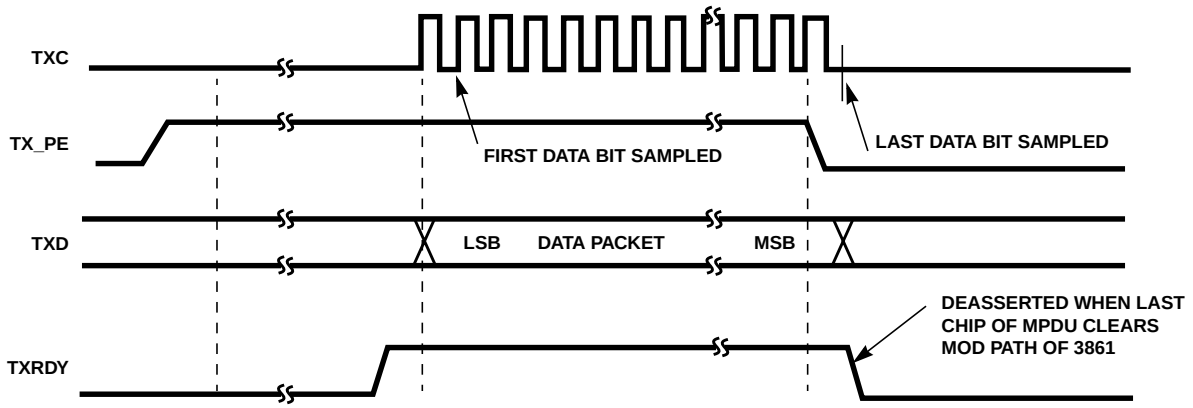
For more detailed information concerning BBP packet transmission see the HFA3861 data sheet.

**TABLE 3. BBP TRANSMIT PORT AC ELECTRICAL SPECIFICATIONS**

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| TX_PE to $I_{OUT}/Q_{OUT}$ (1st Valid Chip) | $t_{D1}$ | 2.18 | 2.3 | µs (Note 19) |
| TX_PE Inactive Width | $t_{TLP}$ | 2.22 | - | µs (Note 20) |
| TXC Width Hi or Low | $t_{TCD}$ | 40 | - | ns |
| TXRDY Active to 1st TX_CLK Hi | $t_{RC}$ | 260 | - | ns |
| Setup TXD to TXC Hi | $t_{TDS}$ | 30 | - | ns |
| Hold TXD to TXC Hi | $t_{TDH}$ | 0 | - | ns |
| TXC to TX_PE Inactive (1MBps) | $t_{PEH}$ | 0 | 965 | ns (Note 22) |
| TXC to TX_PE Inactive (2MBps) | $t_{PEH}$ | 0 | 420 | ns (Note 22) |
| TXC to TX_PE Inactive (5.5MBps) | $t_{PEH}$ | 0 | 160 | ns (Note 22) |
| TXC to TX_PE Inactive (11MBps) | $t_{PEH}$ | 0 | 65 | ns (Note 22) |
| TXRDY Inactive To Last Chip of MPDU Out | $t_{RI}$ | -20 | 20 | ns |
| TXD Modulation Extension | $t_{ME}$ | 2 | - | µs (Note 21) |

NOTES:

19. $I_{OUT}/Q_{OUT}$ are modulated before first valid chip of preamble is output to provide ramp up time for RF/IF circuits.
20. TX_PE must be inactive before going active to generate a new packet.
21. $I_{OUT}/Q_{OUT}$ are modulated after last chip of valid data to provide ramp down time for RF/IF circuits.
22. Delay from TXC to inactive edge of TXPE to prevent next TXC. Because TXPE asynchronously stops TXC, TXPE going inactive within 40ns of TXC will cause TXC minimum hi time to be less than 40ns.




NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge of TXC.

**FIGURE 22. BBP TRANSMIT PORT TIMING**

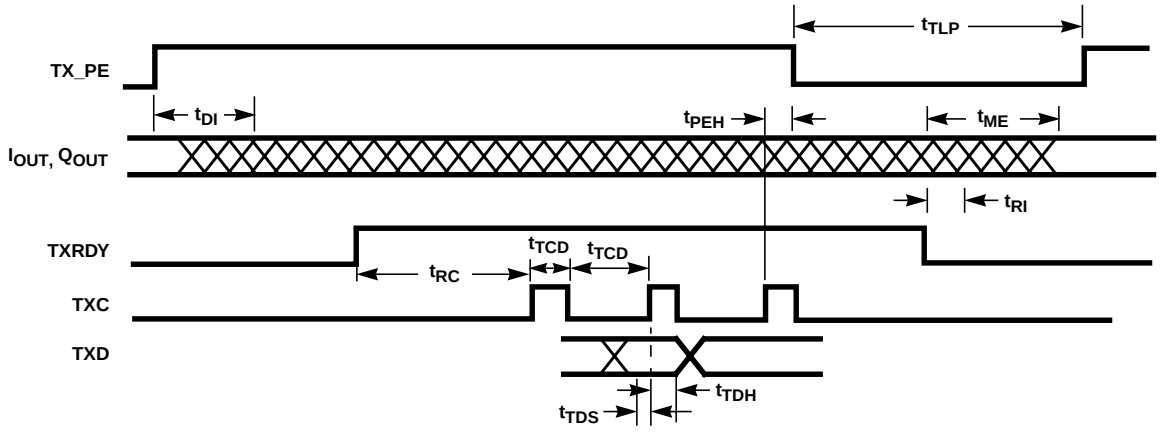



**FIGURE 23. BBP TRANSMIT PORT SIGNAL TIMING**

### *Power Sequencing*

The HFA3841 provides a number of firmware controlled port pins that are used for controlling the power sequencing and other functions in the front end components of the PHY.

Packet transmission requires precise control of the radio. Ideally, energy at the antenna ceases after the last symbol of information has been transmitted. Additionally, the transmit/receive switch must be controlled properly to protect the receiver. It's also important to apply appropriate modulation to the PA while it's active.

Signaling sequences for the beginning and end of normal transmissions are illustrated in Figure 24. Table 4 lists applicable delays.

A transmission begins with PE2 as shown in Figure 24. Next, the transmit/receive switch is configured for transmission via the differential pair TR_SW and TR_SW_BAR. This is followed by TX_PE which activates the transmit state machine in the BBP. Lastly, PA_PE activates the PA. Delays for these signals related to the initiation of transmission are referenced to PE2.

Immediately after the final data bit has been clocked out of the HFA3841, TX_PE is de-asserted. The HFA3841 then waits for TXRDY to go inactive, signaling that the BBP has modulated the final information-rich symbol. It then immediately de-asserts PA_PE followed by placing the transmit/receive switch in the receive position and ending with PE2 going high. Delays for these signals related to the termination of transmission are referenced to the rising edge of PE2.

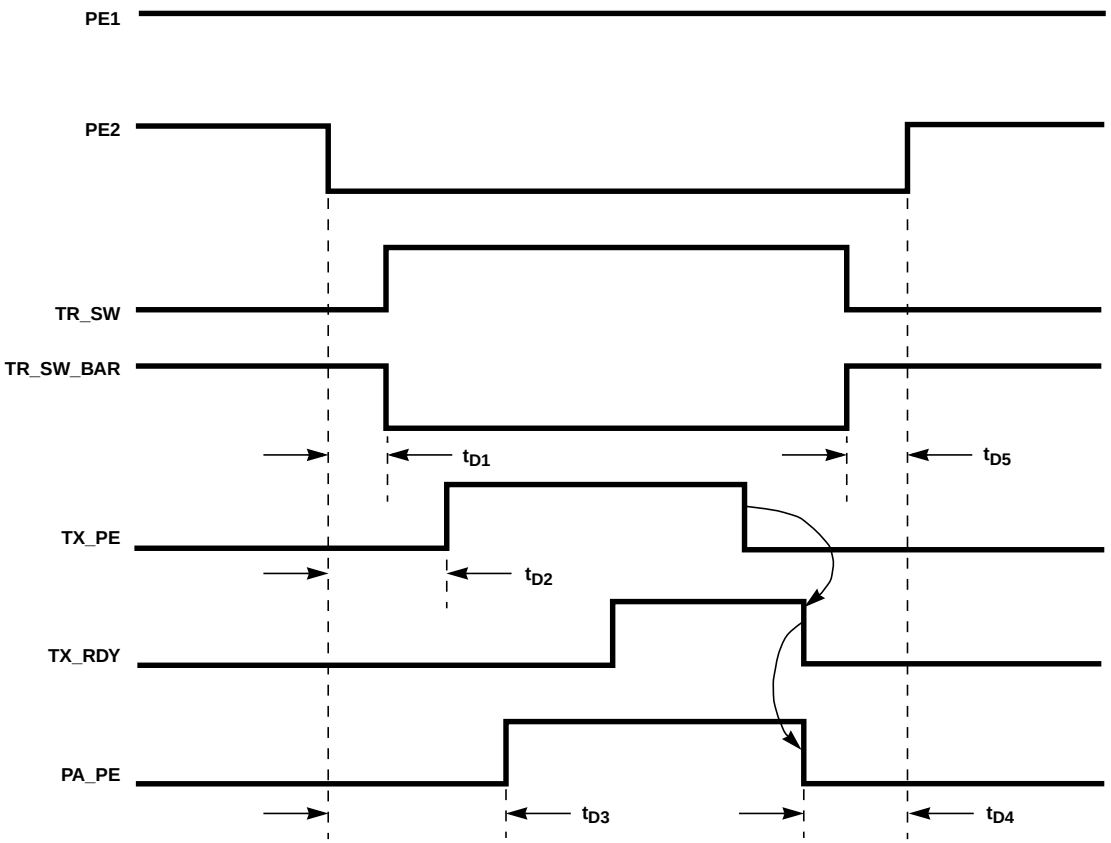



FIGURE 24. TRANSMIT CONTROL SIGNAL SEQUENCING

TABLE 4. TRANSMIT CONTROL TIMING SPECIFICATIONS

| PARAMETER | SYMBOL | DELAY | TOLERANCE | UNITS |
|---|---|---|---|---|
| PE2 to TR Switch | $t_{D1}$ | 2 | ±0.1 | µs |
| PE2 to BBP TX_PE | $t_{D2}$ | TBD | ±0.1 | µs |
| PE2 to PA_PE | $t_{D3}$ | 3 | ±0.1 | µs |
| PA_PE to PE2 | $t_{D4}$ | 3 | ±0.1 | µs |
| TR Switch to PE2 | $t_{D5}$ | 2 | ±0.1 | µs |

PE1 and PE2 encoding details are found in Table 5.

Note that during normal receive and transmit operation that PE1 is static and PE2 toggles for receive and transmit states.

TABLE 5. POWER ENABLE STATES

| | PE1 | PE2 | PLL_PE |
|---|---|---|---|
| Power Down State | 0 | 0 | 1 |
| Receive State | 1 | 1 | 1 |
| Transmit State | 1 | 0 | 1 |
| PLL Active State | 0 | 1 | 1 |
| PLL Disable State | X | X | 0 |

NOTE: PLL_PE is controlled via the serial interface, and can be used to disable the internal synthesizer, the actual synthesizer control is an AND function of PLL_PE, and a result of the OR function of PE1 and PE2. PE1 and PE2 will directly control the power enable functionality of the LO buffer(s)/phase shifter.

## Master Clock

### Prescaler

The HFA3841 contains a clock prescaler to provide flexibility in the choice of clock input frequencies. For 11Mb/s operation, the internal master clock, MCLK, must be between 11MHz and 16MHz. The clock generator itself requires an input from the prescaler that is twice the desired MCLK frequency. Thus the lowest oscillator frequency that can be used for an 11MHz MCLK is 22MHz. The prescaler can divide by integers and 1/2 steps (IE 1, 1.5, 2, 2.5). Another way to look at it is that the divisor ratio between the external clock source and the internal MCLK may be integers between 2 and 14.

Typically, the 44MHz baseband clock is used as the input, and the prescaler is set to divide by 2. Another useful configuration is to set the prescaler to divide by 1.5 (resulting in 44MHz ÷3) for an MCLK of 14.67MHz.

### Off Chip

If an off chip oscillator source is used, it should be connected to the XTALI pin. Insure that the signal amplitude meets CMOS levels at the XTALI pin.

### Oscillator

The XTALI and XTALO pins provide an on-chip oscillator function to generate the master clock. For a standard pierce oscillator, the crystal is connected between XTALI and XTALO. Two capacitors, typically 15pF each, are connected from each pin to ground. The crystal should be a fundamental mode, specified under parallel resonance conditions. The load capacitance seen by the crystal will be approximately 2pF more than the series combination of $C_1$ and $C_2$ plus stray capacitance. After power on, the crystal will require time to stabilize before normal operation can commence. Insure that reset remains asserted for enough time for the crystal oscillator to stabilize.

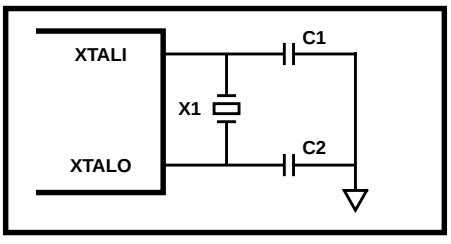



**FIGURE 25. POWER ON RESET CONFIGURATION**

## Power On Reset Configuration

Power On Reset is issued to the HFA3841 with the HRESET pin or via the soft reset bit, SRESET, in the Configuration Option Register (COR, bit 7). HRESET originates from the HOST system which applies HRESET for at least 0.01ms after $V_{CC}$ has reached 90% of its end value (see PC-Card standard, Vol. 2, Ch. 4.12.1).

The MD[15:8] pin values are sampled on the falling edge of HRESET or SRESET. These pins have internal 50K pull-down resistors. External pull-up resistors (typically 10kΩ) are used for bits that should be read as high at reset.

The table below summarizes the effect per pin.

**TABLE 6. POR PINS AND FUNCTIONALITY**

| PIN | LATCH OUTPUT | FUNCTIONALITY |
|---|---|---|
| MD[8] | Reserved | |
| MD[9] | Nvdis | Disable mapping of CS to NV (Flash) |
| MD[10] | MEM16 | External memory (RAM and Flash) is 16 bits wide |
| MD[11] | IDLE | See below |
| MD[12] | Reserved | |
| MD[15:13] | MD15/14/13 | FW purposes |

MD[11], IDLE, has no equivalent functionality in any control register. When asserted at reset, it will inhibit firmware execution. This is used to allow the initial download of firmware in “Genesis Mode”. See the Hardware Reference Manual for more details. The latch is cleared when the Software Reset, SRESET, COR(7) is active.

## References

For Intersil documents available on the internet, see web site http://www.intersil.com/
Intersil AnswerFAX (321) 724-7800.

[1] IEEE Std 802.11-1999 Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification.

[2] *HFA3860B Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4594.

[3] *HFA3861 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4699.

[4] *HFA3783 Data Sheet*, Quad IF, Intersil Corporation, AnswerFAX Doc. No. 4633.

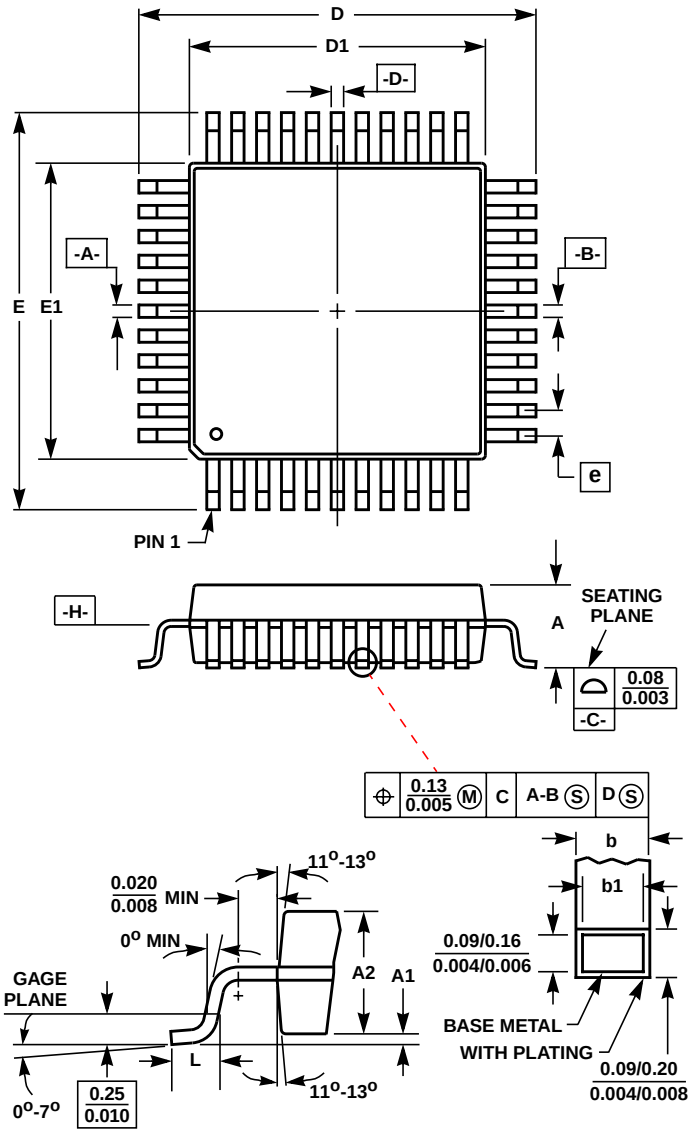
[5] *HFA3683 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4634.

[6] PC Card Standard 1996, PCMCIA/JEIDA.

[7] A*N9874 Application Note*, Intersil Corporation, “ISA Plug and Play with the HFA3841”.

[8] A*N9844 Application Note*, Intersil Corporation, “HFA3841 to PRISMII Connections”, AnswerFAX Doc. No. 99844

## Thin Plastic Quad Flatpack Packages (LQFP)




**Q128.14x20 (JEDEC MS-026BHB ISSUE C)**
**128 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.062 | - | 1.60 | - |
| A1 | 0.002 | 0.005 | 0.05 | 0.15 | - |
| A2 | 0.054 | 0.057 | 1.35 | 1.45 | - |
| b | 0.007 | 0.010 | 0.17 | 0.27 | 6 |
| b1 | 0.007 | 0.009 | 0.17 | 0.23 | - |
| D | 0.862 | 0.870 | 21.90 | 22.10 | 3 |
| D1 | 0.783 | 0.791 | 19.90 | 20.10 | 4, 5 |
| E | 0.626 | 0.634 | 15.90 | 16.10 | 3 |
| E1 | 0.547 | 0.555 | 13.90 | 14.10 | 4, 5 |
| L | 0.018 | 0.029 | 0.45 | 0.75 | - |
| N | 128 | | 128 | | 7 |
| e | 0.0197 BSC | | 0.50 BSC | | - |

Rev. 0 7/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.



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