

20A, 30V, 0.052 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76107.

Ordering Information

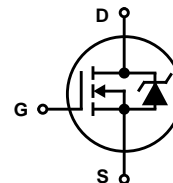
PART NUMBER	PACKAGE	BRAND
HUF76107D3	TO-251AA	76107D
HUF76107D3S	TO-252AA	76107D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HUF76107D3ST.

Features

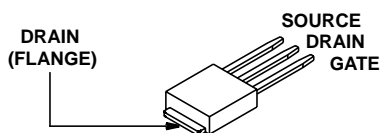
- Logic Level Gate Drive
- 20A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.052\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER® Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

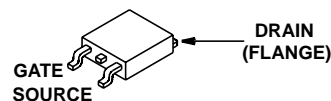


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



HUF76107D3, HUF76107D3S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	20 A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5\text{V}$)	I_D	10.5 A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2)	I_D	10 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figure 6
Power Dissipation	P_D	35 W
Derate Above 25°C		0.30 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 20\text{A}$, $V_{GS} = 10\text{V}$ (Figure 9, 10)	-	0.042	0.052	Ω
		$I_D = 10.5\text{A}$, $V_{GS} = 5\text{V}$ (Figure 9)	-	0.058	0.080	Ω
		$I_D = 10\text{A}$, $V_{GS} = 4.5\text{V}$ (Figure 9)	-	0.065	0.085	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	3.3	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251, TO-252	-	-	100	$^\circ\text{C}/\text{W}$
SWITCHING SPECIFICATIONS ($V_{GS} = 4.5\text{V}$)						
Turn-On Time	t_{ON}	$V_{DD} = 15\text{V}$, $I_D \cong 10\text{A}$, $R_L = 1.50\Omega$, $V_{GS} = 4.5\text{V}$, $R_{GS} = 33\Omega$ (Figure 15)	-	-	120	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	t_r		-	66	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	16	-	ns
Fall Time	t_f		-	22	-	ns
Turn-Off Time	t_{OFF}		-	-	57	ns

HUF76107D3, HUF76107D3S

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 15\text{V}$, $I_D \cong 20\text{A}$, $R_L = 0.75\Omega$, $V_{GS} = 10\text{V}$, $R_{GS} = 33\Omega$ (Figures 16)	-	-	75	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	18	-	ns	
Rise Time	t_r		-	30	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	62	-	ns	
Fall Time	t_f		-	20	-	ns	
Turn-Off Time	t_{OFF}		-	-	125	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 15\text{V}$, $I_D \cong 10.5\text{A}$, $R_L = 1.43\Omega$ $I_{g(REF)} = 1.0\text{mA}$ (Figure 14)	-	8.6	10.3	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V to } 5\text{V}$		-	4.7	5.7	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } 1\text{V}$		-	0.35	0.42	nC
Gate to Source Gate Charge	Q_{gs}			-	1.00	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	2.40	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13)	-	315	-	pF	
Output Capacitance	C_{OSS}		-	170	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 10.5\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 10.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	39	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 10.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	49	nC

Typical Performance Curves Unless otherwise specified

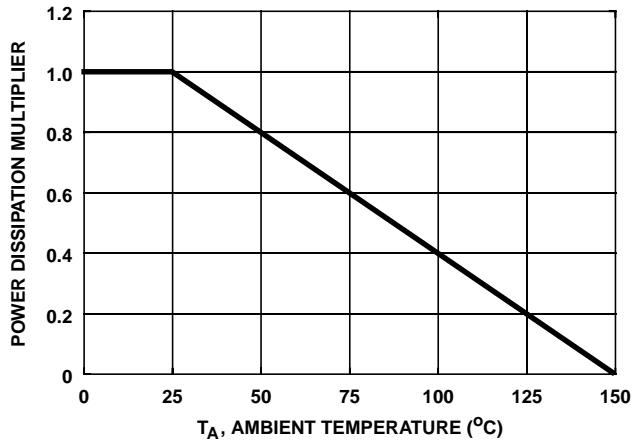


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

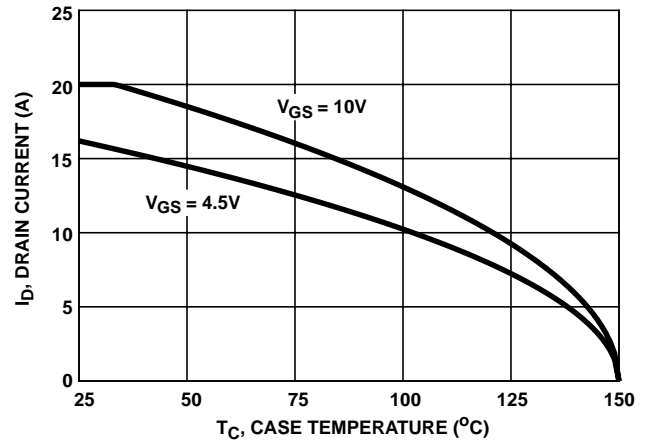


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless otherwise specified (Continued)

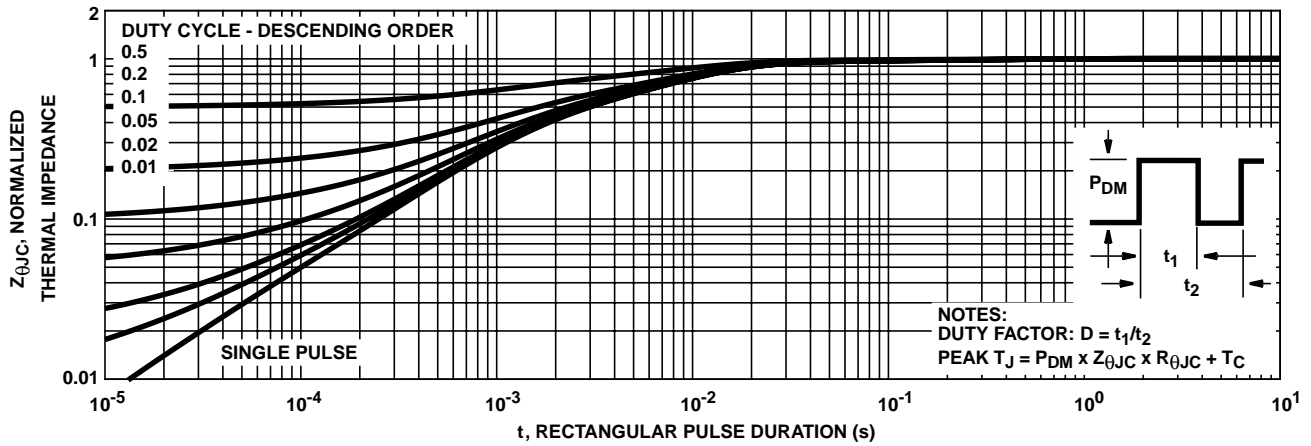


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

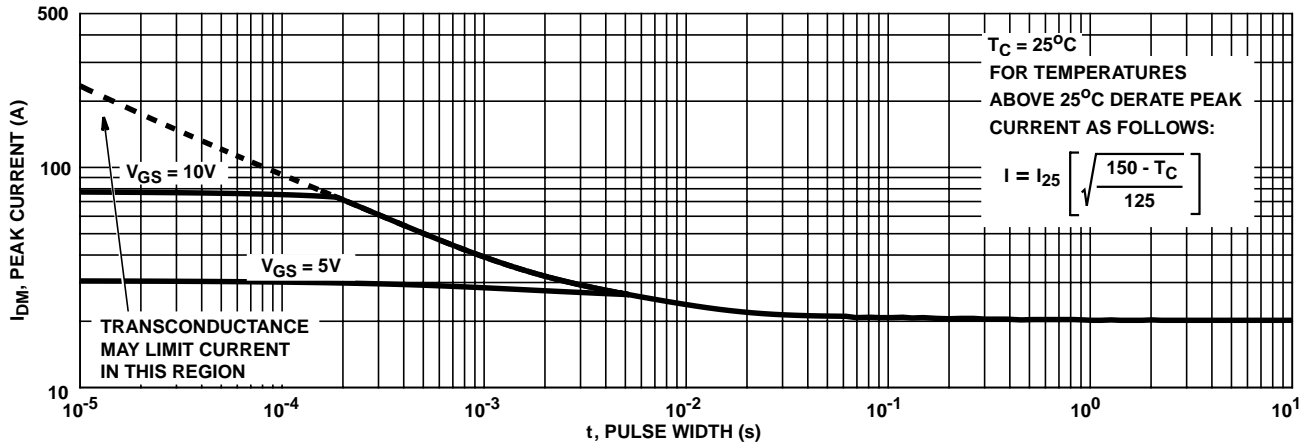


FIGURE 4. PEAK CURRENT CAPABILITY

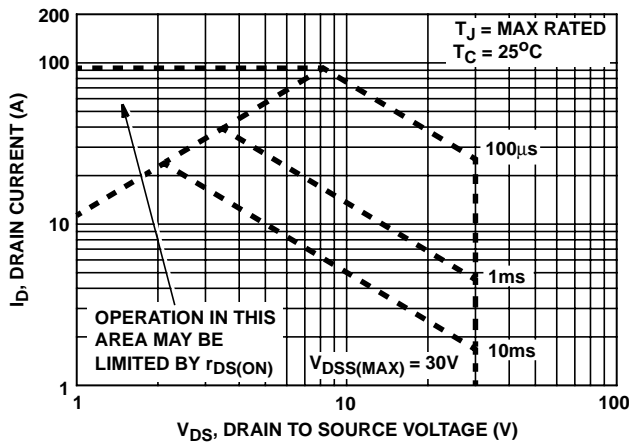
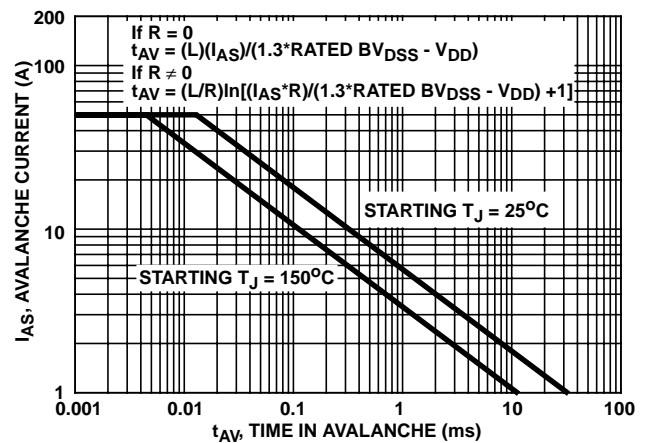


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves Unless otherwise specified (Continued)

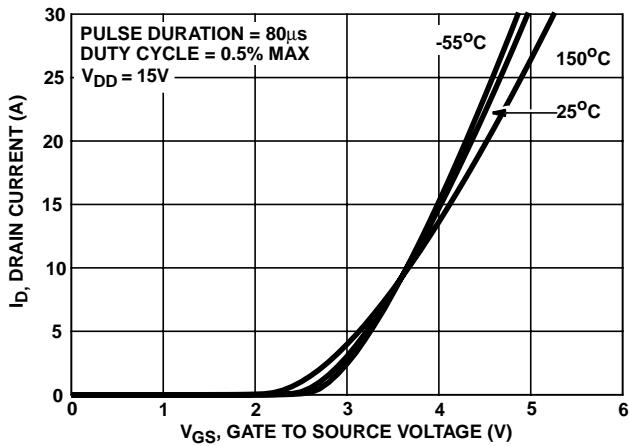


FIGURE 7. TRANSFER CHARACTERISTICS

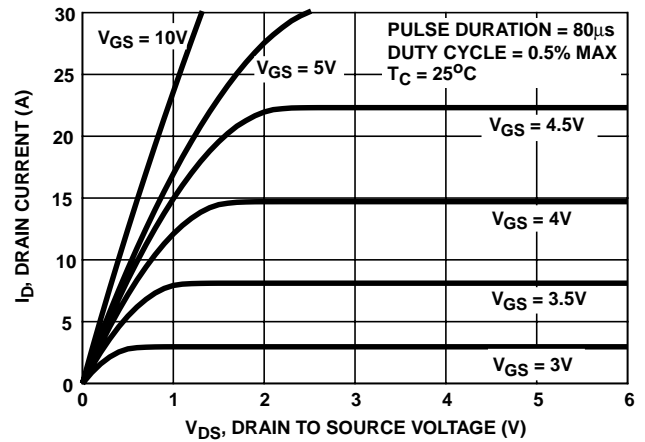


FIGURE 8. SATURATION CHARACTERISTICS

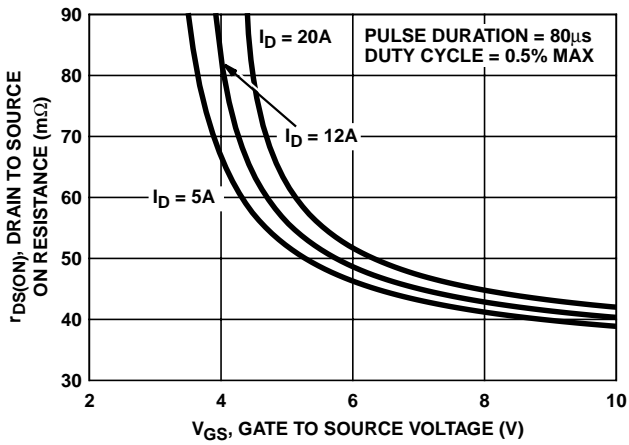


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

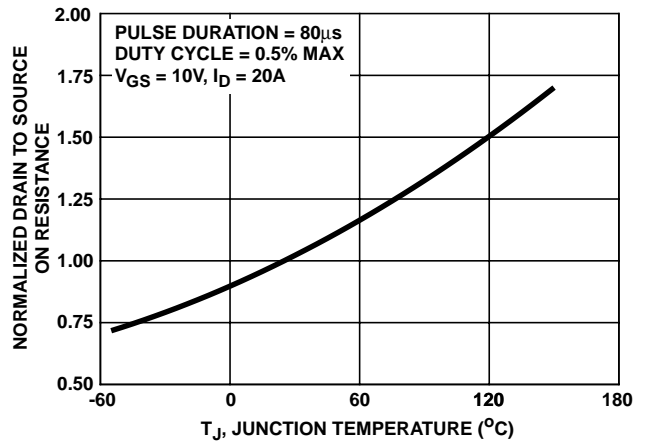


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

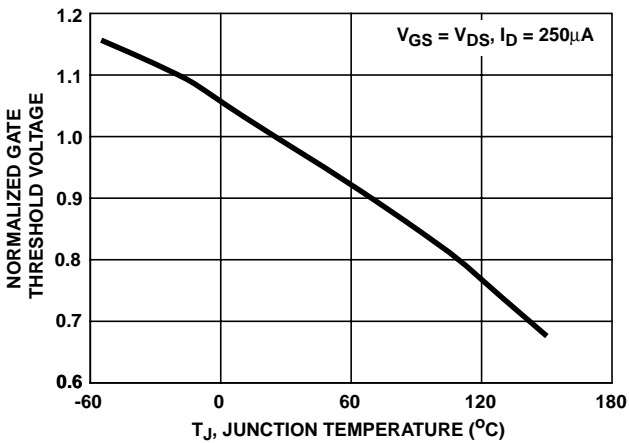


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

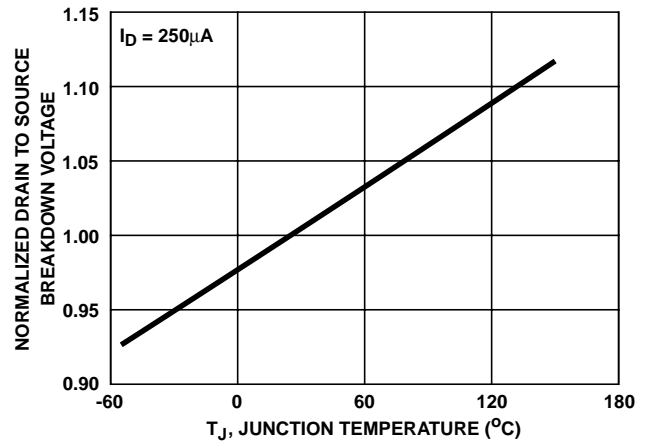


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless otherwise specified (Continued)

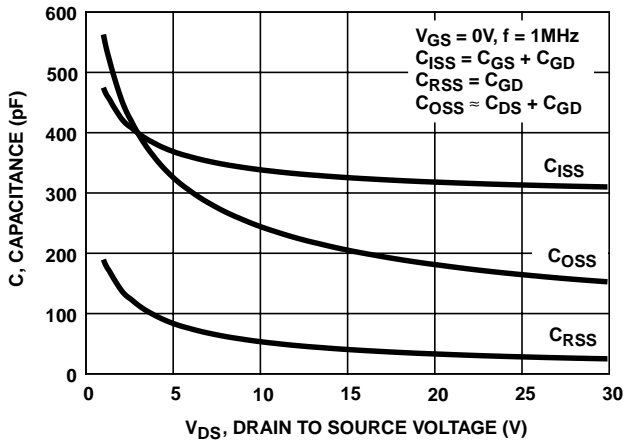
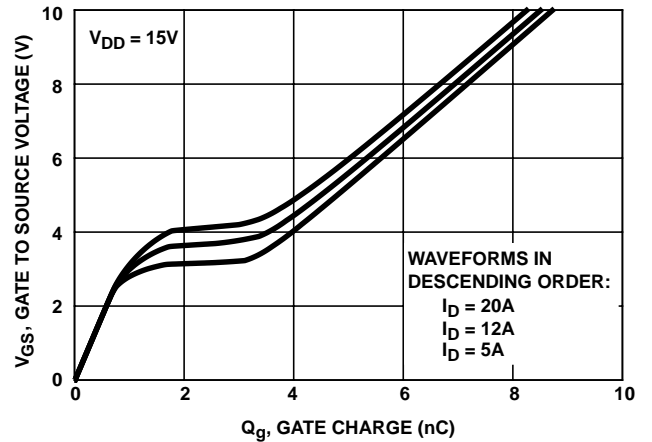


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

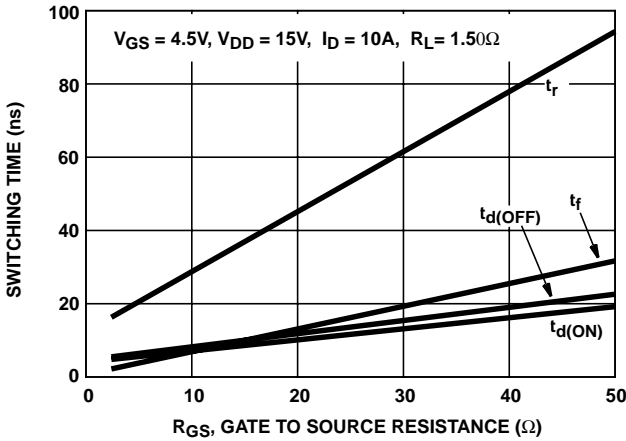


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

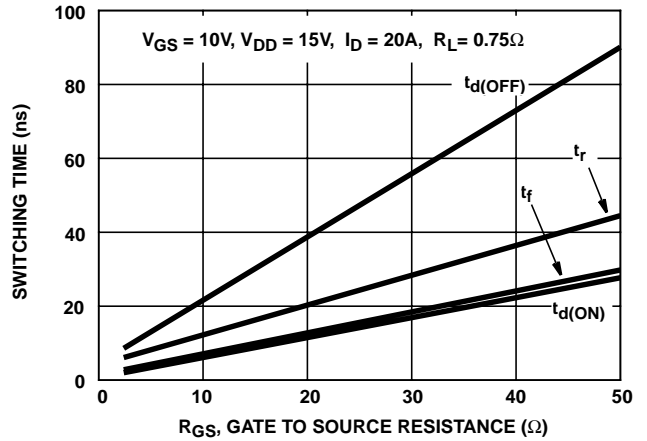


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

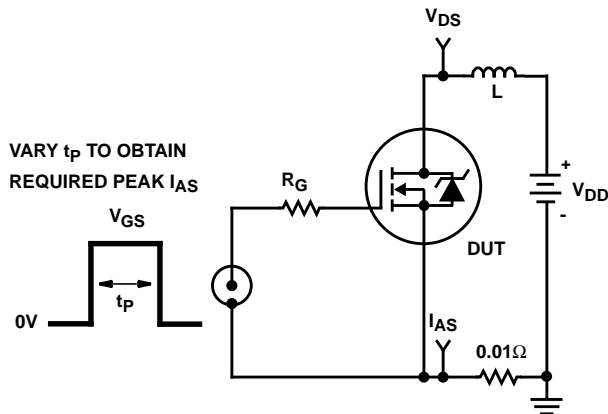


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

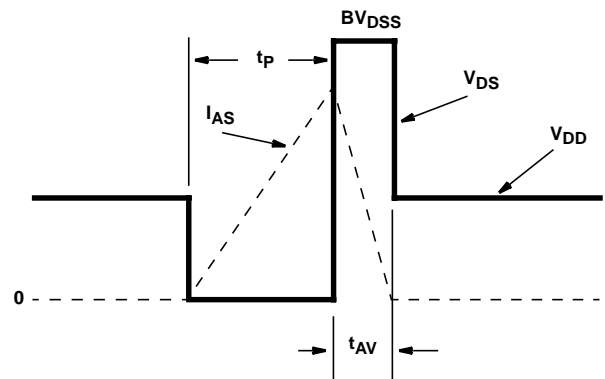


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

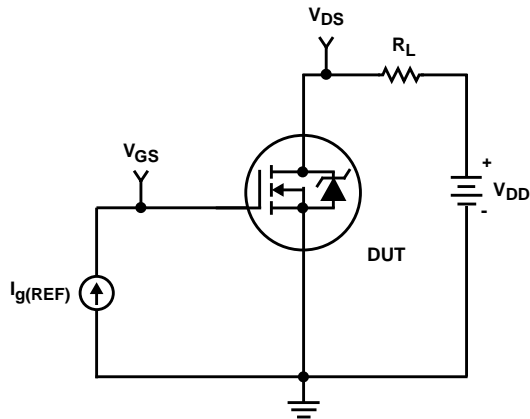


FIGURE 19. GATE CHARGE TEST CIRCUIT

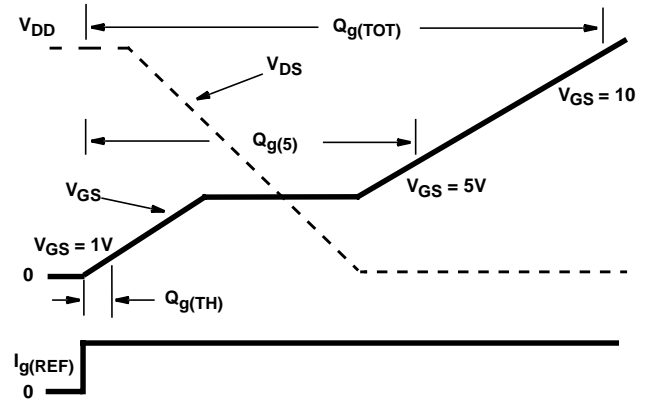


FIGURE 20. GATE CHARGE WAVEFORMS

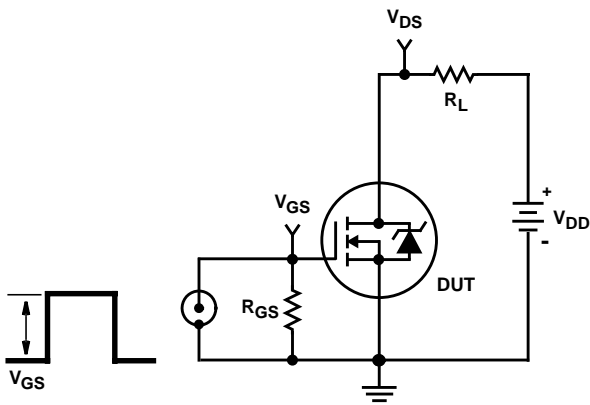


FIGURE 21. SWITCHING TIME TEST CIRCUIT

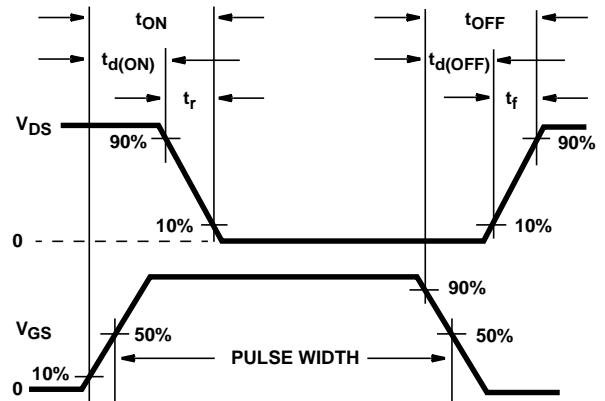


FIGURE 22. SWITCHING TIME WAVEFORMS

PSPICE Electrical Model

SUBCKT HUF76107 2 1 3 ; REV June 1998

CA 12 8 4.2e-10
 CB 15 14 4.9e-10
 CIN 6 8 2.85e-10

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.7
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 3.61e-9
 LSOURCE 3 7 3.61e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 3.7e-3
 RGATE 9 20 3.39
 RLDRAIN 2 5 10
 RLGATE 1 9 36.1
 RLSOURCE 3 7 36.1
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 30e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

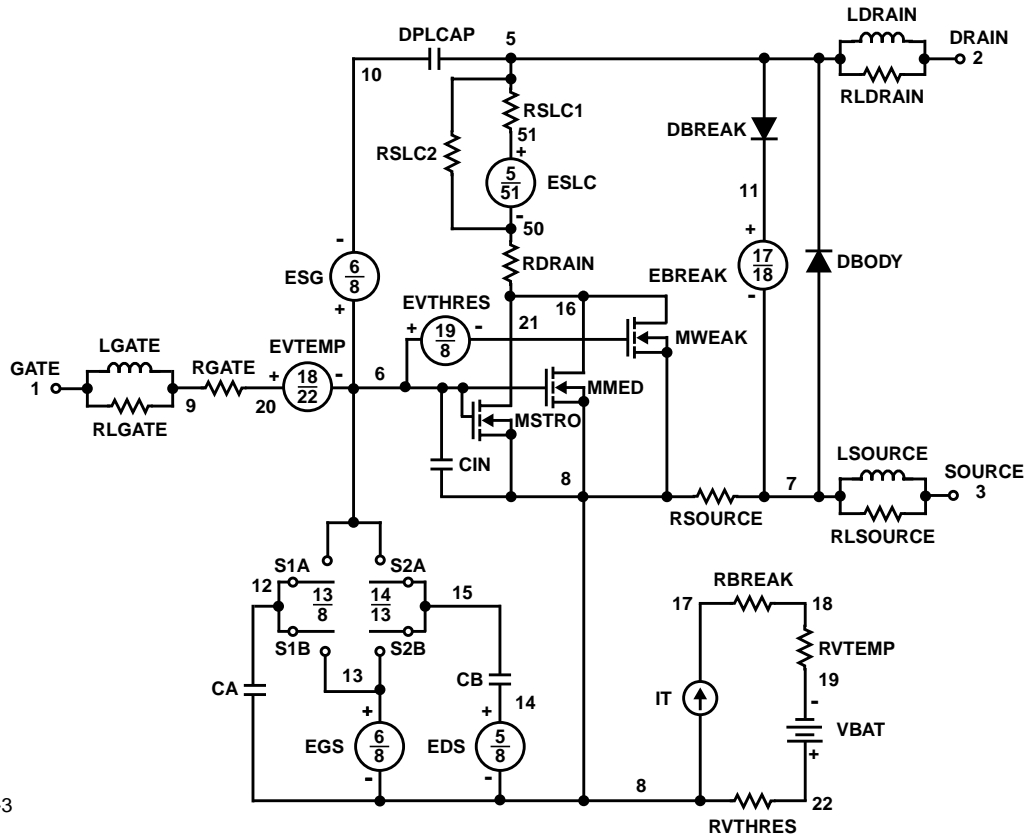
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*50),7))}

.MODEL DBODYMOD D (IS = 2.8e-13 IKF = 5 RS = 1.37e-2 TRS1 = 2e-4 TRS2 = 2e-6 CJO = 4.9e-10 TT = 2.88e-8 M = 3.9e-1 XTI = 4.75)
 .MODEL DBREAKMOD D (RS = 2.5e-1 TRS1 = 9.94e-4 TRS2 = 9.12e-7)
 .MODEL DPLCAPMOD D (CJO = 3.2e-10 IS = 1e-30 N = 10 M = 7.4e-1)
 .MODEL MMEDMOD NMOS (VTO = 2.07 KP = 1.25 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.39)
 .MODEL MSTROMOD NMOS (VTO = 1.8 KP = 1e-1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 1.8 KP = 1e-1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33.9 RS = 1)
 .MODEL RBREAKMOD RES (TC1 = 9.94e-4 TC2 = 9.84e-8)
 .MODEL RDRAINMOD RES (TC1 = 3.9e-2 TC2 = 5.5e-5)
 .MODEL RSLCMOD RES (TC1 = 1e-4 TC2 = 3.2e-6)
 .MODEL RSOURCEMOD RES (TC1 = 1e-12 TC2 = 6e-6)
 .MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -5.96e-6)
 .MODEL RVTEMPMOD RES (TC1 = -1.4e-3 TC2 = 1e-10)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.2 VOFF = -0.5)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = -4.2)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF = 0.0)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.0 VOFF = -0.8)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

nom temp=25 deg c 30v LL Ultrafet

REV Junel 1998

template huf76107 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is=2.8e-13,xti=4.75,cjo=4.9e-10,t=2.88e-8,m=3.9e-1)
d..model dbreakmod = ()
d..model dplcapmod = (cjo=3.2e-10,is=1e-30,n=10,m=7.4e-1)
m..model mmedmod = (type=_n,vto=2.07,kp=1.25,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2.4,kp=19.5,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.8,kp=1e-1,is=1e-30,tox=1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4.2,voff=-0.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-4.2)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.8,voff=0.0)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.0,voff=-0.8)
```

```
c.ca n12 n8 = 4.2e-10
c.cb n15 n14 = 4.9e-10
c.cin n6 n8 = 2.85e-10
```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod
```

```
i.it n8 n17 = 1
```

```
l.l drain n2 n5 = 1e-9
l.l gate n1 n9 = 3.61e-9
l.l source n3 n7 = 3.61e-9
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod,l=1u,w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod,l=1u,w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod,l=1u,w=1u
```

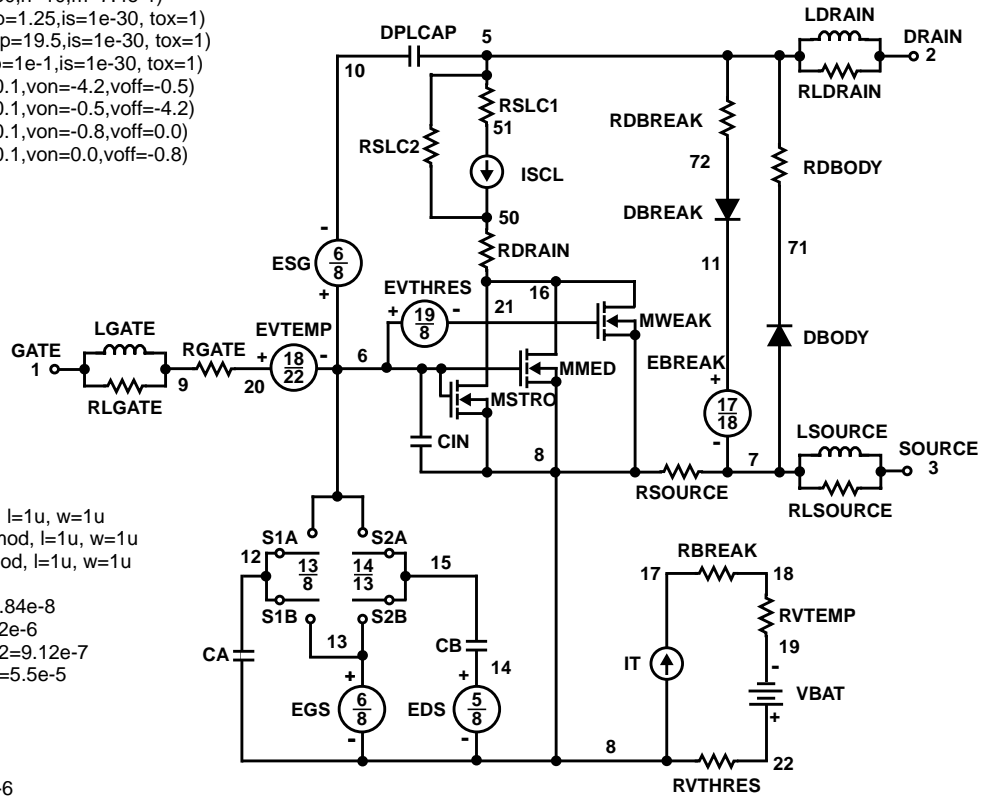
```
res.rbreak n17 n18 = 1,tc1=9.94e-4,tc2=-9.84e-8
res.rbody n71 n5 = 1.37e-2,tc1=2e-4,tc2=2e-6
res.rdbreak n72 n5 = 2.5e-1,tc1=9.94e-4,tc2=9.12e-7
res.rdrain n50 n16 = 3.7e-3,tc1=3.9e-2,tc2=5.5e-5
res.rgate n9 n20 = 3.39
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 36.1
res.rlsource n3 n7 = 36.1
res.rslc1 n5 n51 = 1e-6,tc1=1e-4,tc2=3.2e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 30e-3,tc1=1e-12,tc2=6e-6
res.rvtemp n18 n19 = 1,tc1=-1.4e-3,tc2=1e-10
res.rvthres n22 n8 = 1,tc1=-1.9e-3,tc2=-5.96e-6
```

```
spe.ebreak n11 n7 n17 n18 = 35.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/50)**7)
}
}
```



SPICE Thermal Model

REV June1998

HUF76107

CTHERM1 th 6 5.0e-5
 CTHERM2 6 5 9.0e-4
 CTHERM3 5 4 1.3e-3
 CTHERM4 4 3 1.3e-3
 CTHERM5 3 2 2.2e-2
 CTHERM6 2 tl 7.9e-3

RTHERM1 th 6 2.0e-4
 RTHERM2 6 5 6.0e-3
 RTHERM3 5 4 3.5e-2
 RTHERM4 4 3 8.5e-1
 RTHERM5 3 2 5.1e-1
 RTHERM6 2 tl 1

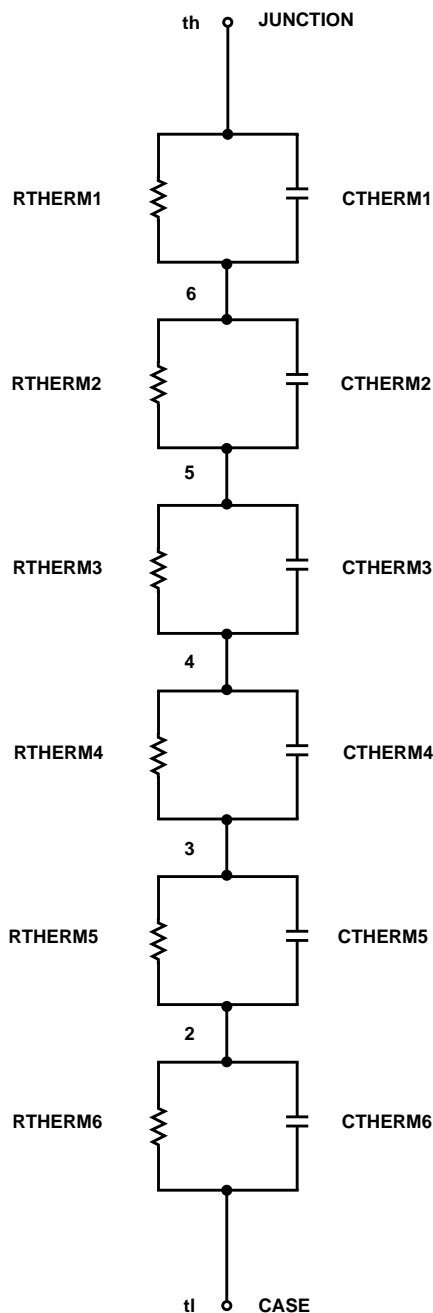
SABER Thermal Model

SABER thermal model HUF76107

template thermal_model th tl
 thermal_c th, tl

```
{
ctherm.ctherm1 th 6 = 5.0e-5
ctherm.ctherm2 6 5 = 9.0e-4
ctherm.ctherm3 5 4 = 1.3e-3
ctherm.ctherm4 4 3 = 1.3e-3
ctherm.ctherm5 3 2 = 2.2e-2
ctherm.ctherm6 2 tl = 7.9e-3
```

```
rtherm.rtherm1 th 6 = 2.0e-4
rtherm.rtherm2 6 5 = 6.0e-3
rtherm.rtherm3 5 4 = 3.5e-2
rtherm.rtherm4 4 3 = 8.5e-1
rtherm.rtherm5 3 2 = 5.1e-1
rtherm.rtherm6 2 tl = 1
}
```



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>