ACS21MS

Data Sheet | July 1999 | File Number 4757

Radiation Hardened Dual 4-Input AND Gate

The Radiation Hardened ACS21MS is a Dual 4-Input AND Gate. For each gate, a HIGH level on all inputs results in a HIGH level on the Y output. A LOW level on any input results in a LOW level on the Y output. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS21MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS21MS are contained in SMD 5962-98629. A “hot-link” is provided on our homepage for downloading.
www.intersil.com/spacedefense/newsafclasst.asp

Features

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25 Micron Radiation Hardened SOS CMOS
- Radiation Environment
  - Latch-Up Free Under Any Conditions
  - Total Dose (Max.) . . . . 3 x 10^5 RAD(Si)
  - SEU Immunity. . . . . <1 x 10^{-10} Errors/Bit/Day
  - SEU LET Threshold . . . . >100MeV/(mg/cm^2)
- Input Logic Levels. . . . $V_{IL} = (0.3)(V_{CC})$, $V_{IH} = (0.7)(V_{CC})$
- Output Current . . . . ±12mA (Min)
- Quiescent Supply Current . . . . 5.0µA (Max)
- Propagation Delay . . . . 15ns (Max)

Applications

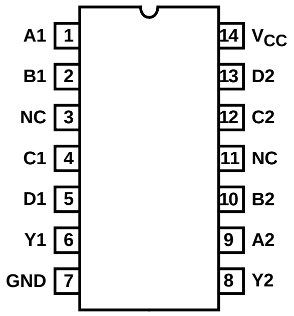
- High Speed Control Circuits
- Sensor Monitoring
- Low Power Designs

Ordering Information

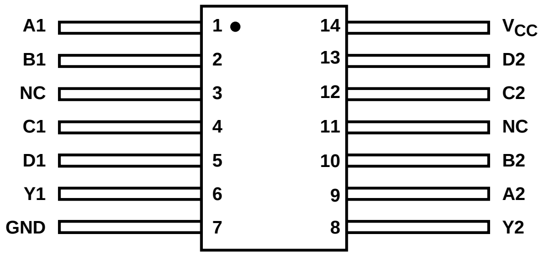
ORDERING NUMBER	INTERNAL MARKETING NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9862901VCC	ACS21DMSR-03	-55 to 125	14 Ld SBDIP	CDIP2-T14
ACS21D/SAMPLE-03	ACS21D/SAMPLE-03	25	14 Ld SBDIP	CDIP2-T14
5962F9862901VXC	ACS21KMSR-03	-55 to 125	14 Ld Flatpack	CDFP3-F14
ACS21K/SAMPLE-03	ACS21K/SAMPLE-03	25	14 Ld Flatpack	CDFP3-F14
5962F9862901V9A	ACS21HMSR-03	25	Die	NA

Pinouts

ACS21MS
(SBDIP)
TOP VIEW



ACS21MS
(FLATPACK)
TOP VIEW



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Die Characteristics

DIE DIMENSIONS:

Size: 2390μm x 2390μm (94 mils x 94 mils)
Thickness: 525μm ±25μm (20.6 mils ±1 mil)
Bond Pad: 110μm x 110μm (4.3 x 4.3 mils)

METALLIZATION: Al

Metal 1 Thickness: 0.7μm ±0.1μm
Metal 2 Thickness: 1.0μm ±0.1μm

SUBSTRATE POTENTIAL

Unbiased Insulator

PASSIVATION:

Type: Phosphorous Silicon Glass (PSG)
Thickness: 1.30μm ±0.15μm

SPECIAL INSTRUCTIONS

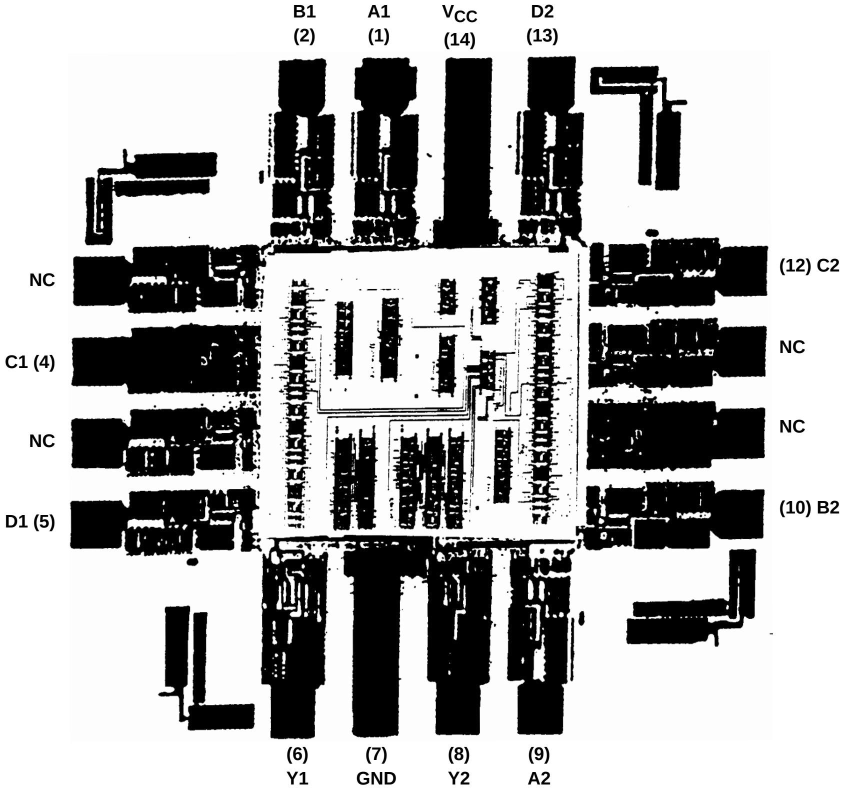
Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Current Density: <2.0 x 10^5 A/cm^2
Transistor Count: 92

Metallization Mask Layout

ACS21MS



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