

# IR2101

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

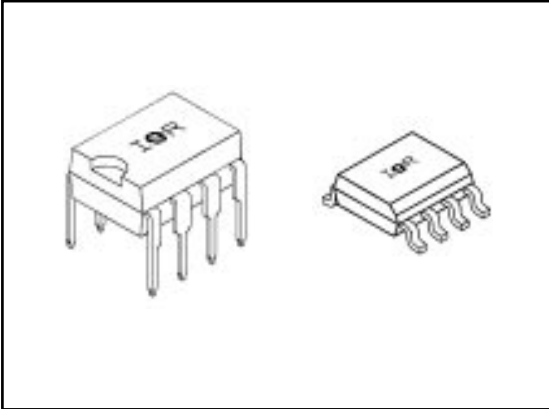
### Product Summary

<b>V<sub>OFFSET</sub></b>	<b>600V max.</b>
<b>I<sub>O+/-</sub></b>	<b>100 mA / 210 mA</b>
<b>V<sub>OUT</sub></b>	<b>10 - 20V</b>
<b>t<sub>on/off</sub> (typ.)</b>	<b>130 &amp; 90 ns</b>
<b>Delay Matching</b>	<b>30 ns</b>

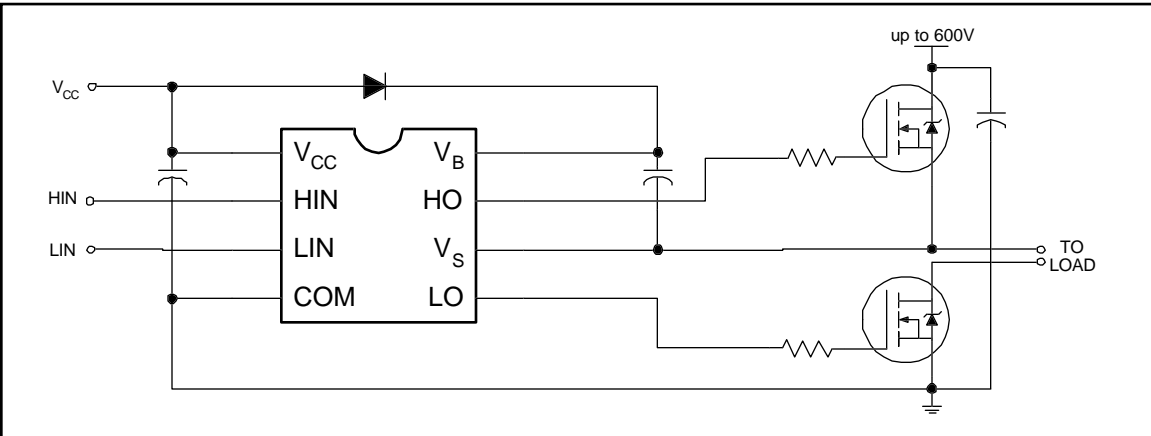
### Description

The IR2101 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

### Packages



### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Voltage	-0.3	625	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V <sub>LO</sub>	Low Side Output Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic Input Voltage (HIN & LIN)	-0.3	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>A</sub> ≤ +25°C (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction Temperature	—	150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	Note 1	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low Side and Logic Fixed Supply Voltage	10	20	
V <sub>LO</sub>	Low Side Output Voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic Input Voltage (HIN & LIN)	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$ ,  $C_L = 1000 \text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

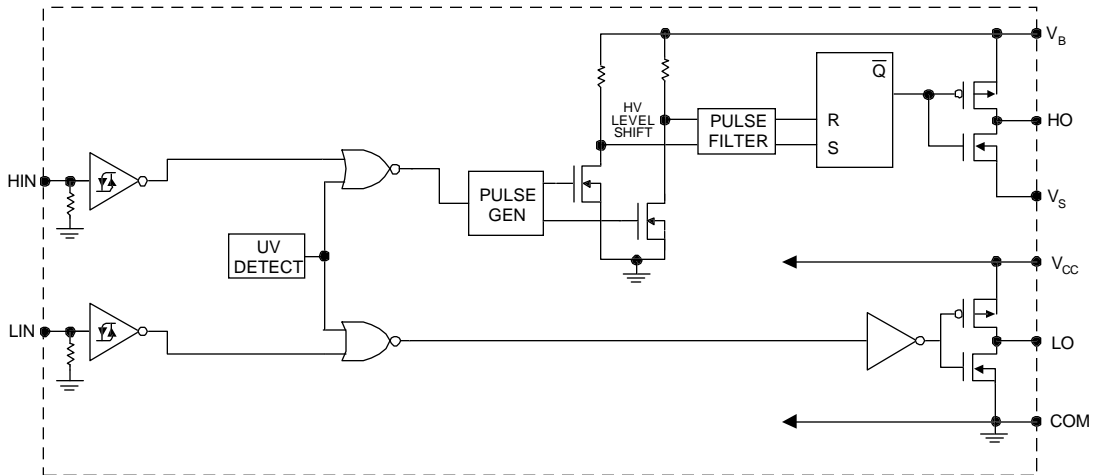
Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{on}$	Turn-On Propagation Delay	—	130	200	ns	$V_S = 0V$
$t_{off}$	Turn-Off Propagation Delay	—	90	200		$V_S = 600V$
$t_r$	Turn-On Rise Time	—	80	120		
$t_f$	Turn-Off Fall Time	—	40	70		
MT	Delay Matching, HS & LS Turn-On/Off	—	30	—		

## Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$V_{IH}$	Logic "1" Input Voltage	2.7	—	—	V	$V_{CC} = 10V$ to $20V$
$V_{IL}$	Logic "0" Input Voltage	—	—	0.8		$V_{CC} = 10V$ to $20V$
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	20	50		$V_{IN} = 0V$ or $5V$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	140	240		$V_{IN} = 0V$ or $5V$
$I_{IN+}$	Logic "1" Input Bias Current	—	20	40		$V_{IN} = 5V$
$I_{IN-}$	Logic "0" Input Bias Current	—	—	1.0		$V_{IN} = 0V$
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	8.8	9.3	9.8	V	
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	7.5	8.2	8.6		
$I_{O+}$	Output High Short Circuit Pulsed Current	100	125	—	mA	$V_O = 0V, V_{IN} = 5V$ $PW \leq 10 \mu s$
$I_{O-}$	Output Low Short Circuit Pulsed Current	210	250	—		$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$

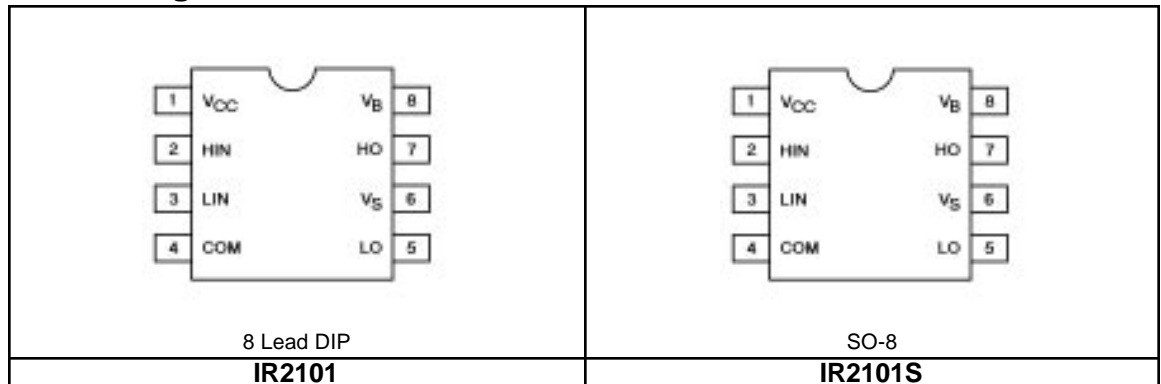
## Functional Block Diagram



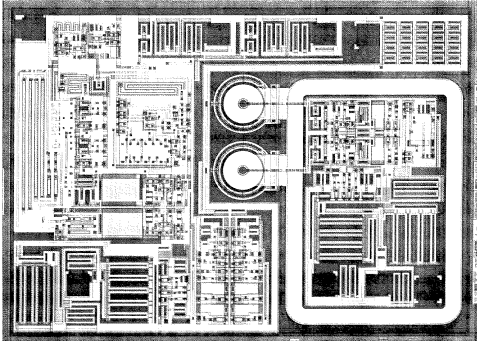
## Lead Definitions

Lead	
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments



**Device Information**

Process & Design Rule		HVDCMOS 4.0 $\mu$ m
Transistor Count		168
Die Size		67 X 91 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
	First Layer	Width Spacing Thickness
		4 $\mu$ m 6 $\mu$ m 5000Å
Second Layer	Material	Al - Si (Si: 1.0% $\pm$ 0.1%)
	Width Spacing Thickness	6 $\mu$ m 9 $\mu$ m 20,000Å
Contact Hole Dimension		5 $\mu$ m X 5 $\mu$ m
Insulation Layer	Material	PSG (SiO <sub>2</sub> )
	Thickness	1.5 $\mu$ m
Passivation	Material	PSG (SiO <sub>2</sub> )
	Thickness	1.5 $\mu$ m
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 Lead PDIP / SO-8
	Materials	EME6300 / MP150 / MP190
Remarks:		

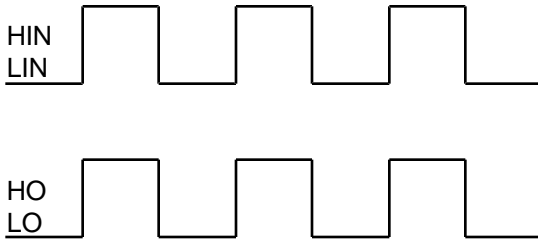


Figure 1. Input/Output Timing Diagram

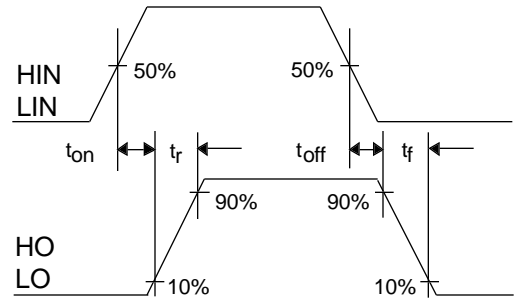


Figure 2. Switching Time Waveform Definitions

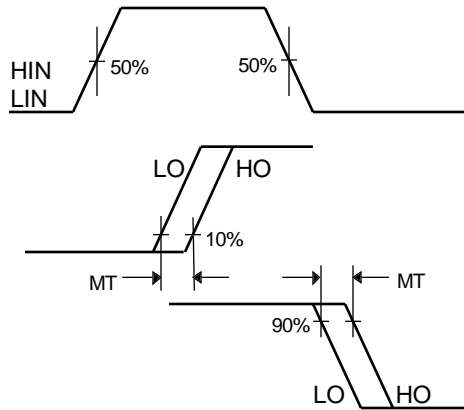


Figure 3. Delay Matching Waveform Definitions