

# IR2112

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V  
Logic and power ground  $\pm 5V$  offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

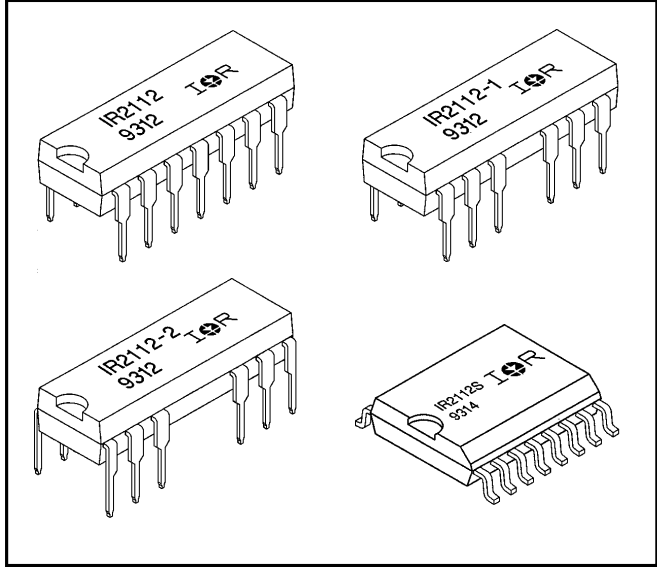
### Description

The IR2112 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

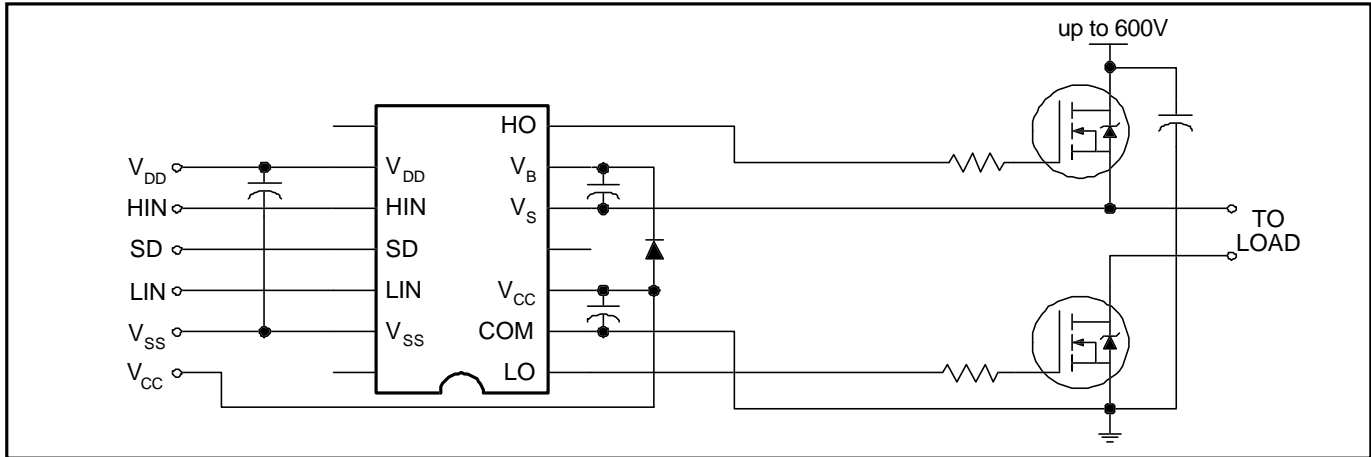
### Product Summary

<b>V<sub>OFFSET</sub></b>	<b>600V max.</b>
<b>I<sub>O+/-</sub></b>	<b>200 mA / 420 mA</b>
<b>V<sub>OUT</sub></b>	<b>10 - 20V</b>
<b>t<sub>on/off (typ.)</sub></b>	<b>125 &amp; 105 ns</b>
<b>Delay Matching</b>	<b>30 ns</b>

### Packages



### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Voltage	-0.3	625	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low Side Fixed Supply Voltage	-0.3	25	
V <sub>LO</sub>	Low Side Output Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>DD</sub>	Logic Supply Voltage	-0.3	V <sub>SS</sub> + 25	
V <sub>SS</sub>	Logic Supply Offset Voltage	V <sub>CC</sub> - 25	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic Input Voltage (HIN, LIN & SD)	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>A</sub> ≤ +25°C (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	—	1.6	
	(16 Lead SOIC)	—	1.25	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 5 & 6)	—	75	
	(16 Lead SOIC)	—	100	
T <sub>J</sub>	Junction Temperature	—	150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	Note 1	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low Side Fixed Supply Voltage	10	20	
V <sub>LO</sub>	Low Side Output Voltage	0	V <sub>CC</sub>	
V <sub>DD</sub>	Logic Supply Voltage	V <sub>SS</sub> + 5	V <sub>SS</sub> + 20	
V <sub>SS</sub>	Logic Supply Offset Voltage	-5	5	
V <sub>IN</sub>	Logic Input Voltage (HIN, LIN & SD)	V <sub>SS</sub>	V <sub>DD</sub>	
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V,  $C_L$  = 1000 pF,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

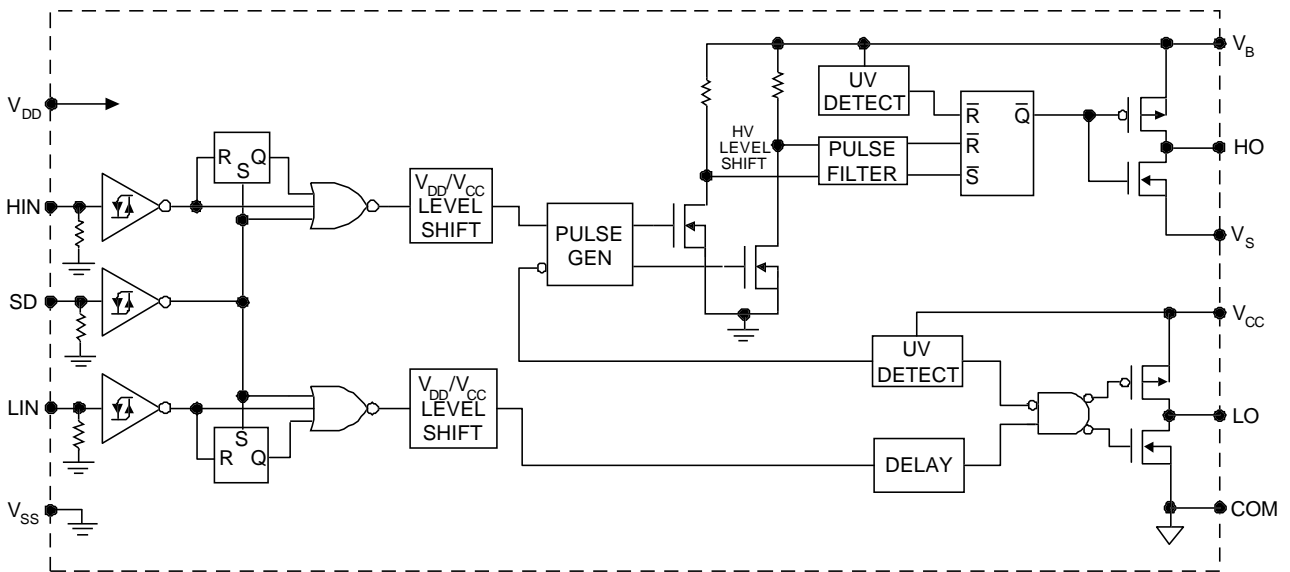
Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
$t_{on}$	Turn-On Propagation Delay	7	—	125	180	ns	$V_S = 0V$
$t_{off}$	Turn-Off Propagation Delay	8	—	105	160		$V_S = 600V$
$t_{sd}$	Shutdown Propagation Delay	9	—	105	160		$V_S = 600V$
$t_r$	Turn-On Rise Time	10	—	80	130		
$t_f$	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
$V_{IH}$	Logic "1" Input Voltage	12	9.5	—	—	V	
$V_{IL}$	Logic "0" Input Voltage	13	—	—	6.0		
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	14	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low Level Output Voltage, $V_O$	15	—	—	100		$I_O = 0A$
$I_{LK}$	Offset Supply Leakage Current	16	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	17	—	25	60		$V_{IN} = 0V$ or $V_{DD}$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	18	—	80	180		$V_{IN} = 0V$ or $V_{DD}$
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	19	—	2.0	5.0		$V_{IN} = 0V$ or $V_{DD}$
$I_{IN+}$	Logic "1" Input Bias Current	20	—	20	40		$V_{IN} = V_{DD}$
$I_{IN-}$	Logic "0" Input Bias Current	21	—	—	1.0		$V_{IN} = 0V$
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
$I_{O+}$	Output High Short Circuit Pulsed Current	26	200	250	—	A	$V_O = 0V, V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
$I_{O-}$	Output Low Short Circuit Pulsed Current	27	420	500	—		$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$

## Functional Block Diagram



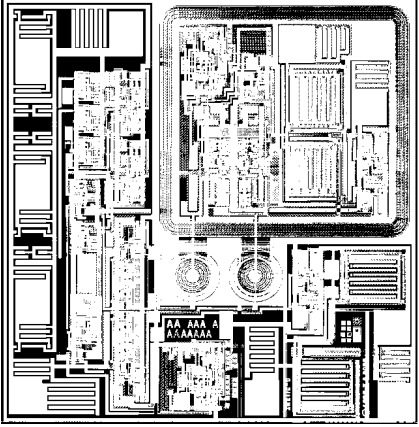
## Lead Definitions

Lead Symbol	Description
V <sub>DD</sub>	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V <sub>SS</sub>	Logic ground
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

<p>14 Lead DIP</p>	<p>14 Lead DIP w/o Lead 4</p>	<p>16 Lead DIP w/o Leads 4 &amp; 5</p>	<p>16 Lead SOIC (Wide Body)</p>
<b>IR2112</b>	<b>IR2112-1</b>	<b>IR2112-2</b>	<b>IR2112S</b>
<b>Part Number</b>			

**Device Information**

Process & Design Rule		HVDCMOS 4.0 $\mu\text{m}$
Transistor Count		220
Die Size		100 X 117 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800 $\text{\AA}$
Connections	Material	Poly Silicon
	First Layer	
	Width	4 $\mu\text{m}$
	Spacing	6 $\mu\text{m}$
	Thickness	5000 $\text{\AA}$
Second Layer	Material	Al - Si (Si: 1.0% $\pm$ 0.1%)
	Width	6 $\mu\text{m}$
	Spacing	9 $\mu\text{m}$
	Thickness	20,000 $\text{\AA}$
Contact Hole Dimension		8 $\mu\text{m}$ X 8 $\mu\text{m}$
Insulation Layer	Material	PSG ( $\text{SiO}_2$ )
	Thickness	1.5 $\mu\text{m}$
Passivation	Material	PSG ( $\text{SiO}_2$ )
	Thickness	1.5 $\mu\text{m}$
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	14 & 16 Lead PDIP / 16 Lead SOIC
	Materials	EME6300 / MP150 / MP190
Remarks:		

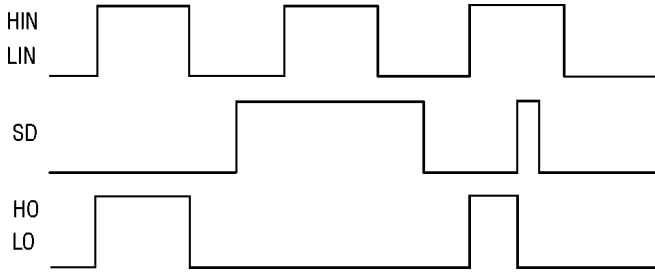


Figure 1. Input/Output Timing Diagram

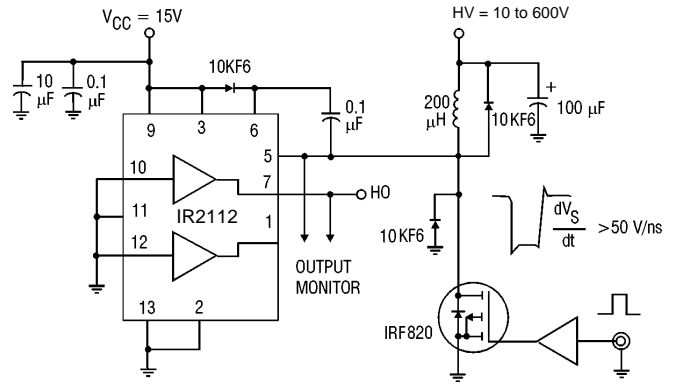


Figure 2. Floating Supply Voltage Transient Test Circuit

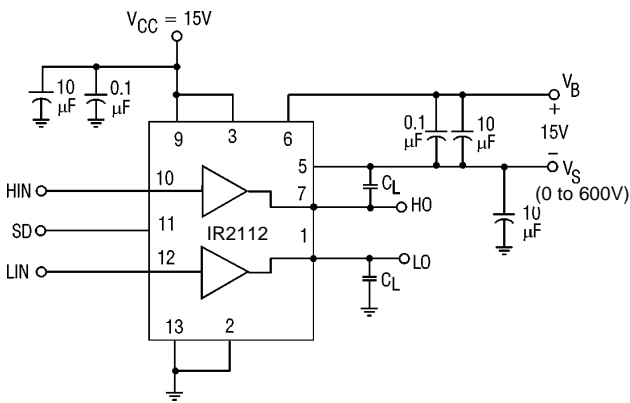


Figure 3. Switching Time Test Circuit

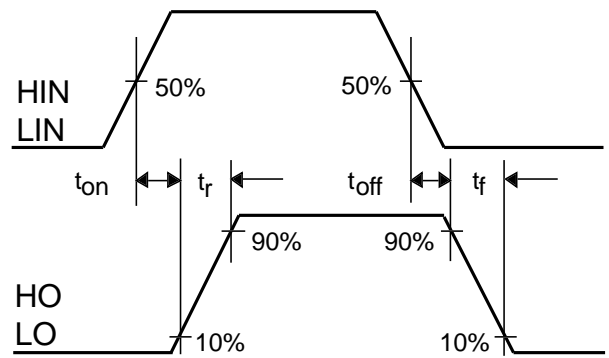


Figure 4. Switching Time Waveform Definition

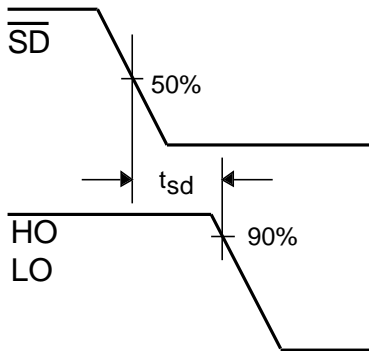


Figure 3. Shutdown Waveform Definitions

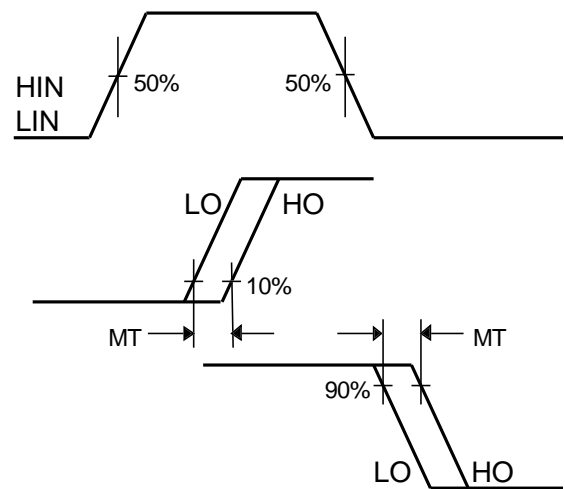
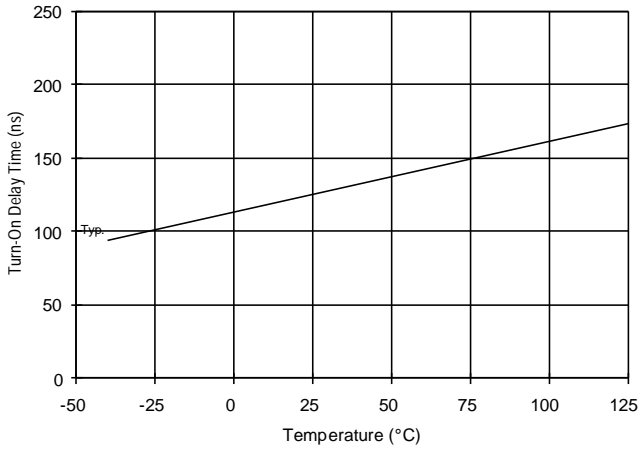
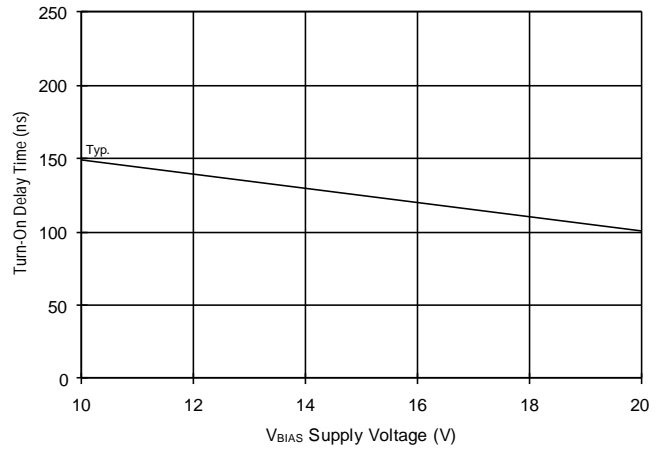


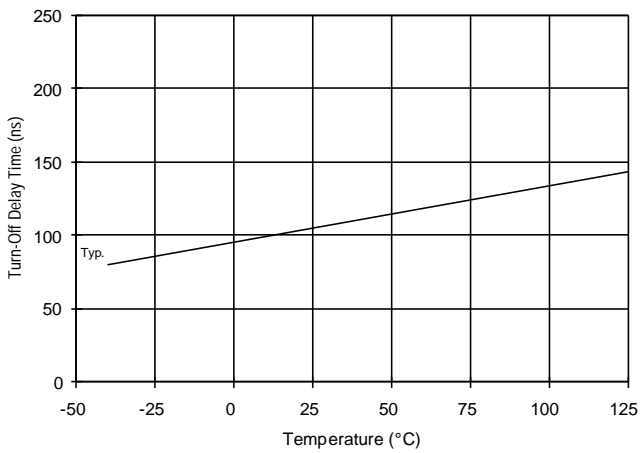
Figure 6. Delay Matching Waveform Definitions



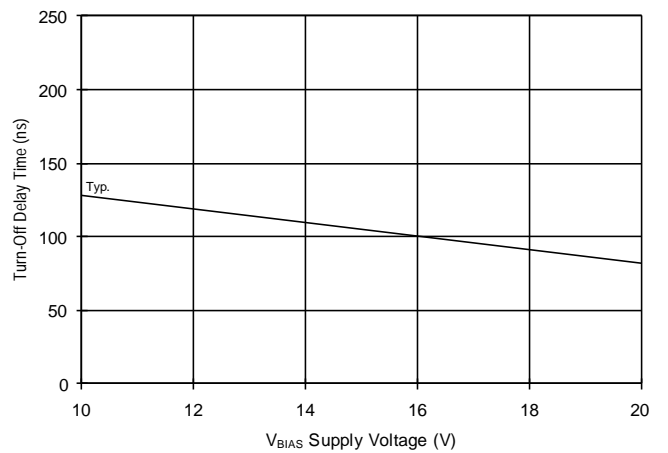
**Figure 7A. Turn-On Time vs. Temperature**



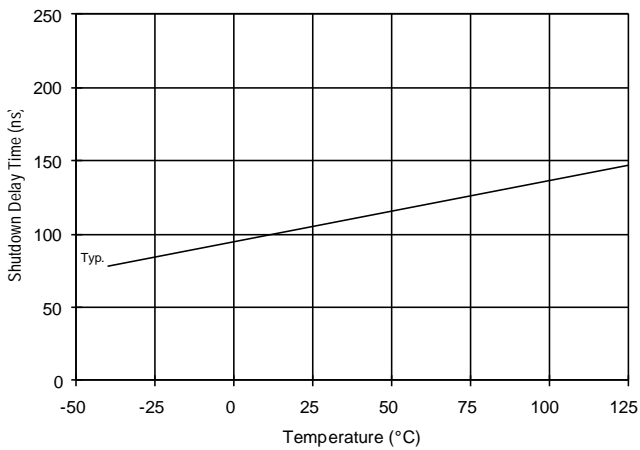
**Figure 7B. Turn-On Time vs. Voltage**



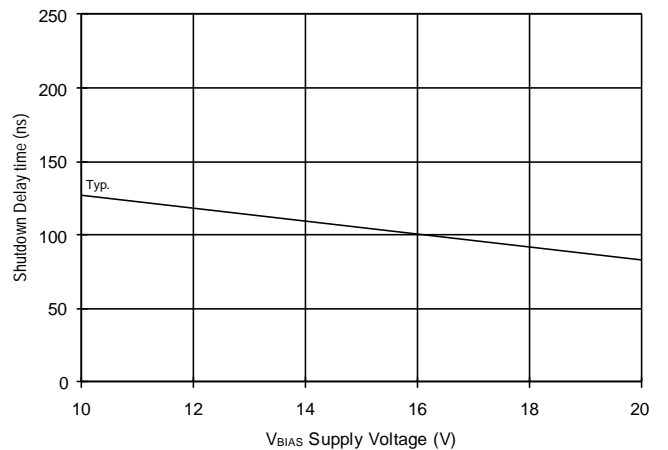
**Figure 8A. Turn-Off Time vs. Temperature**



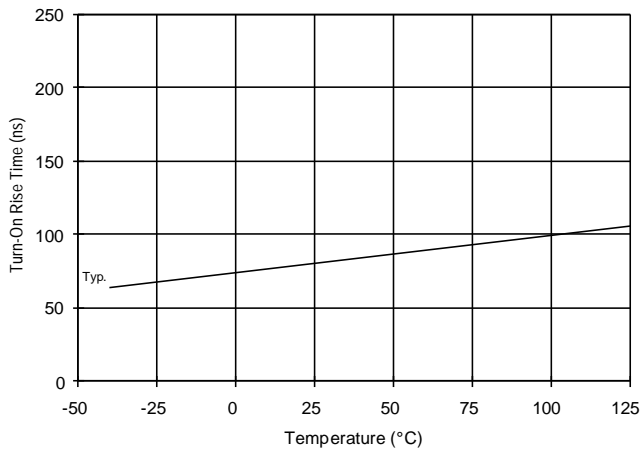
**Figure 8B. Turn-Off Time vs. Voltage**



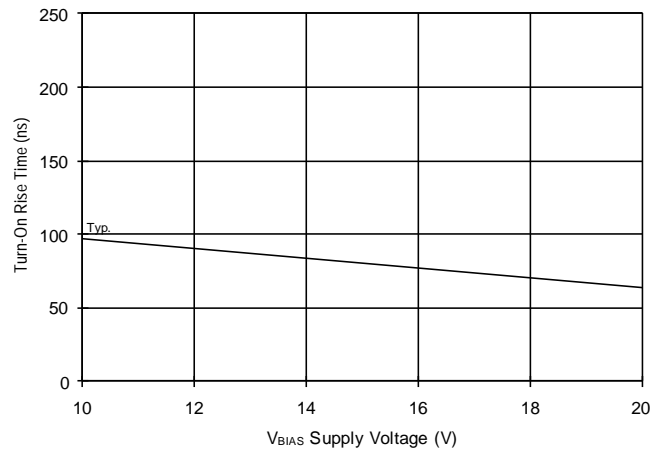
**Figure 9A. Shutdown Time vs. Temperature**



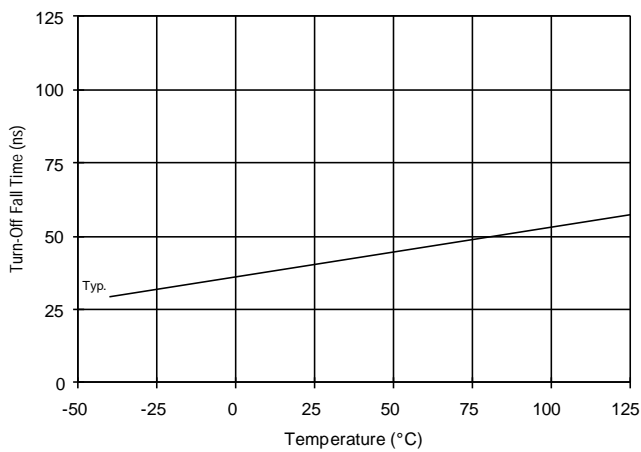
**Figure 9B. Shutdown Time vs. Voltage**



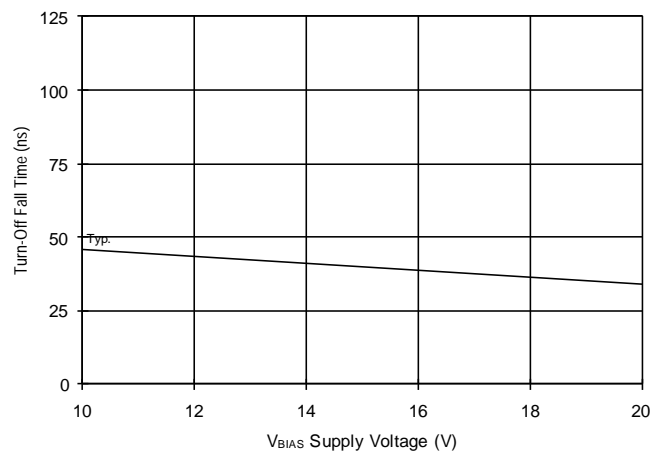
**Figure 10A. Turn-On Rise Time vs. Temperature**



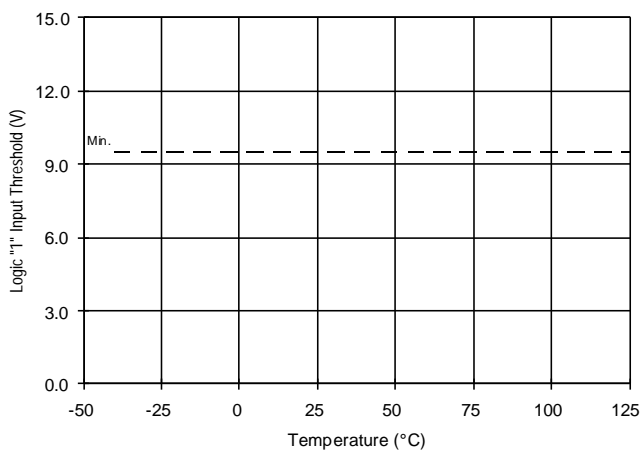
**Figure 10B. Turn-On Rise Time vs. Voltage**



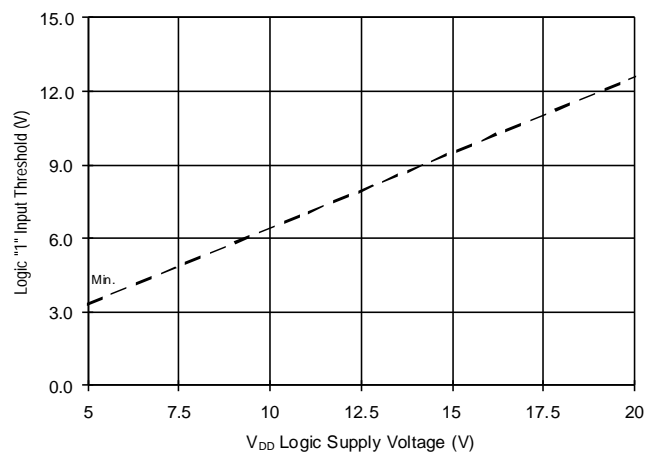
**Figure 11A. Turn-Off Fall Time vs. Temperature**



**Figure 11B. Turn-Off Fall Time vs. Voltage**

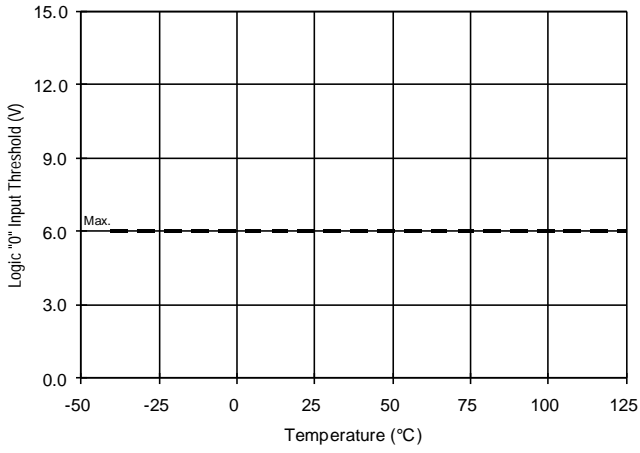


**Figure 12A. Logic "1" Input Threshold vs. Temperature**

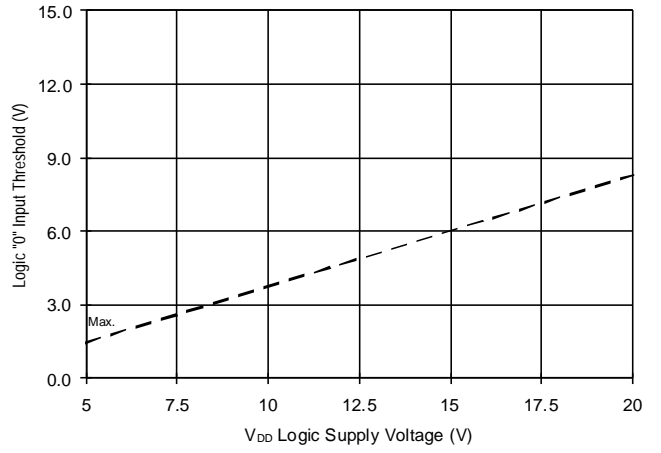


**Figure 12B. Logic "1" Input Threshold vs. Voltage**

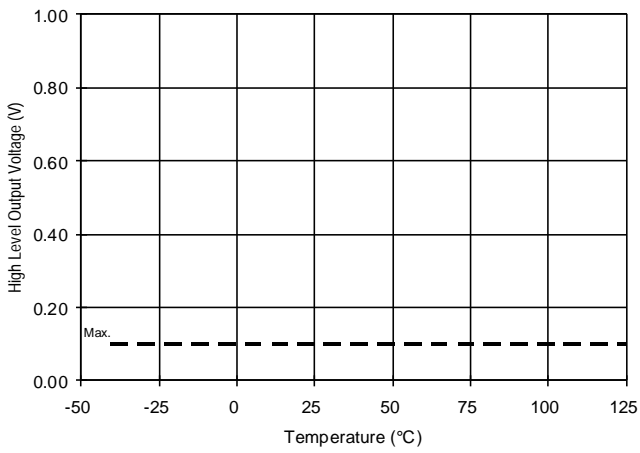




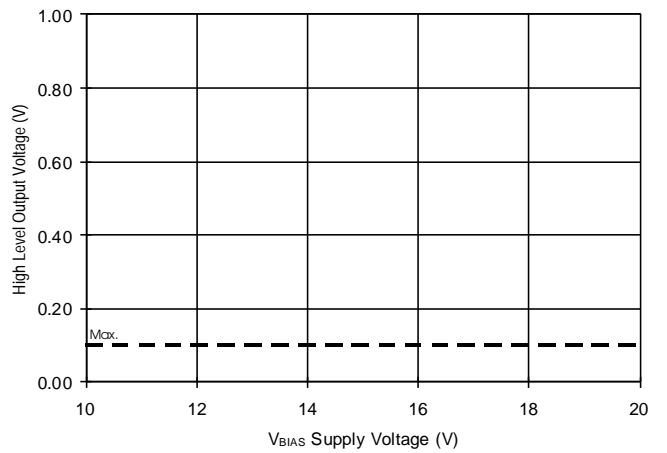
**Figure 13A. Logic "0" Input Threshold vs. Temperature**



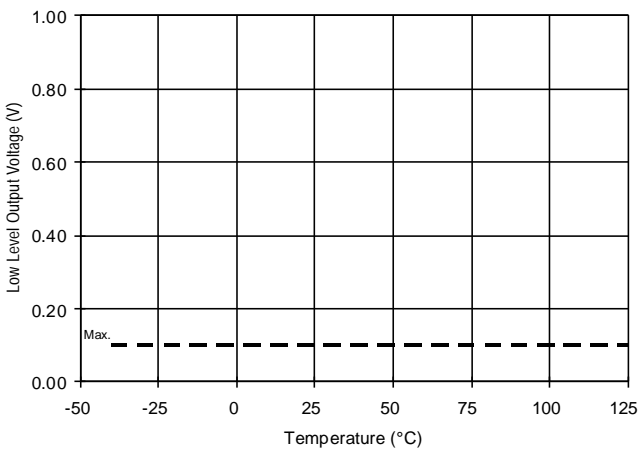
**Figure 13B. Logic "0" Input Threshold vs. Voltage**



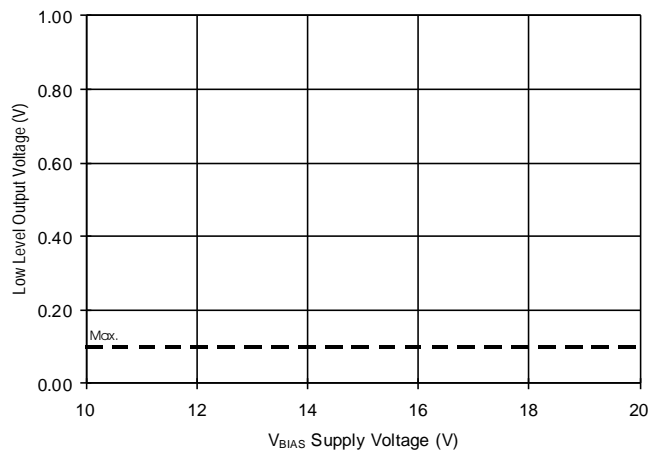
**Figure 14A. High Level Output vs. Temperature**



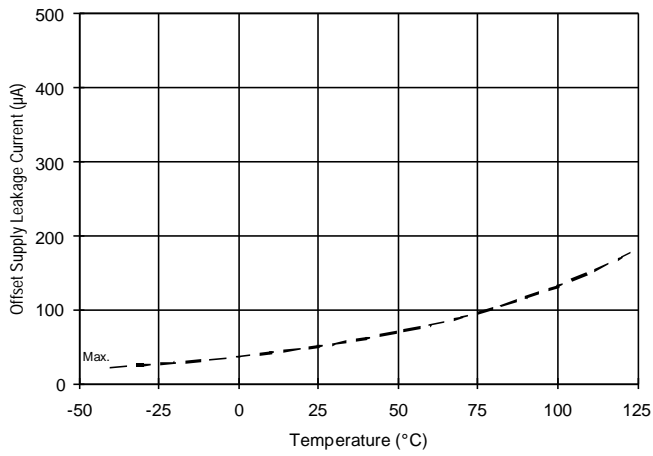
**Figure 14B. High Level Output vs. Voltage**



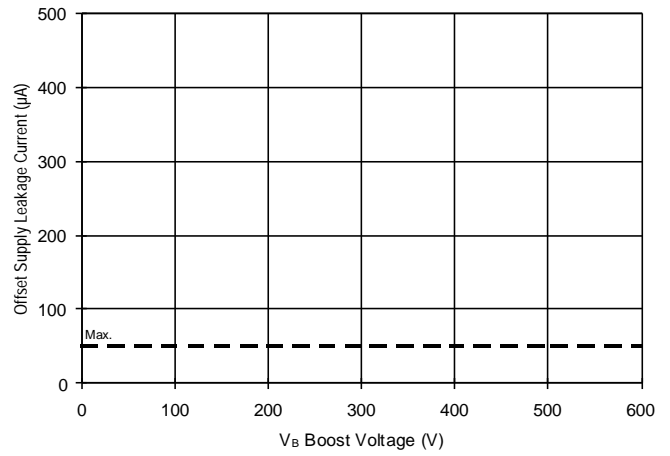
**Figure 15A. Low Level Output vs. Temperature**



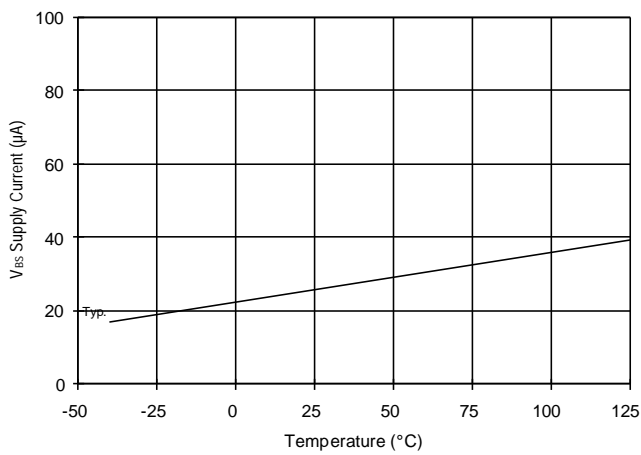
**Figure 15B. Low Level Output vs. Voltage**



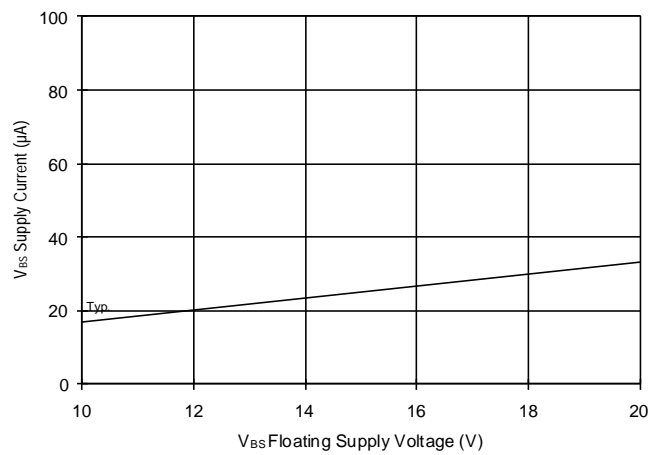
**Figure 16A. Offset Supply Current vs. Temperature**



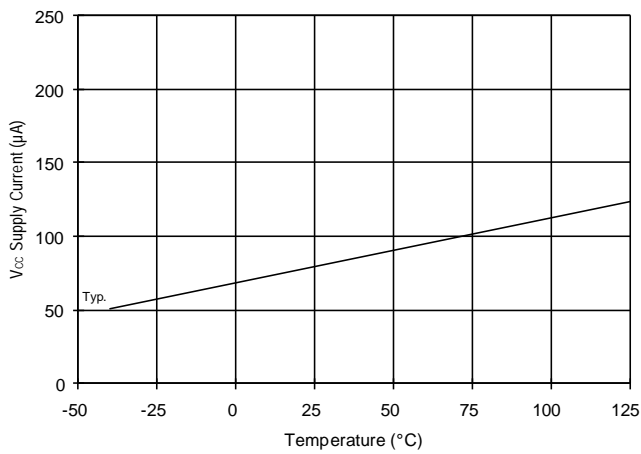
**Figure 16B. Offset Supply Current vs. Voltage**



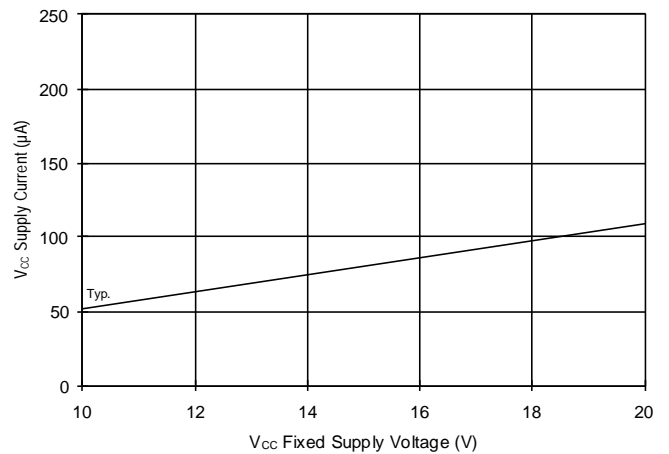
**Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature**



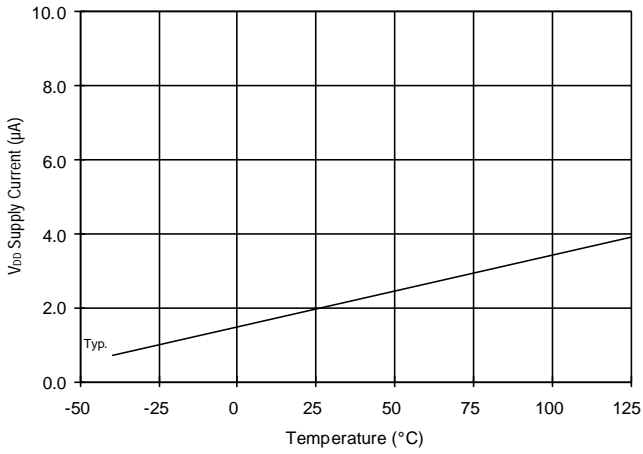
**Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage**



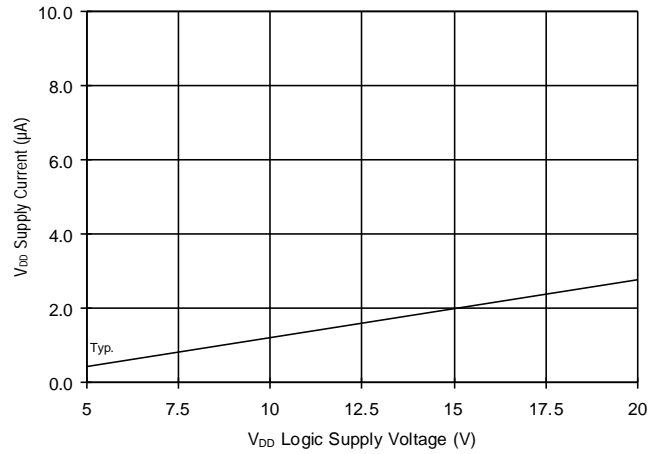
**Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature**



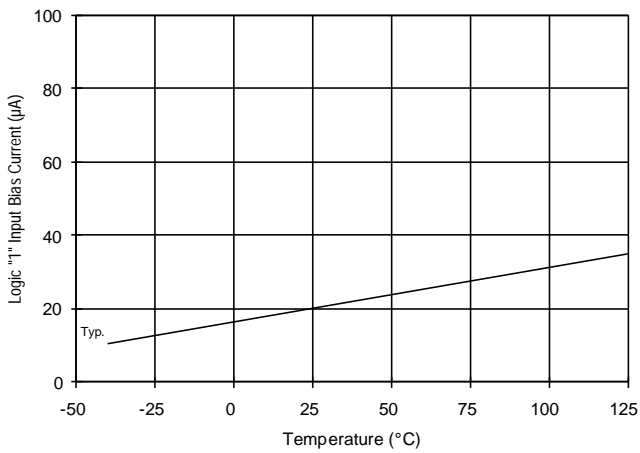
**Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage**



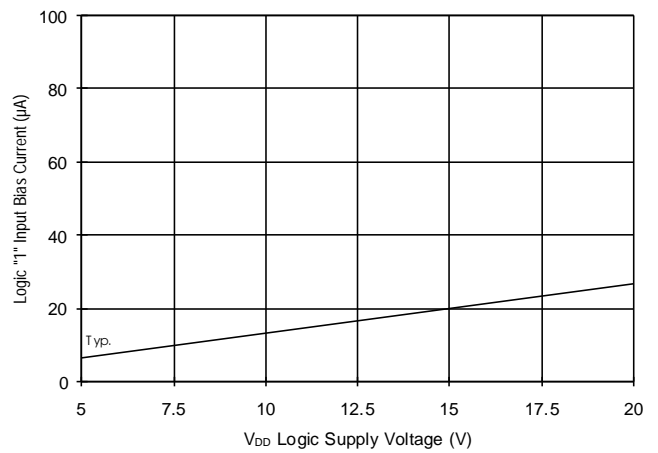
**Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature**



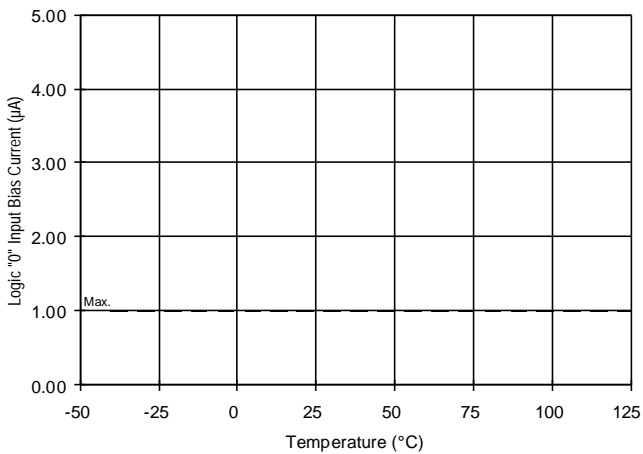
**Figure 19B. V<sub>DD</sub> Supply Current vs. Voltage**



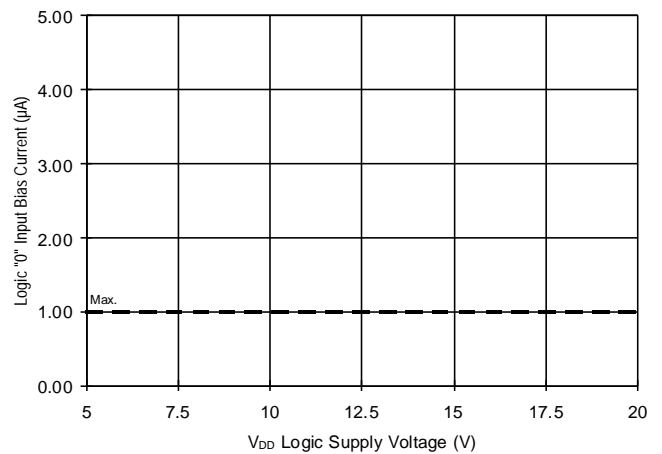
**Figure 20A. Logic "1" Input Current vs. Temperature**



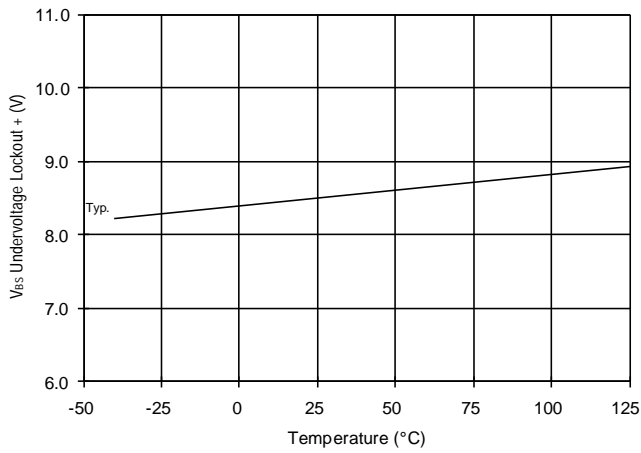
**Figure 20B. Logic "1" Input Current vs. Voltage**



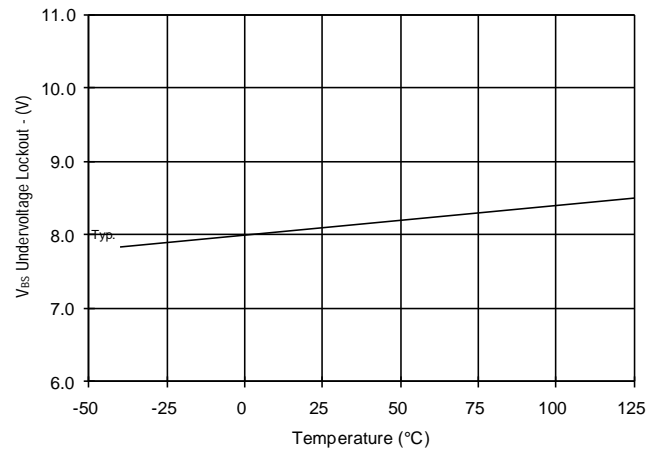
**Figure 21A. Logic "0" Input Current vs. Temperature**



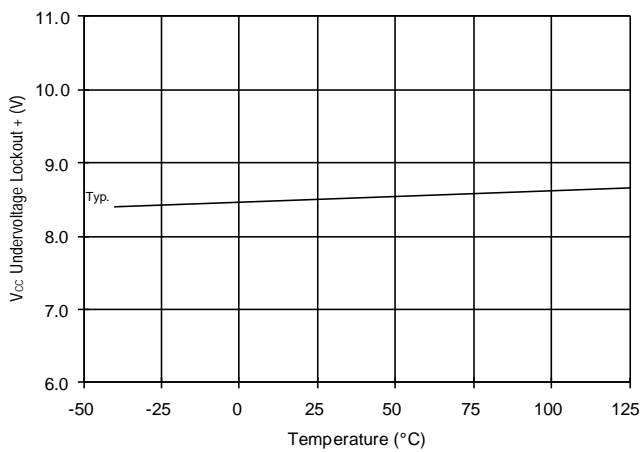
**Figure 21B. Logic "0" Input Current vs. Voltage**



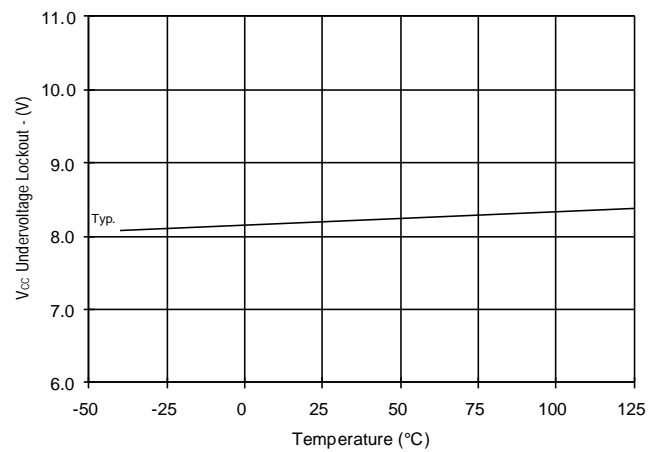
**Figure 22. V<sub>BS</sub> Undervoltage (+) vs. Temperature**



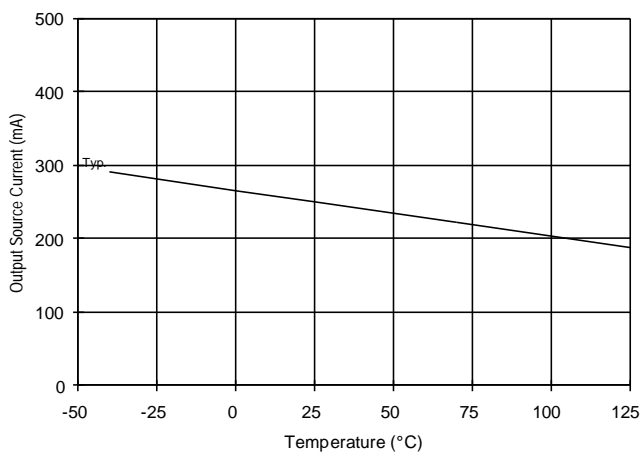
**Figure 23. V<sub>BS</sub> Undervoltage (-) vs. Temperature**



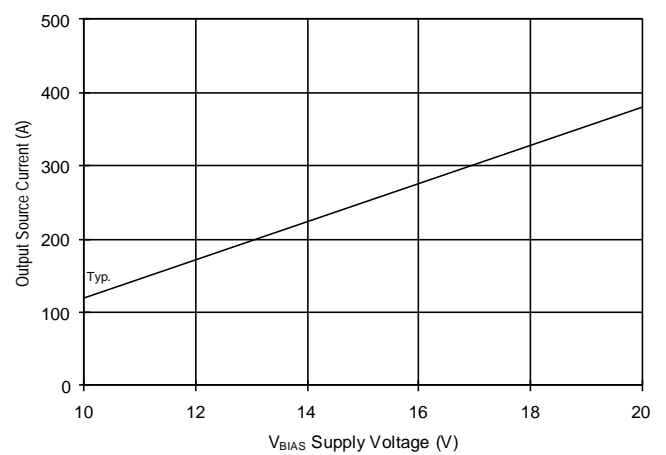
**Figure 24. V<sub>CC</sub> Undervoltage (+) vs. Temperature**



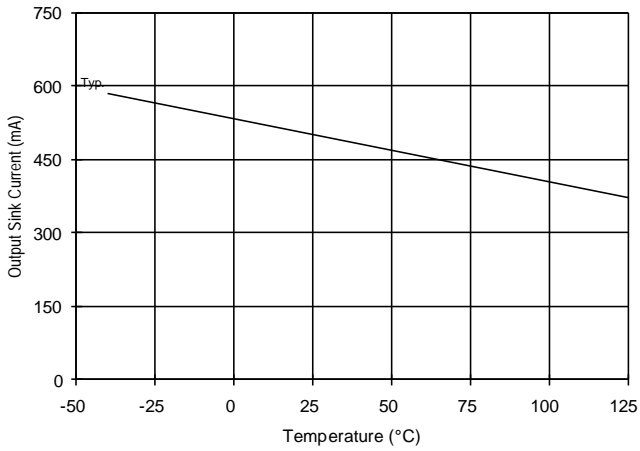
**Figure 25. V<sub>CC</sub> Undervoltage (-) vs. Temperature**



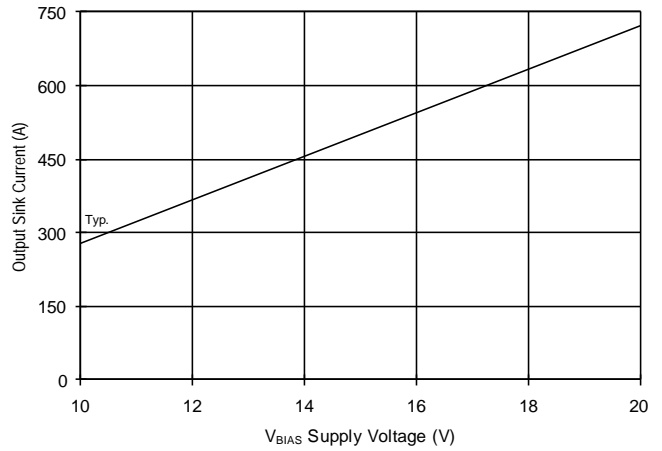
**Figure 26A. Output Source Current vs. Temperature**



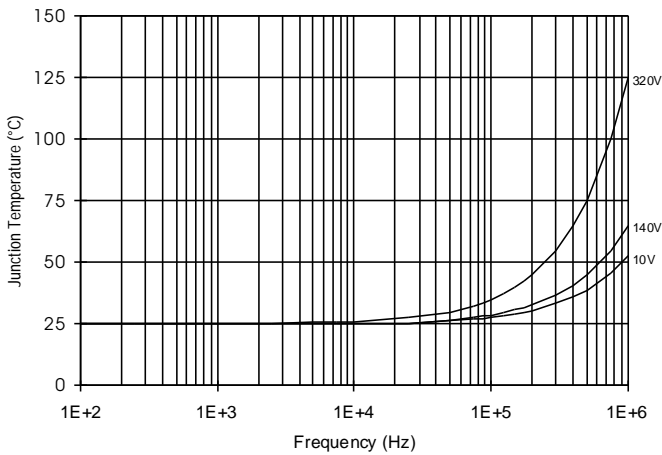
**Figure 26B. Output Source Current vs. Voltage**



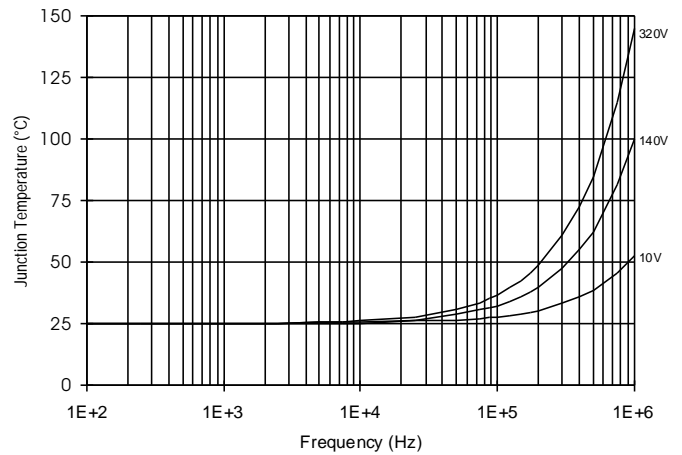
**Figure 27A. Output Sink Current vs. Temperature**



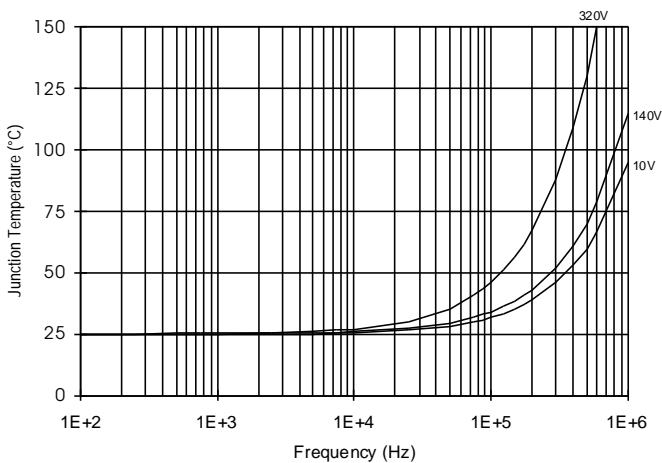
**Figure 27B. Output Sink Current vs. Voltage**



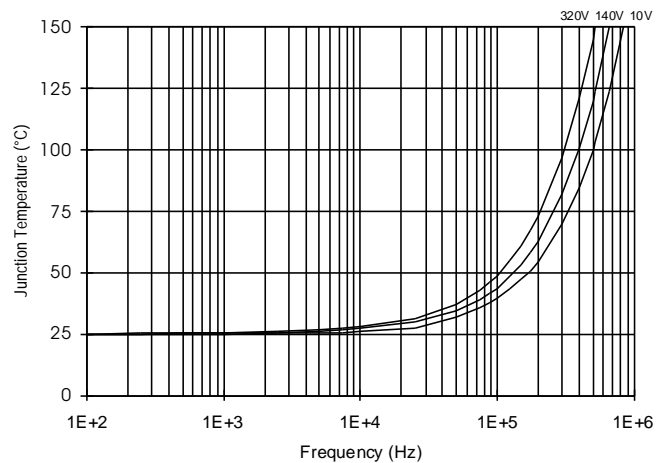
**Figure 28. IR2112  $T_J$  vs. Frequency (IRFBC20)**  
 $R_{GATE} = 33\Omega, V_{CC} = 15V$



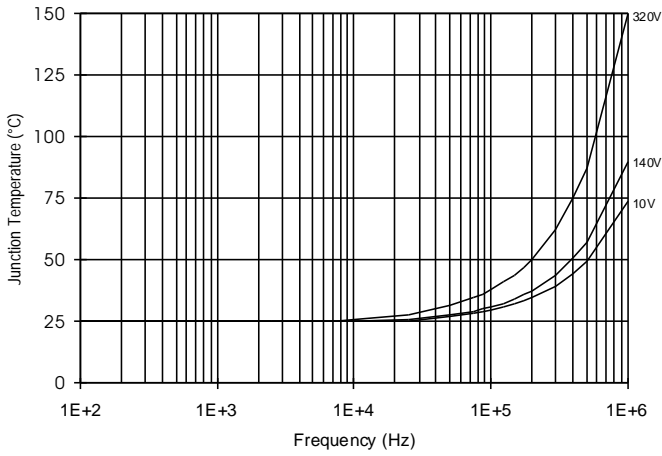
**Figure 29. IR2112  $T_J$  vs. Frequency (IRFBC30)**  
 $R_{GATE} = 22\Omega, V_{CC} = 15V$



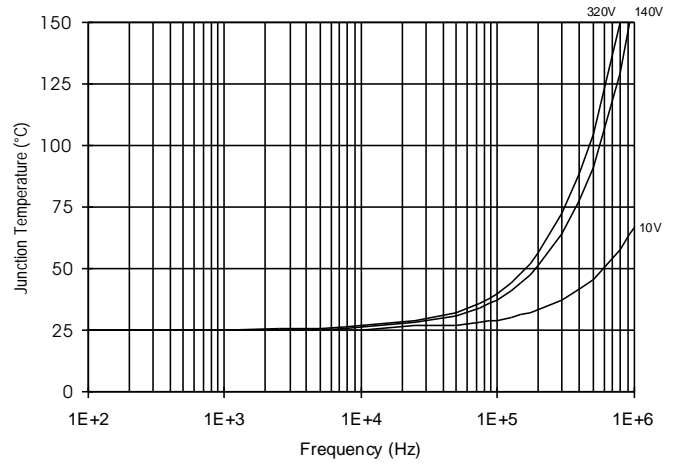
**Figure 30. IR2112  $T_J$  vs. Frequency (IRFBC40)**  
 $R_{GATE} = 15\Omega, V_{CC} = 15V$



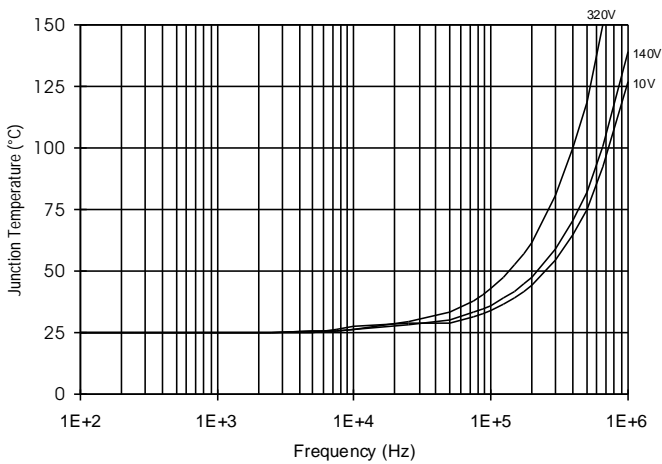
**Figure 31. IR2112  $T_J$  vs. Frequency (IRFPE50)**  
 $R_{GATE} = 10\Omega, V_{CC} = 15V$



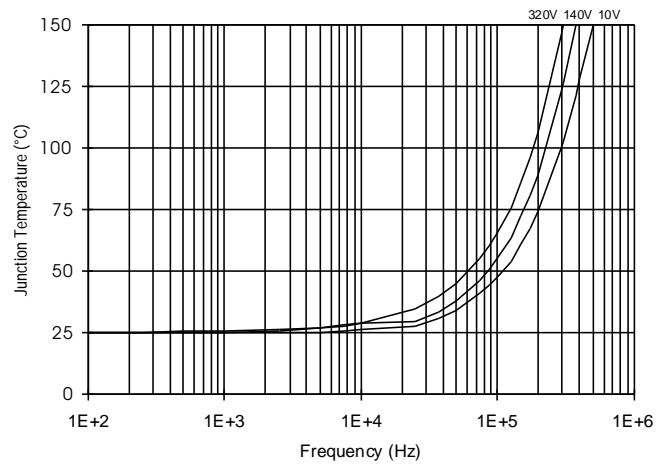
**Figure 32. IR2112S  $T_J$  vs. Frequency (IRFBC20)**  
 $R_{GATE} = 33\Omega, V_{CC} = 15V$



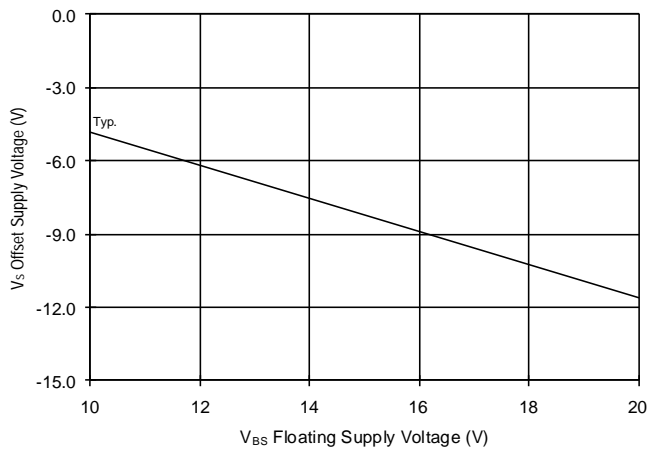
**Figure 33. IR2112S  $T_J$  vs. Frequency (IRFBC30)**  
 $R_{GATE} = 22\Omega, V_{CC} = 15V$



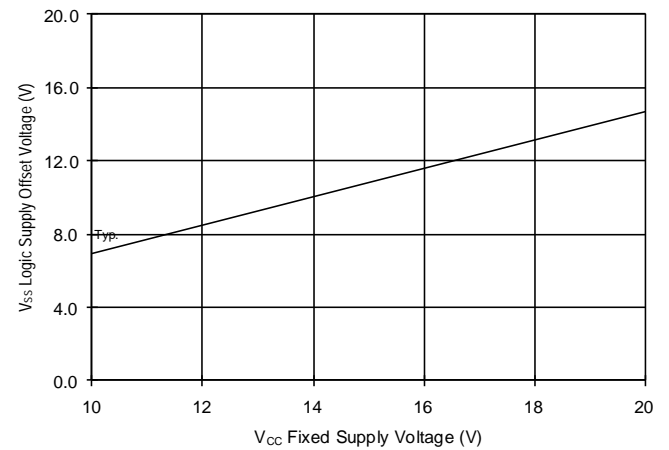
**Figure 34. IR2112S  $T_J$  vs. Frequency (IRFBC40)**  
 $R_{GATE} = 15\Omega, V_{CC} = 15V$



**Figure 35. IR2112S  $T_J$  vs. Frequency (IRFPE50)**  
 $R_{GATE} = 10\Omega, V_{CC} = 15V$



**Figure 36. Maximum  $V_S$  Negative Offset vs.  $V_{BS}$  Supply Voltage**



**Figure 37. Maximum  $V_{SS}$  Positive Offset vs.  $V_{CC}$  Supply Voltage**