International
IOR Rectifier

Provisional Data Sheet No. PD-9.1556

# HEXFET® POWER MOSFET

# IRFNG50

N-CHANNEL

## 1000 Volt, 2.0Ω HEXFET

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

The Surface Mount Device (SMD-1) package represents another step in the continual evolution of surface mount technology. The SMD-1 will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the SMD-1 package to meet the specific needs of the power market by increasing the size of the termination pads, thereby enhancing thermal and electrical performance.

## Product Summary

| Part Number | $BV_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRFNG50 | 1000V | 2.0Ω | 5.5A |

## Features:

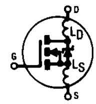
- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light-weight

## Absolute Maximum Ratings

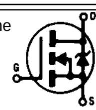
| | Parameter | IRFNG50 | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 25°C | Continuous Drain Current | 5.5 | A |
| $I_D$ @ $V_{GS}$ = 10V, $T_C$ = 100°C | Continuous Drain Current | 3.5 | |
| $I_{DM}$ | Pulsed Drain Current ① | 22 | |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 150 | W |
| | Linear Derating Factor | 1.2 | W/K ⑤ |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 860 | mJ |
| $I_{AR}$ | Avalanche Current ① | 5.5 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 15.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 1.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction<br>Storage Temperature Range | -55 to 150 | °C |
| | Package Mounting Surface Temperature | 300 (for 5 seconds) | |
| | Weight | 2.6 (typical) | g |

**IRFNG50 Device**

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 1000 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0 mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 1.4 | — | V/°C | Reference to 25°C, $I_D$ = 1.0 mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 2.0 | Ω | $V_{GS}$ = 10V, $I_D$ = 3.5A ④ |
| | | — | — | 2.25 | | $V_{GS}$ = 10V, $I_D$ = 5.5A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $g_{fs}$ | Forward Transconductance | 5.2 | — | — | S (℧) | $V_{DS}$ > 15V, $I_{DS}$ = 3.5A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 25 | μA | $V_{DS}$ = 0.8 x Max Rating, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 0.8 x Max Rating $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | 87 | — | 200 | nC | $V_{GS}$ =10V, $I_D$ = 5.5A |
| $Q_{gs}$ | Gate-to-Source Charge | 8.7 | — | 20 | | $V_{DS}$ = Max. Rating x 0.5 |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | 49 | — | 110 | | see figures 6 and 13 |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 30 | ns | $V_{DD}$ = 500V, $I_D$ = 5.5A, |
| $t_r$ | Rise Time | — | — | 44 | | $R_G$ = 2.35Ω, VGS = 10V |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 210 | | |
| $t_f$ | Fall Time | — | — | 60 | | see figure 10 |
| $L_D$ | Internal Drain Inductance | — | 2.0 | — | nH | Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances.  |
| $L_S$ | Internal Source Inductance | — | 6.5 | — | | Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. |
| $C_{iss}$ | Input Capacitance | — | 2400 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V |
| $C_{oss}$ | Output Capacitance | — | 240 | — | | f = 1.0 MHz |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 80 | — | | see figure 5 |

## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 5.5 | A | Modified MOSFET symbol showing the integral reverse p-n junction rectifier.  |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | 22 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.8 | V | $T_j$ = 25°C, $I_S$ = 5.5A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 1200 | ns | $T_j$ = 25°C, $I_F$ = 5.5A, di/dt ≤ 100A/μs |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 8.4 | μC | $V_{DD}$ ≤ 50V ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | | | |

## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | — | — | 0.83 | K/W | |
| $R_{thJPCB}$ | Junction-to-PC Board | — | TBD | — | | Soldered to a copper clad PC board |

## IRFNG50 Device

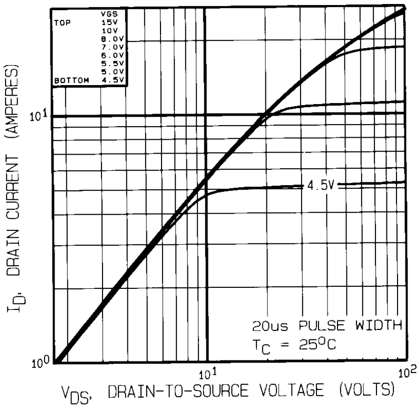



**Fig. 1 — Typical Output Characteristics $T_C$ = 25°C**

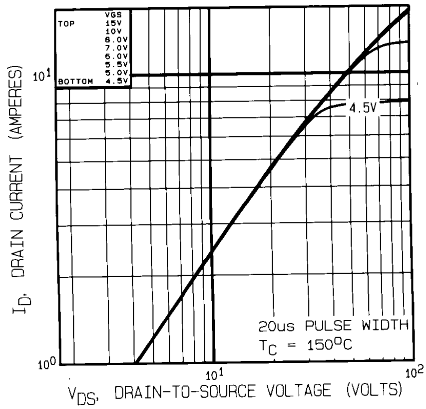



**Fig. 2 — Typical Output Characteristics $T_C$ = 150°C**

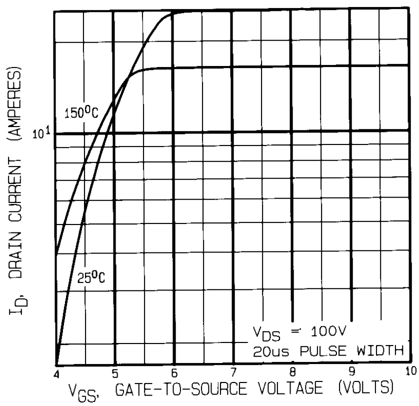



**Fig. 3 — Typical Transfer Characteristics**

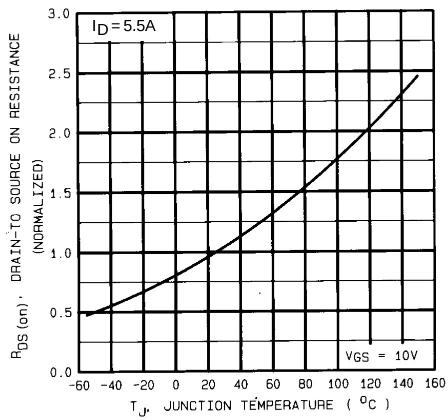



**Fig. 4 — Normalized On-Resistance Vs.Temperature**

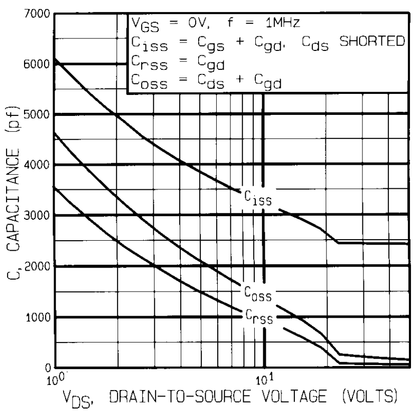



**Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage**

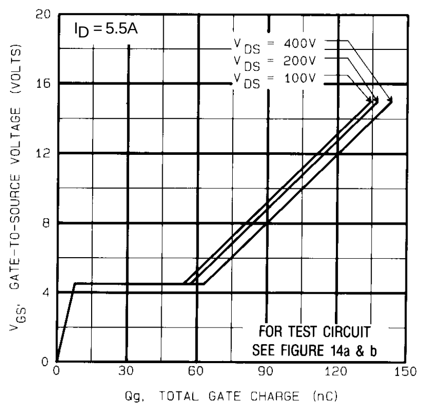



**Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage**

## IRFNG50 Device

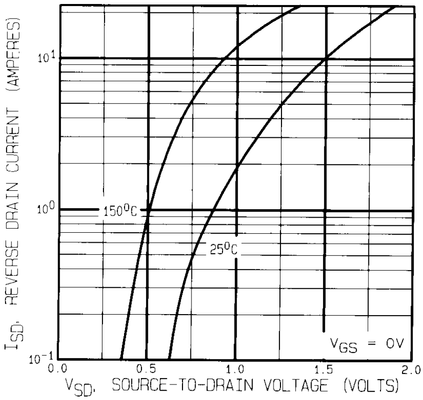



**Fig. 7 — Typical Source-to-Drain Diode Forward Voltage**

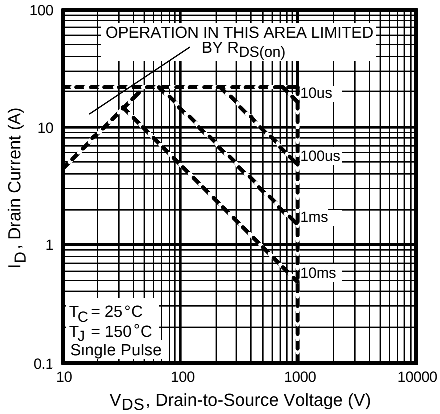



**Fig. 8 — Maximum Safe Operating Area**

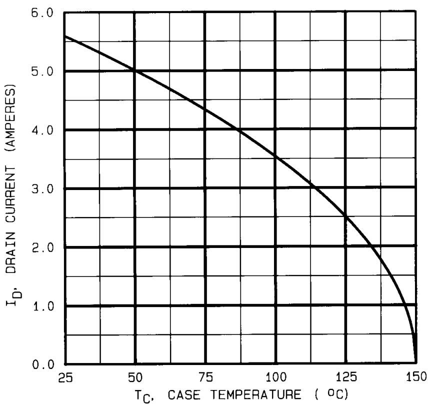



**Fig. 9 — Maximum Drain Current Vs. Case Temperature**

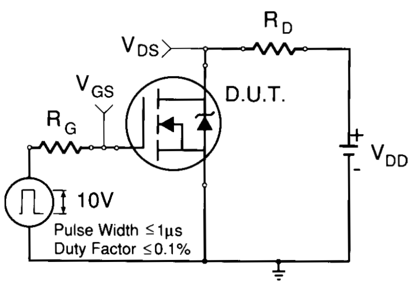



**Fig. 10a — Switching Time Test Circuit**

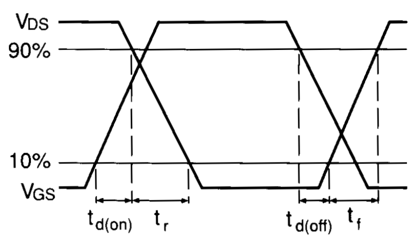



**Fig. 10b — Switching Time Waveforms**

## IRFNG50 Device

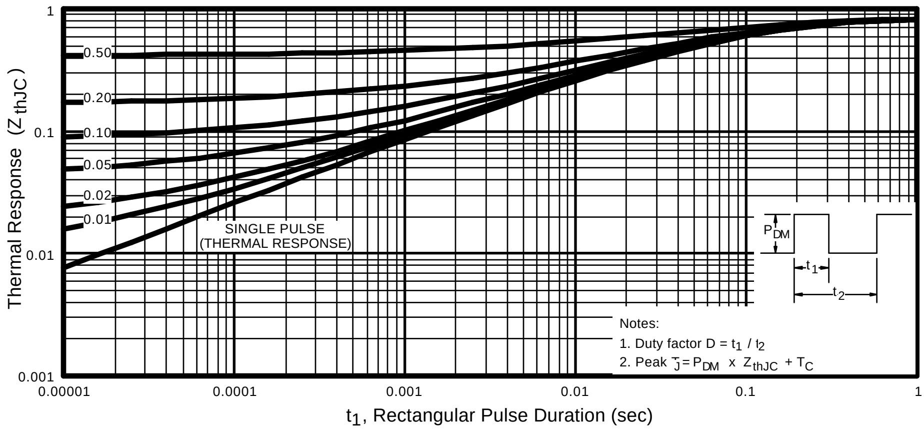



**Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration**

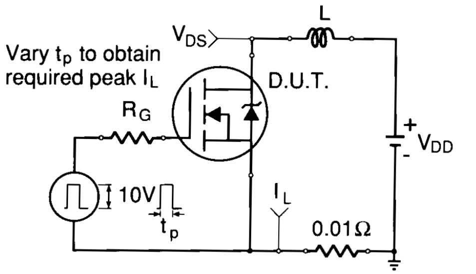



**Fig. 12a — Unclamped Inductive Test Circuit**

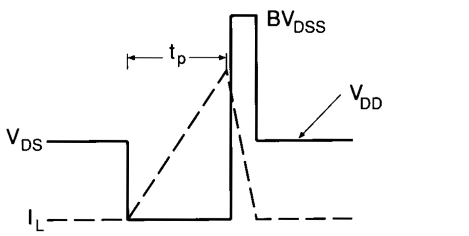



**Fig. 12b — Unclamped Inductive Waveforms**

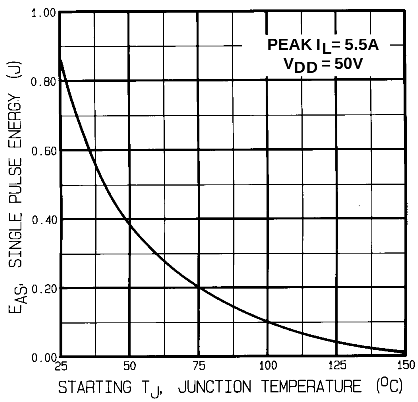



**Fig. 12c — Max. Avalanche Energy vs. Current**

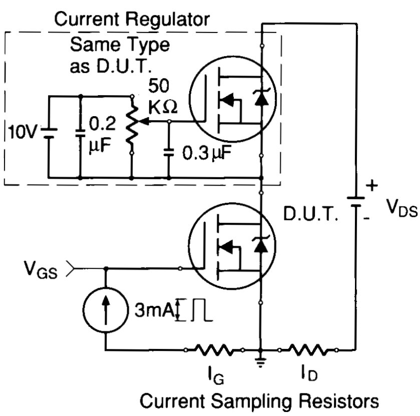



**Fig. 13a — Gate Charge Test Circuit**

**IRFNG50 Device**

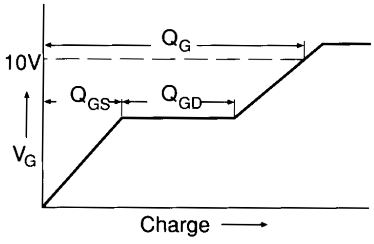



**Fig. 13b — Basic Gate Charge Waveform**

① Repetitive Rating; Pulse width limited by maximum junction temperature. (see figure 11)

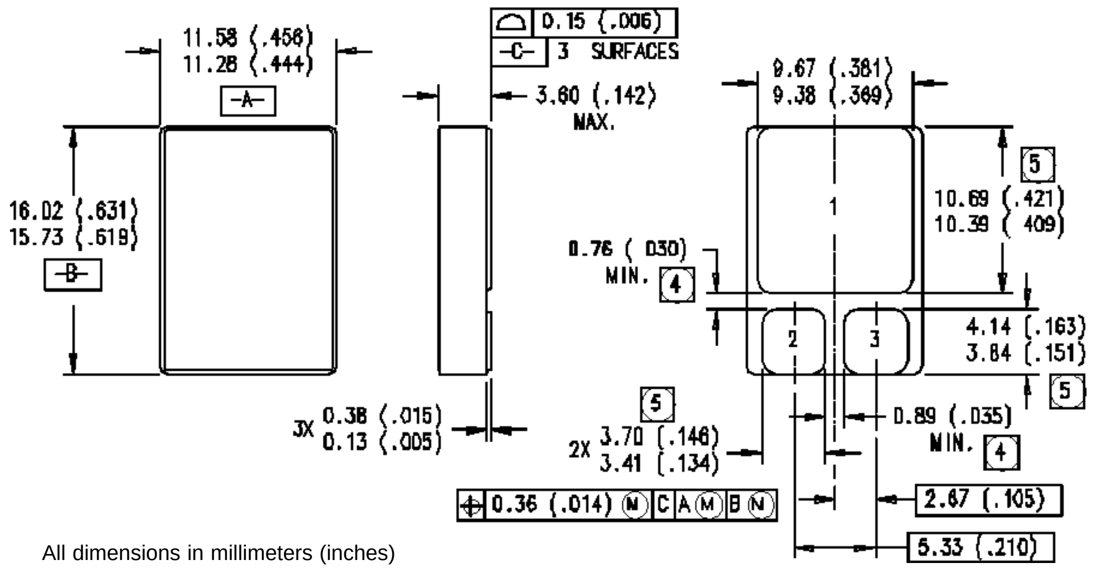
② @ $V_{DD}$ = 50V, Starting $T_J$ = 25°C,
$E_{AS} = [0.5 * L * (I_L^2) * [BV_{DSS}/(BV_{DSS}-V_{DD})]$
Peak $I_L$ = 5.5A, $V_{GS}$ = 10V, 25 ≤ $R_G$ ≤ 200Ω

③ $I_{SD}$ ≤ 5.5A, di/dt ≤ 120A/µs,
$V_{DD}$ ≤ $BV_{DSS}$, $T_J$ ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ K/W = °C/W
W/K = W/°C

## Case Outline and Dimensions — SMD-1




All dimensions in millimeters (inches)

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