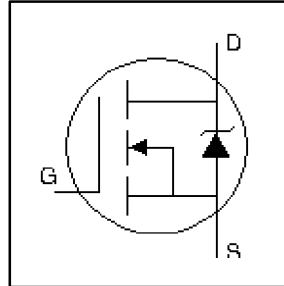


HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- R_{DS(on)} Specified at V_{GS}=4V & 5V
- Fast Switching



$V_{DSS} = 200V$

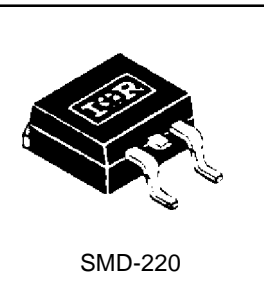
$R_{DS(on)} = 0.80\Omega$

$I_D = 5.2A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface-mount application.



SMD-220

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 5.0 V	5.2	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 5.0 V	3.3	
I _{DM}	Pulsed Drain Current ①	21	
P _D @ T _C = 25°C	Power Dissipation	50	W
P _D @ T _A = 25°C	Power Dissipation (PCB Mount)**	3.1	
	Linear Derating Factor	0.40	W/°C
	Linear Derating Factor (PCB Mount)**	0.025	
V _{GS}	Gate-to-Source Voltage	±10	V
E _{AS}	Single Pulse Avalanche Energy ②	125	mJ
I _{AR}	Avalanche Current ①	5.2	A
E _{AR}	Repetitive Avalanche Energy ①	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	2.5	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount)**	—	—	40	
R _{θJA}	Junction-to-Ambient	—	—	62	

** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques, refer to Application Note AN-994.

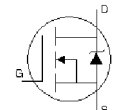
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.80	Ω	$V_{GS} = 10.0V, I_D = 3.1A$ ④
		—	—	1.0		$V_{GS} = 4.0V, I_D = 2.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	1.2	—	—	S	$V_{DS} = 50V, I_D = 3.1A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	16	nC	$I_D = 5.2A$
Q_{gs}	Gate-to-Source Charge	—	—	2.9		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.6		$V_{GS} = 5.0V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	4.2	—		$V_{DD} = 100V$
t_r	Rise Time	—	31	—	ns	$I_D = 5.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		$R_G = 9.0\Omega$
t_f	Fall Time	—	17	—		$R_D = 20\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	360	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	91	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	27	—		$f = 1.0\text{MHz}$, See Fig. 5



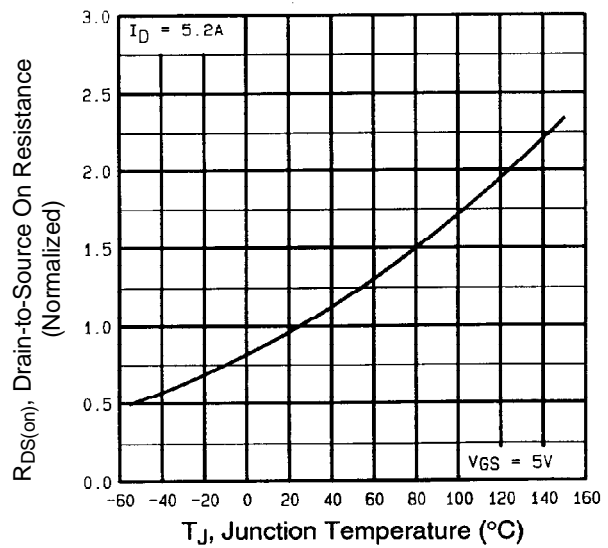
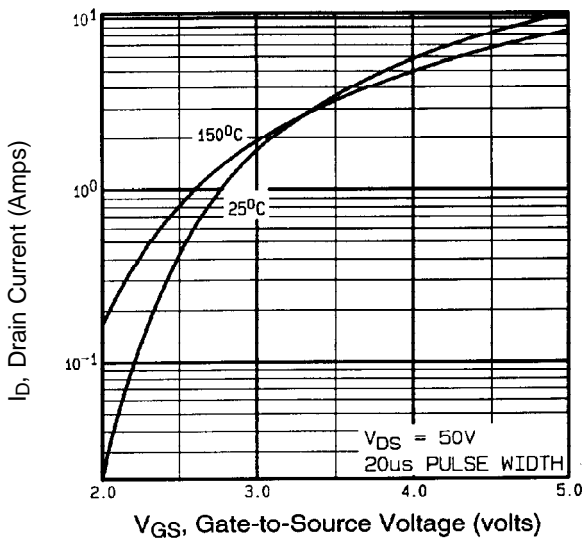
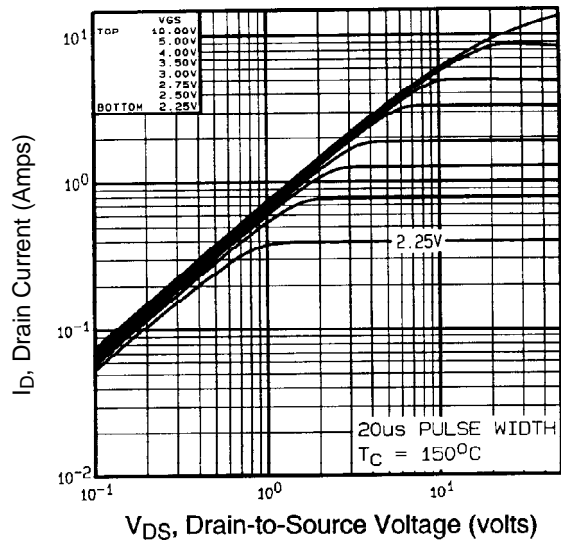
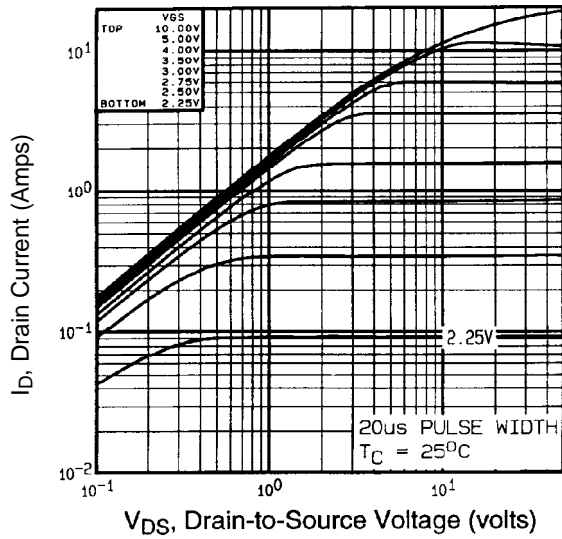
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	$T_J = 25^\circ\text{C}, I_S = 5.2A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	180	270	ns	$T_J = 25^\circ\text{C}, I_F = 5.2A$
Q_{rr}	Reverse Recovery Charge	—	1.1	1.7	μC	$di/dt = 100A/\mu s$ ②
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ\text{C}$, $L = 6.9\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 5.2A$. (See Figure 12)
- ③ $I_{SD} \leq 5.2A$, $di/dt \leq 95A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



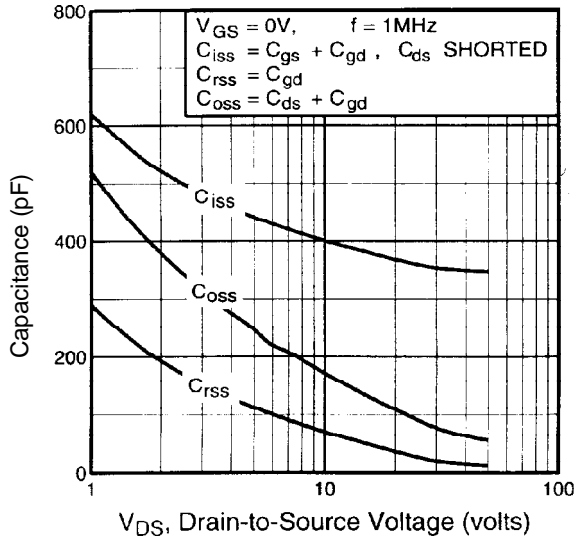


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

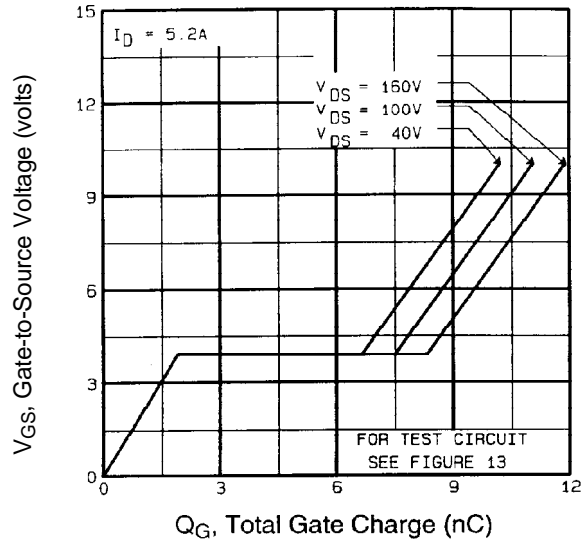


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

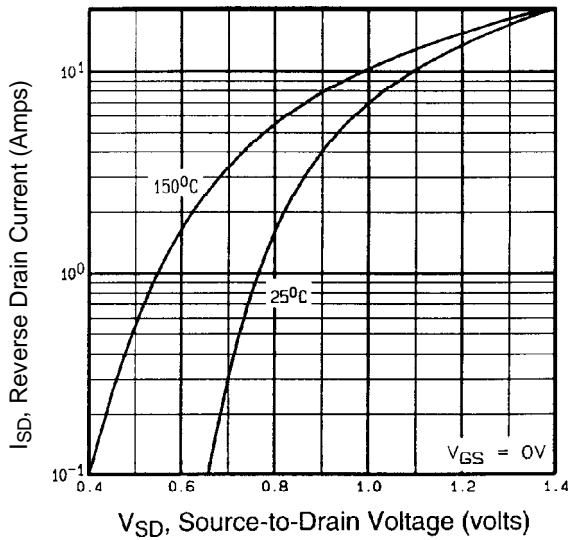


Fig 7. Typical Source-Drain Diode Forward Voltage

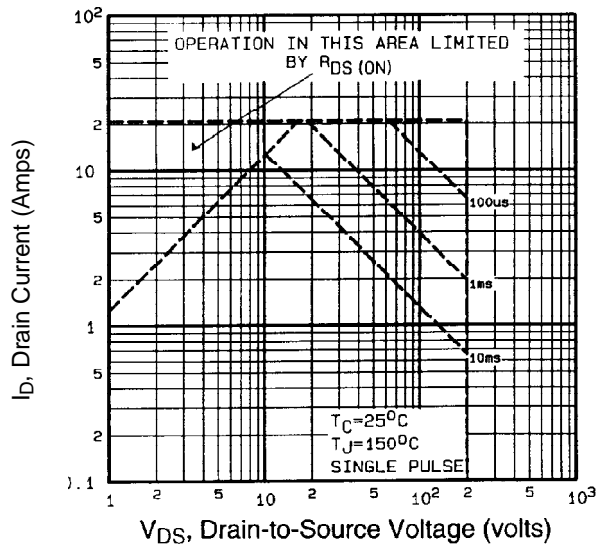


Fig 8. Maximum Safe Operating Area

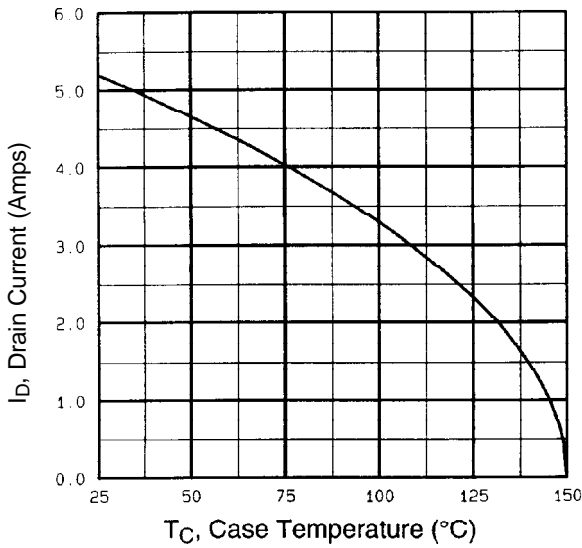


Fig 9. Maximum Drain Current Vs. Case Temperature

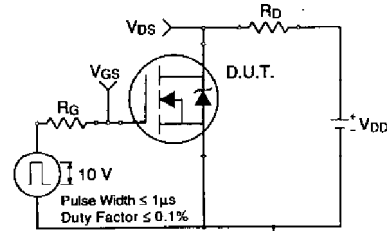


Fig 10a. Switching Time Test Circuit

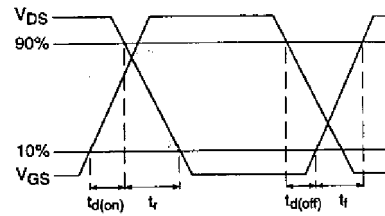


Fig 10b. Switching Time Waveforms

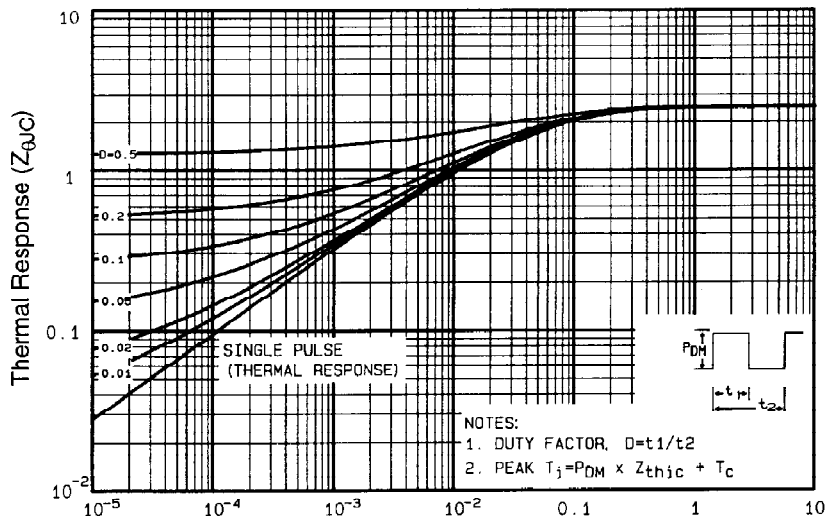


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

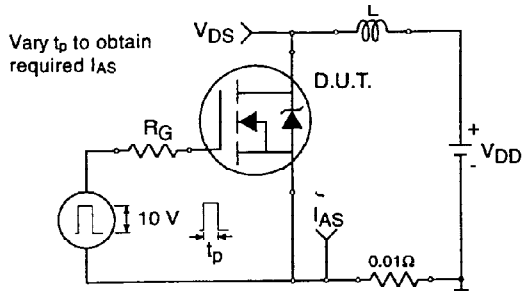


Fig 12a. Unclamped Inductive Test Circuit

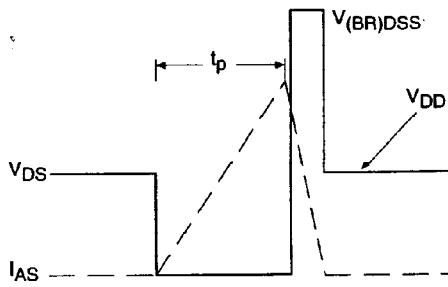


Fig 12b. Unclamped Inductive Waveforms

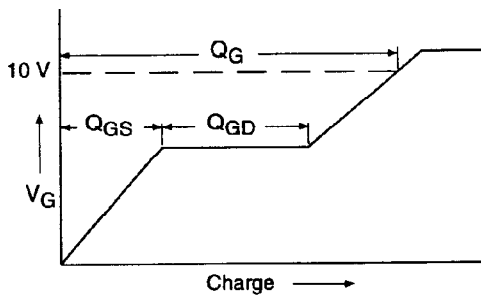


Fig 13a. Basic Gate Charge Waveform

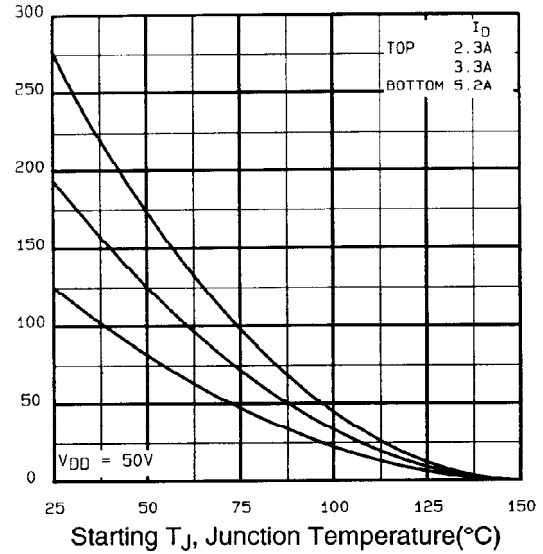


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

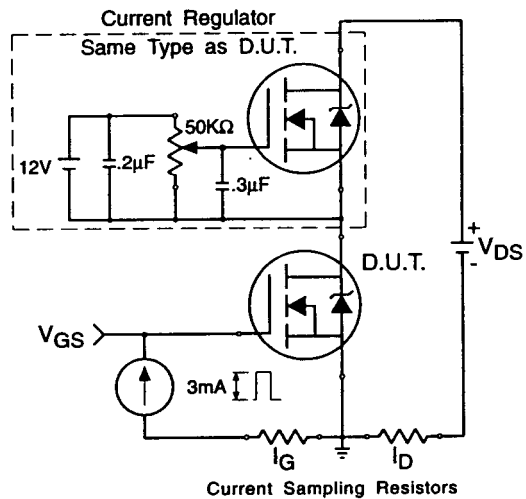
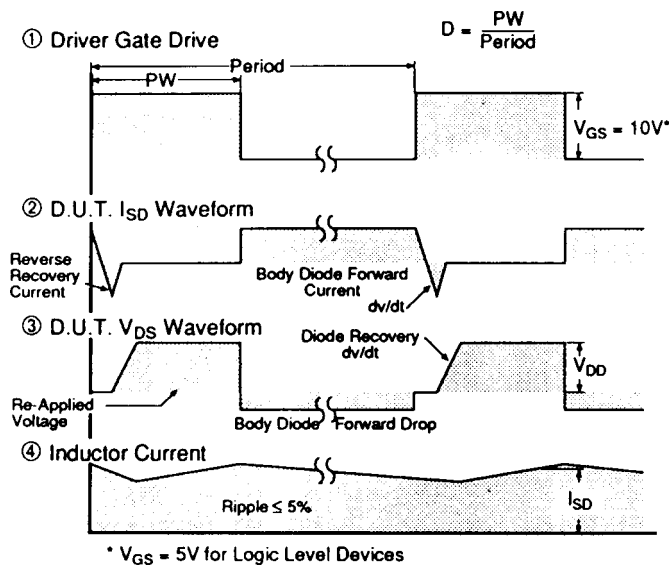
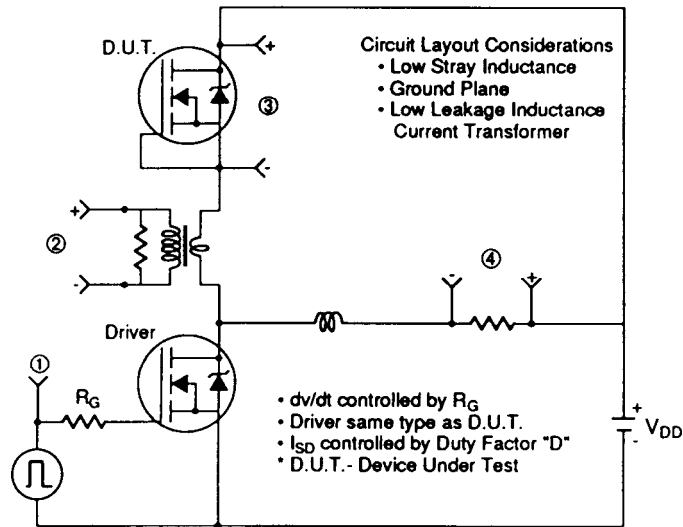
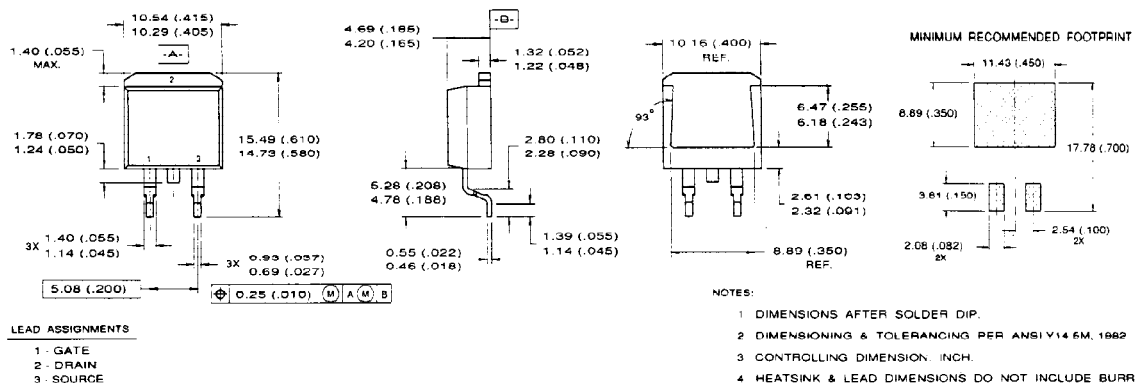


Fig 13b. Gate Charge Test Circuit

Fig 14. Peak Diode Recovery dv/dt Test Circuit

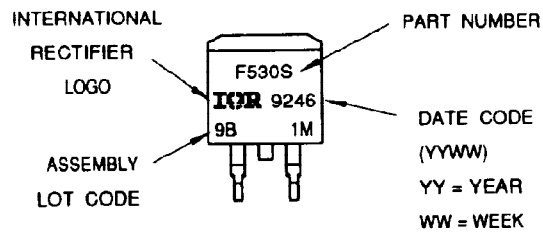


Package Outline SMD-220



Part Marking Information SMD-220

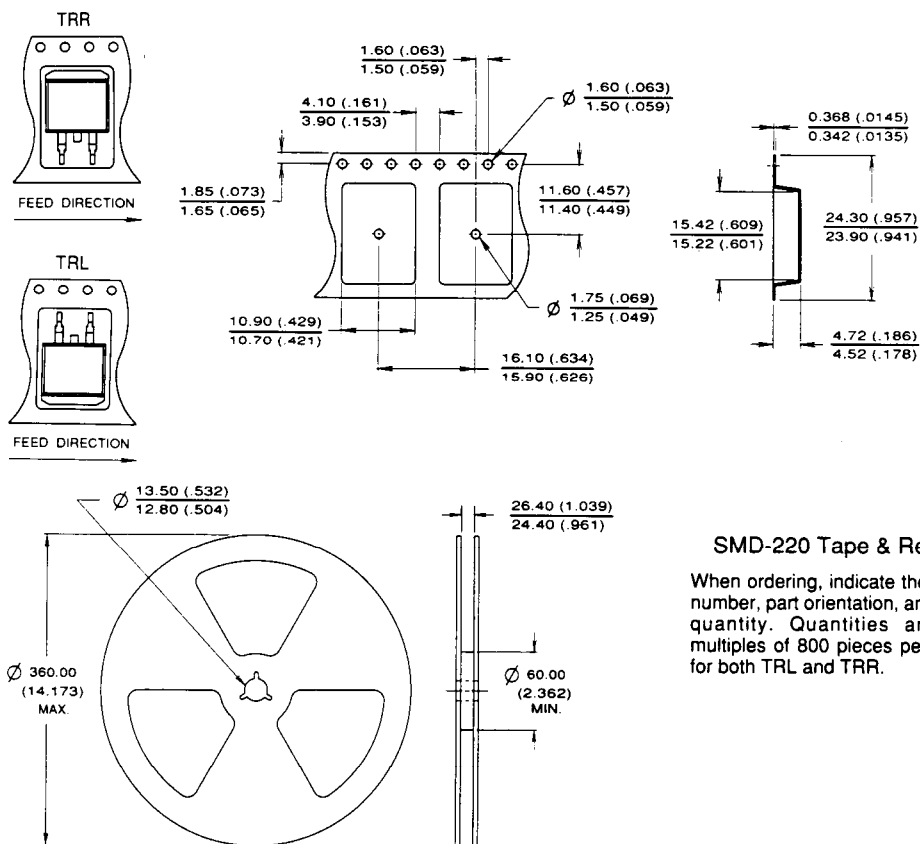
EXAMPLE: THIS IS AN IRF530S WITH
ASSEMBLY LOT CODE 9B1M





IRL620S

Package Outline SMD-220 Tape and Reel



SMD-220 Tape & Reel

When ordering, indicate the part number, part orientation, and the quantity. Quantities are in multiples of 800 pieces per reel for both TRL and TRR.

International IOR Rectifier

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Data and specifications subject to change without notice.