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REFERENCE DESIGN

IRAUDAMP4

120 W x 2 Channel Class D Audio Power Amplifier Using IRS20955 and IRF6645

By

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REFERENCE DESIGN

Introduction

The IRAUDAMP4 reference design is an example of a two-channel 120 W half-bridge Class D audio power amplifier. The reference design will demonstrate how to use the IRS20955, implement protection circuits, and design an optimum PCB layout using the IRF6645 DirectFET MOSFETs. The resulting design requires no heatsink for normal operation (one-eighth of continuous rated power). The reference design contains all the required housekeeping power supplies for ease of use. The two-channel design is scalable, for power and the number of channels.

Applications

AV receivers
Home theater systems
Mini component stereos
Sub-woofers

Features

Output Power:	120 W x two channels, Total Harmonic Distortion (THD) = 1%, 1 kHz
Residual Noise:	52 µV, IHF-A weighted, AES-17 filter
Distortion:	0.004% THD+N @ 60 W, 4 Ω
Efficiency:	96% @ 120 W, 4 Ω, single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), Over-voltage protection (OVP), Under-voltage protection (UVP), DC-protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltage	±35 V	
Load Impedance	4 Ω	
Self-Oscillating Frequency	400 kHz	No input signal
Gain Setting	26.8 dB	1 Vrms input yields rated power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS20955 gate driver, IRF6645 DirectFET MOSFET	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 25 - 35 V	
Output Power CH1-2: (1% THD+N)	120 W	1 kHz
Output Power CH1-2: (10% THD+N)	170 W	1 kHz
Rated Load Impedance	4 Ω	
Supply Current	100 mA	No input signal
Total Idle Power Consumption	7 W	No input signal
Channel Efficiency	96%	Single-channel driven, 120 W, Class D stage

Audio Performance	Typical	/ Class D*	Notes / Conditions
THD+N, 1 W THD+N, 10 W THD+N, 60 W	0.005% 0.002% 0.004%	0.002% 0.001% 0.003%	1 kHz, Single-channel driven
Dynamic Range	113 dB	120 dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 20Hz - 20 kHz BW, A-Weighted	70 µV 50 µV	40 µV 20 µV	Self-oscillating – 400 kHz Internal clock – 300 kHz
Damping Factor	170	2000	1 kHz, relative to 4 Ω load
Channel Separation	95 dB 80 dB	100 dB 85 dB	100 Hz 10 kHz
Frequency Response : 20Hz-20 kHz : 20Hz-40 kHz	±1 dB ±3 dB		1W, 4 Ω - 8 Ω Load

Thermal Performance	Typical	Notes / Conditions
Idling	T_C =30 °C T_{PCB}=37 °C	No signal input, T_A=25 °C
2ch x 15 W (1/8 rated power)	T_C =54 °C T_{PCB}=67 °C	Continuous, T_A=25 °C
2ch x 120 W (rated power)	T_C =80 °C T_{PCB}=106 °C	At OTP shutdown @ 150 s, T_A=25 °C

Physical Specifications	
Dimensions	5.8 in (L) x 5.2 in (W)

Note: Specifications are typical and not guaranteed

*Class D refers to audio performance measurements of the Class D output power stage only, with preamp and output filter bypassed.

Connection Diagram

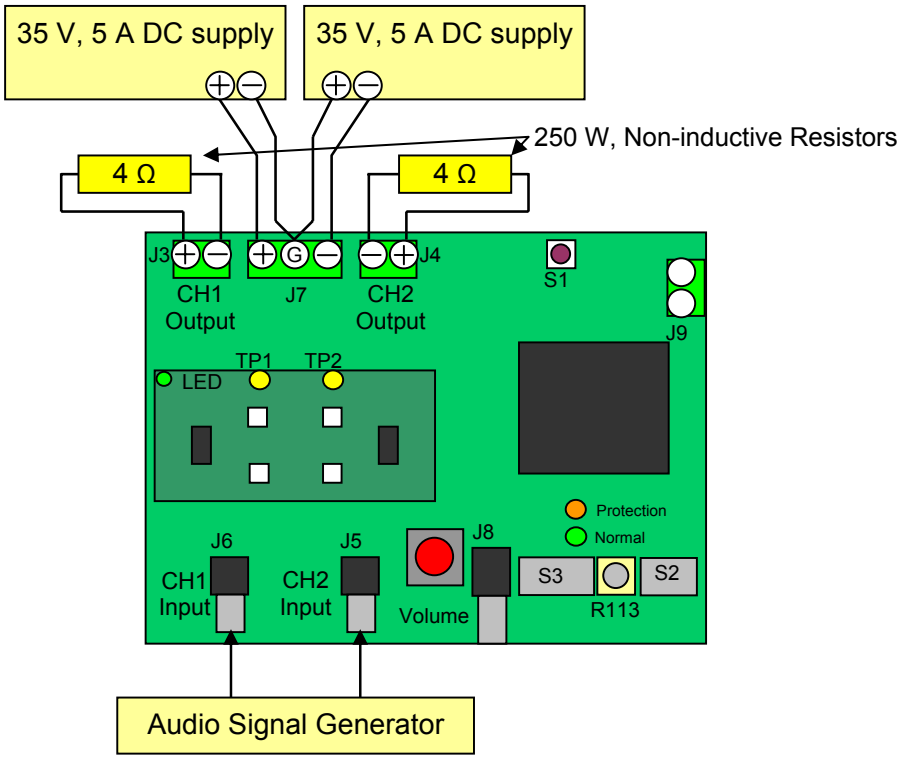


Figure 1. Typical Test Setup

Pin Description

CH1 IN	J6	Analog input for CH1
CH2 IN	J5	Analog input for CH2
POWER	J7	Positive and negative supply (+B / -B)
CH1 OUT	J3	Output for CH1
CH2 OUT	J4	Output for CH2
EXT CLK	J8	External clock sync
DCP OUT	J9	DC protection relay output

Power-on and Power-off Procedure

Always apply or remove ±35 V bus supplies at the same time.

Functional Description

Class D Operation

Referring to CH1 as an example, the op-amp U1 forms a front-end second-order integrator with C11, C13 & R25 + R29P. This integrator receives a rectangular feedback waveform from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input signal shifts the average value of this quadratic waveform (through gain relationship between R13 and R31 + R33) so that the duty varies according to the instantaneous value of the analog input signal. The IRS20955 input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where this signal is split into two signals, with opposite polarity and added deadtime, for high-side and low-side MOSFET gate signals, respectively. The IRS20955 drives two IRF6645 DirectFET MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L1 and C23, which filters out the Class D switching carrier signal.

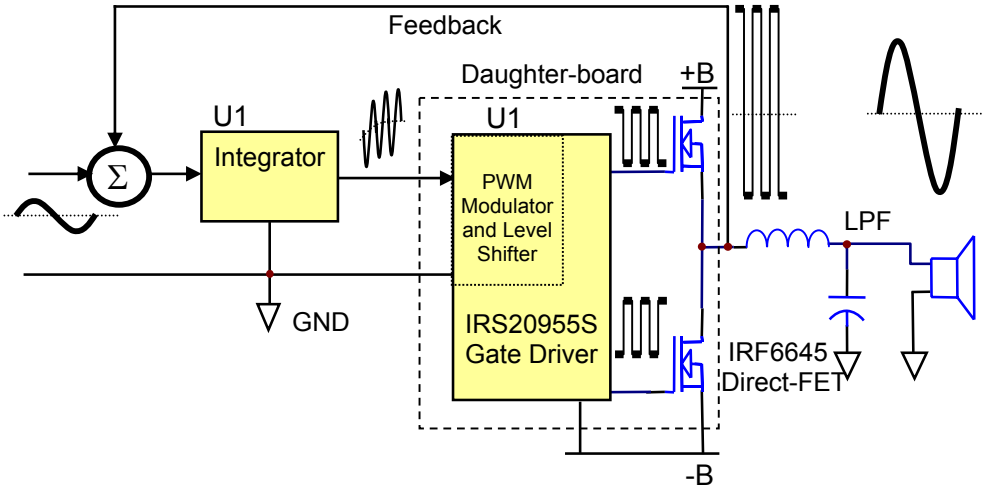


Figure 2. Simplified Block Diagram of Class D Amplifier

Power Supplies

The IRAUDAMP4 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±25 V to ±35 V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5 V supply for analog signal processing (preamp, etc.), while a +12 V supply (V_{CC}), referenced to –B, is included to supply the Class D gate-driver stage.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C31 and C32 on the motherboard, along with high-frequency bypass-caps C15-C18 on daughter board, address the high-frequency ripple current that result from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, having enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP4 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP4 is excellent (Figure 3).

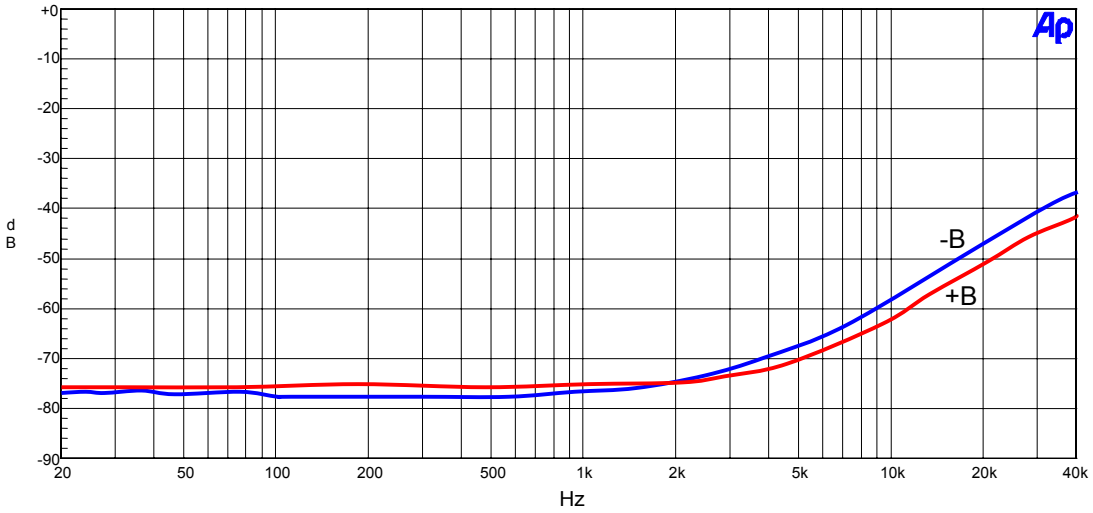


Figure 3. Power Supply Rejection Ratio (PSRR) for Negative (-B) and Positive (+B) Supplies

Bus Pumping

Since the IRAUDAMP4 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

These conditions worsen bus pumping:

– Lower frequencies (bus-pumping duration is longer per half cycle)
– Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
– Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP4 has protection features that will shutdown the switching operation if the bus voltage becomes too high (>40 V) or too low (<20 V). One of the easiest countermeasures is to drive both of the channels out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the –B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

Input

A proper input signal is an analog signal below 20 kHz, up to ±3.5 V peak, having a source impedance of less than 600 Ω. A 30 kHz to 60 kHz input signal can cause LC resonance in the output LPF, resulting in an abnormally large amount of reactive current flowing through the switching stage (especially at 8 Ω or higher impedance towards open load), causing OCP activation. The IRAUDAMP4 has an RC network, or Zobel network, to damp the resonance and protect the board in such event, but is not thermally rated to handle continuous supersonic frequencies. *These supersonic input frequencies therefore should be avoided.* Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.

Output

Both outputs for the IRAUDAMP4 are single-ended and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for a 4 Ω speaker load for a maximum output power of 120 W, but is capable of operating with higher load impedances (at reduced power), at which point the frequency response will have a small peak at the corner frequency of the output LC low pass filter. The IRAUDAMP4 is stable with capacitive-loading; however, it should be realized that the frequency response degrades with heavy capacitive loading of more than 0.1 µF.

Gain Setting / Volume Control

The IRAUDAMP4 has an internal volume control (potentiometer R108 labeled, "VOLUME") for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_1). The maximum volume setting (clockwise rotation) corresponds to a total gain of +37.9 dB (78.8 V/V). The total gain is a product of the power-stage gain, which is constant (+23.2 dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB. For best performance in testing, the internal volume control should be set to a gain of 21.9 V/V, or 1 Vrms input will result in rated output power (120 W into 4 Ω), allowing for a >11 dB overdrive.

Output Filter Design, Preamplifier and Performance

The audio performance of the IRAUDAMP4 depends on a number of different factors. The section entitled, "Typical Performance" presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the Class D power stage, they have a significant effect on the overall performance.

Output filter

Since the output filter is not included in the control loop of the IRAUDAMP4, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is there important to understand what characteristics are preferable when designing the output filter:

1) The DC resistance of the inductor should me minimized to 20 mΩ or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

Preamplifier

The preamp allows partial gain of the input signal, and in the IRAUDAMP4, controls the volume. The preamp itself will add distortion and noise to the input signal, resulting in a gain through the Class D output stage and appearing at the output. Even a few micro-volts of noise can add significantly to the output noise of the overall amplifier. In fact, the output noise from the preamp contributes more than half of the overall noise to the system.

It is possible to evaluate the performance without the preamp and volume control, by moving resistors R13 and R14 to R71 and R72, respectively. This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the selection of preamp and/or output filter, will improve the overall system performance to approach that of the stand-alone Class D power stage. In the "Typical

Performance" section, only limited data for the stand-alone Class D power stage is given. For example, results for THD+N vs. Output Power are provided, utilizing a range of different inductors. By changing the inductor and repeating this test, a designer can quickly evaluate a particular inductor.

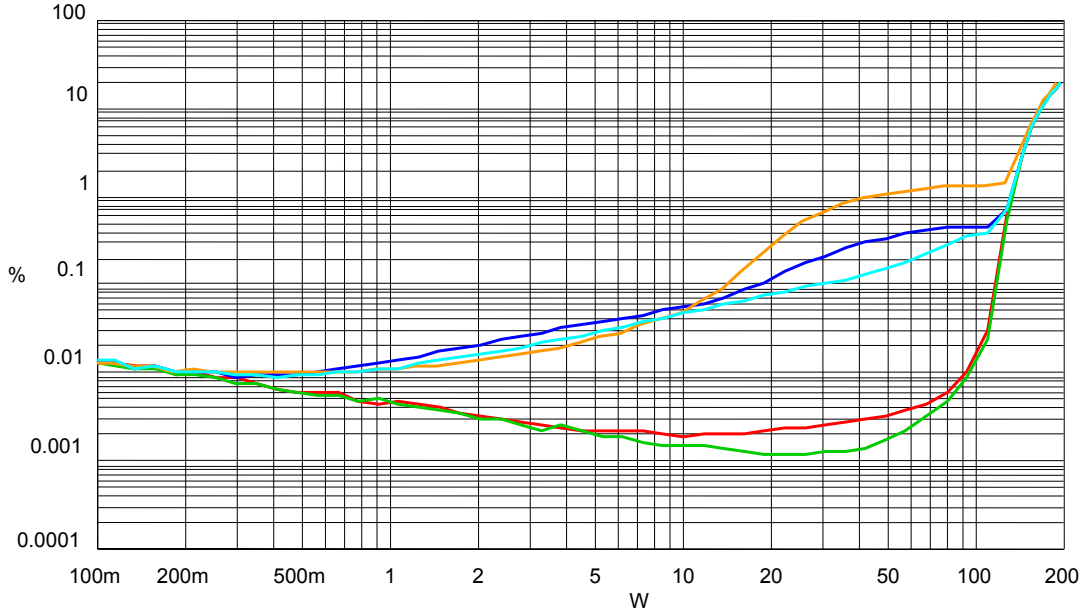


Figure 4. Results of THD+N vs. Output Power with Different Output Inductors

Self-Oscillating PWM Modulator

The IRAUDAMP4 Class D audio power amplifier features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, the IRS20955 gate-driver propagation delay, the IRF6645 switching speed, the time-constant of front-end integrator (e.g. R25 + R29P, C11 and C13 for CH1) and variations in the supply voltages are critical factors of the self-oscillating frequency. Under nominal conditions, the switching-frequency is around 400 kHz with no audio input signal and a +/-35 V supply.

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately,

or have them separated by at least 25 kHz. With the installed components, it is possible to change the self-oscillating frequency from about 160 kHz up to 600 kHz.

Potentiometers for adjusting self-oscillating frequency	
R29P	Switching frequency for CH1*
R30P	Switching frequency for CH2*
*Adjustments have to be done at an idling condition with no signal input.	

Switches and Indicators

There are three different indicators on the reference design:

- An orange LED, signifying a fault / shutdown condition when lit.
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present.
- A green LED on the daughter board, signifying there is power.

There are three switches on the reference design:

- Switch S1 is a trip and reset push-button. Pushing this button has the same effect of a fault condition. The circuit will restart about three seconds after the shutdown button is released.
- Switch S2 is an internal clock-sync frequency selector. This feature allows the designer to modify the switching frequency in order to avoid AM radio interference. With S3 is set to INT, the two settings “H” and “L” will modify the internal clock frequency by about 20 kHz to 40 kHz, either higher “H” or lower “L.” The actual internal frequency is set by potentiometer R113 - “INT FREQ.”
- Switch S3 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.

Switching Frequency Lock / Synchronization Feature

For single-channel operation, the use of the self-oscillating switching scheme will yield the best audio performance. The self-oscillating frequency, however, does change with the duty ratio. This varying frequency can interfere with AM radio broadcasts, where a constant-switching frequency with its harmonics shifted away from the AM carrier frequency, is preferred. In addition to AM broadcasts, multiple channels can also reduce audio performance at low power, and can lead to increased residual noise. Clock frequency locking/synchronization can address these unwanted characteristics.

Please note that the switching frequency lock / synchronization feature is not possible for all frequencies and duty ratios, and operates within a limited frequency and duty-ratio range around the self-oscillating frequency (Figure 5).

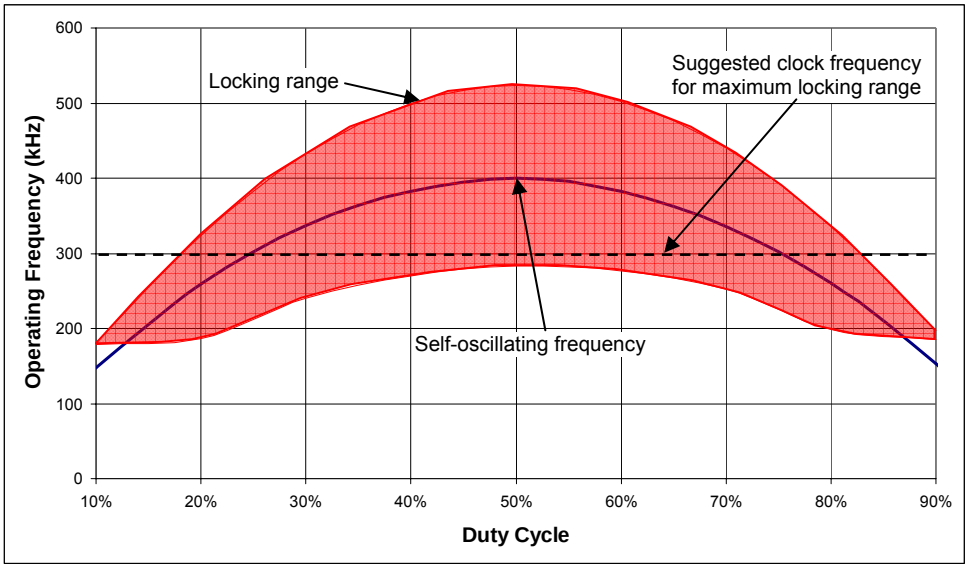


Figure 5. Typical Lock Frequency Range vs. PWM Duty Ratio
(Self-oscillating frequency set to 400 kHz with no input)

As illustrated by the THD+N Ratio vs. Output Power results (Figure 6) , the noise levels increase slightly when all channels are driven (ACD) with the self oscillator, especially below the 5 W range. Residual noise typically increases by a third or more (see "Specifications – Audio Performance") compared to a single-channel driven (SCD) configuration. Locking the oscillator frequency results in lowering the residual noise to that of a single-channel-driven system. The output power range, for which the frequency-locking is successful, depends on what the locking frequency is with respect to the self-oscillating frequency. As illustrated in Figure 6, the locking frequency is lowered (from 450 kHz to 400 kHz to 350 kHz and then 300 kHz) as the output power range (where locking is achieved) is extended. Once locking is lost, however, the audio performance degrades, but the increase in THD seems independent from the clock frequency. Therefore, a 300 kHz clock frequency is recommended.

It is possible to improve the THD performance by increasing the corner frequency of the high pass filter (HPF) (R17 and C15 for Ch1) that is used to inject the clock signal. This drop in THD, however, comes at the cost of reducing the locking range. Resistor values of up to 100 kΩ and capacitor values down to 10 pF can be used.

In the IRAUDAMP4, this switching frequency lock/synchronization feature is achieved with either an internal or external clock input (selectable through S3). If an internal (INT) clock is selected, an internally-generated clock signal will be used, adjusted by setting potentiometer R113 "INT FREQ." If external (EXT) clock signal is selected, a 0 V to 5 V square-wave (~50% duty ratio) logic signal must be applied to BNC connector J17.

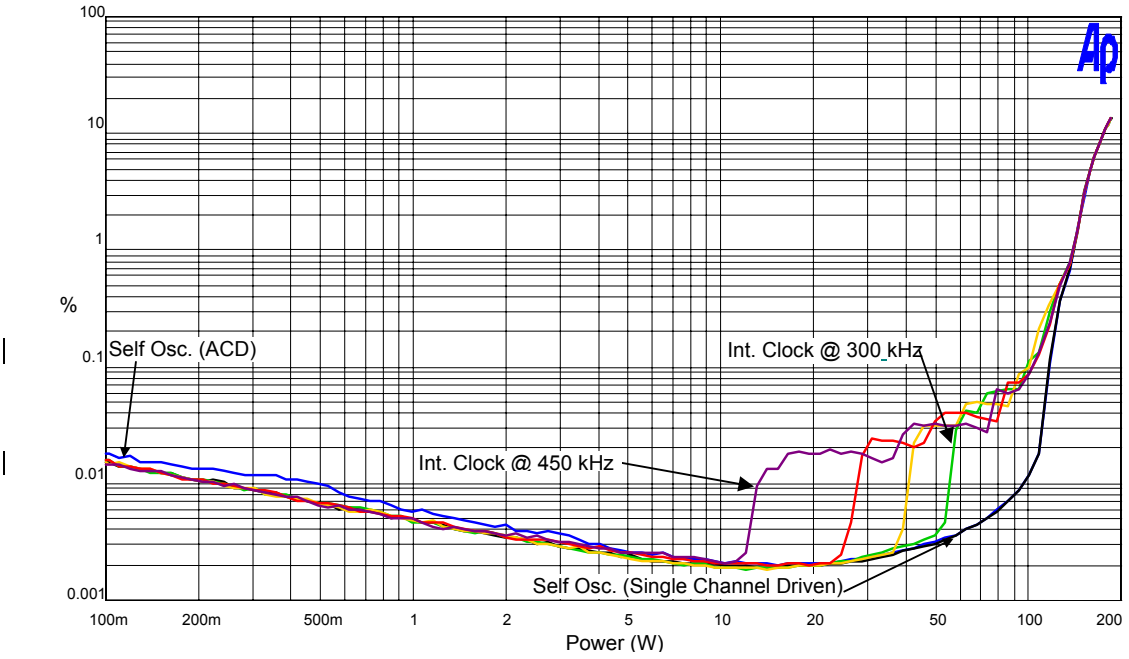


Figure 6. THD+N Ratio vs. Output Power for Different Switching Frequency Lock/Synchronization Conditions

IRS20955 Gate Driver IC

The IRAUDAMP4 uses the IRS20955, which is a high-voltage (up to 200 V), high-speed power MOSFET gate driver with internal deadtime and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. A bi-directional current protection feature that protects both the high-side and low-side MOSFETs are internal to the IRS20955, and the trip levels for both MOSFETs can be set independently. In this design, the deadtime can be selected for optimized performance, by minimizing deadtime while limiting shoot-through. As a result, there is no gate-timing adjustment on the board. Selectable deadtime through the DT pin voltage is an easy and reliable function which requires only two external resistors, R11 and R9.

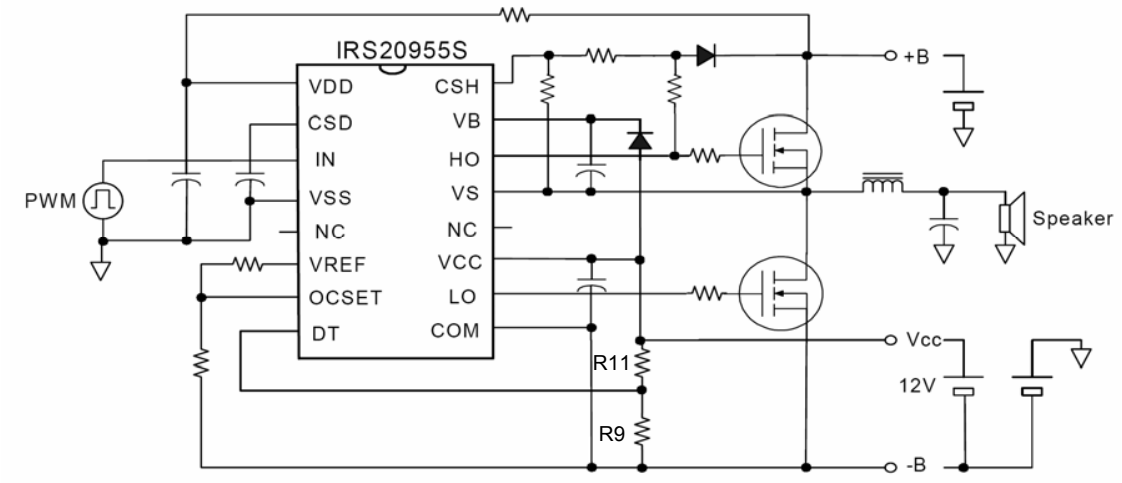


Figure 7. System-level View of Gate Driver IRS20955

Selectable Deadtime

The IRS20955 determines its deadtime based on the voltage applied to the DT pin. An internal comparator translates which pre-determined deadtime is being used by comparing the DT voltage with internal reference voltages. A resistive voltage divider from V_{CC} sets threshold voltages for each setting, negating the need for a precise absolute voltage to set the mode. The threshold voltages between deadtime settings are set internally, based on different ratios of V_{CC} as indicated in the diagram below. In order to avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5 mA is suggested for the external resistor divider circuit. Suggested values of resistance that are used to set a deadtime are given below. Resistors with up to 5% tolerance can be used.

Deadtime mode	Deadtime	R11	R9	DT Voltage
DT1	~15 ns	<10kΩ	Open	V_{CC}
DT2	~25 ns	5.6kΩ	4.7kΩ	0.46(V_{CC})
DT3	~35 ns	8.2kΩ	3.3kΩ	0.29(V_{CC})
DT4	~45 ns	Open	<10kΩ	COM

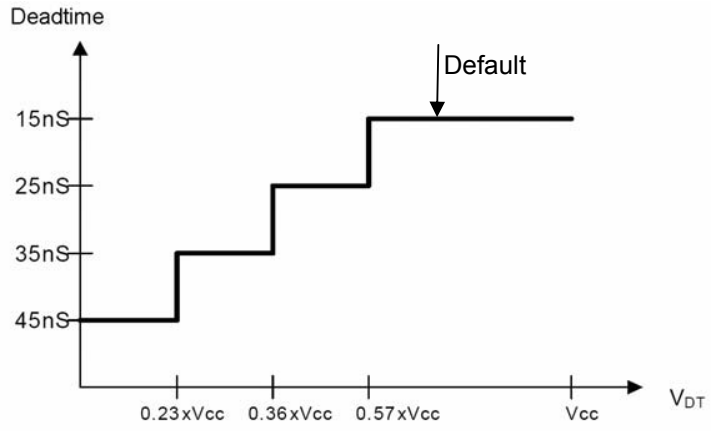


Figure 8. Deadtime Settings vs. V_{DT} Voltage

Over-Current Protection (OCP)

In the IRAUDAMP4, the IRS20955 gate driver accomplishes OCP internally, a feature discussed in greater detail in the “Protection” section.

Offset Null (DC Offset)

The IRAUDAMP4 is designed such that no output-offset nullification is required. DC offsets are tested to be less than ±5 mV.

Bridged Output

The IRAUDAMP4 is not intended for BTL operation. However, BTL operation can be achieved by feeding out-of-phase audio input signals to the two input channels. In BTL operation, minimum load impedance is 8 Ω and rated power is 240 W non-clipping. The installed clamping diodes D5 – D8 are required for BTL operation, since reactive energy flowing from one output to the other during clipping can force the output voltage beyond the voltage supply rails if not clamped.

Startup and Shutdown

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered “click noise”, although in some cases, it can be louder than the click noise of non-relay-based solutions.

The IRAUDAMP4 does not use any series relay to disconnect the speaker from the audible transient noise, but rather a shunt-based click noise reduction circuit that yields audible noise levels that are far less that those generated by the relays they replace. This results in a more reliable, superior performance system.

For the startup and shutdown procedures, the activation (and deactivation) of the click-noise reduction circuit, the Class D power stage and the audio input (mute) controls have to be sequenced correctly to achieve the required click noise reduction. The overall startup sequencing, shutdown sequencing and shunt circuit operation are described below.

Click-Noise Reduction Circuit (Solid-State Shunt)

To reduce the turn-on and turn-off click noise, a low impedance shunting circuit is used to minimize the voltage across the speaker during transients. For this purpose, the shunting circuit must include the following characteristics:

1) An impedance significantly lower than that of the speaker being shunted. In this case, the shunt impedance is ~100 mΩ, compared to the nominal 4 Ω speaker impedance.
2) When deactivated, the shunting circuit must be able to block voltage in both directions due to the bi-directional nature of the audio output.
3) The shunt circuit requires some form of OCP. If one of the Class D output MOSFETs fails, or is conducting when the speaker mute (SP MUTE) is activated, the shunting circuit will effectively try to short one of the two supplies (+/-B).

The implemented click-noise reduction circuit is shown in Figure 9. Before startup or shutdown of the Class D power stage, the click-noise reduction circuit is activated through the SP MUTE control signal. With SP MUTE signal high, the speaker output is shorted through the back-to-back MOSFETs (U9 for Channel 1) with an equivalent on resistance of about 100 mΩ. The two transistors (U7 for Channel 1) are for the OCP circuit.

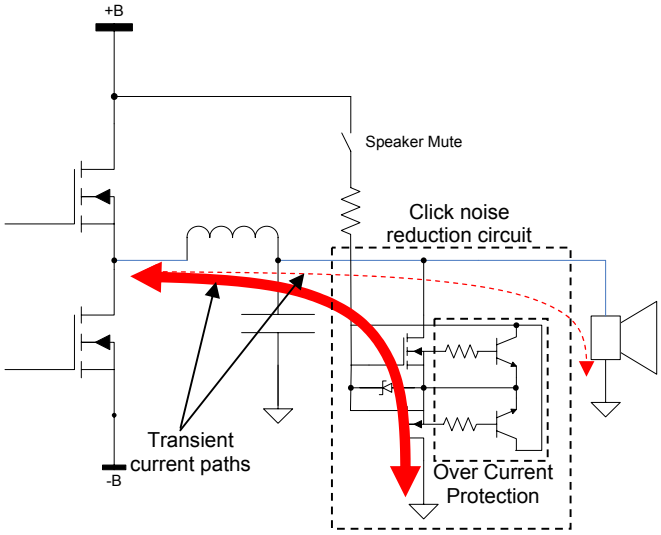


Figure 9. Class D Output Stage with Click-Noise Reduction Circuit

Startup and Shutdown Sequencing

The IRAUDAMP4 sequencing is achieved through the charging and discharging of the CStart capacitor C117. This, coupled to the charging and discharging of the voltage of CSD (C3 on daughter board for CH1) of the IRS20955, is all that is required for complete sequencing. The conceptual startup and shutdown timing diagrams are show in Figure 10.

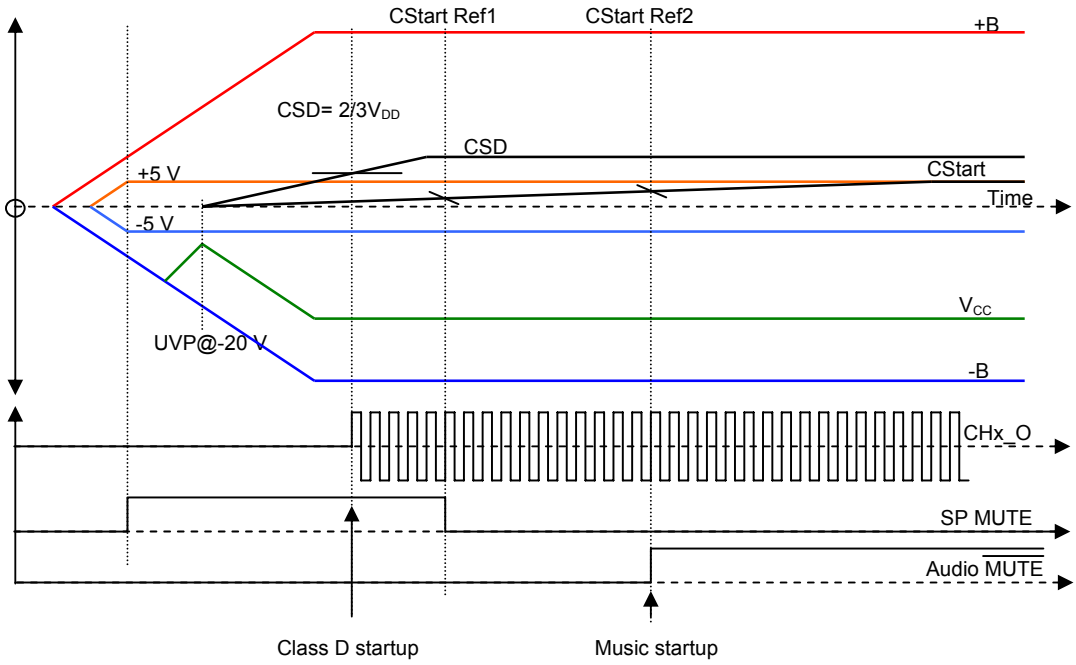


Figure 10. Conceptual Startup Sequencing of Power Supplies and Audio Section Timing

For startup sequencing, +/-B supplies startup at different intervals. As +/-B supplies reach +5 V and -5 V respectively, the analog supplies (+/-5 V) start charging and, once +B reaches ~16 V, V_{CC} charges. Once –B reaches -20 V, the UVP is released and CSD and CStart start charging. Once +/-5 V is established, the click-noise reduction circuit is activated through the SP MUTE control signal. As CSD reaches two-thirds V_{DD}, the Class D stage starts oscillating. Once the startup transient has passed, SP MUTE is released (CStart reaches Ref1). The Class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

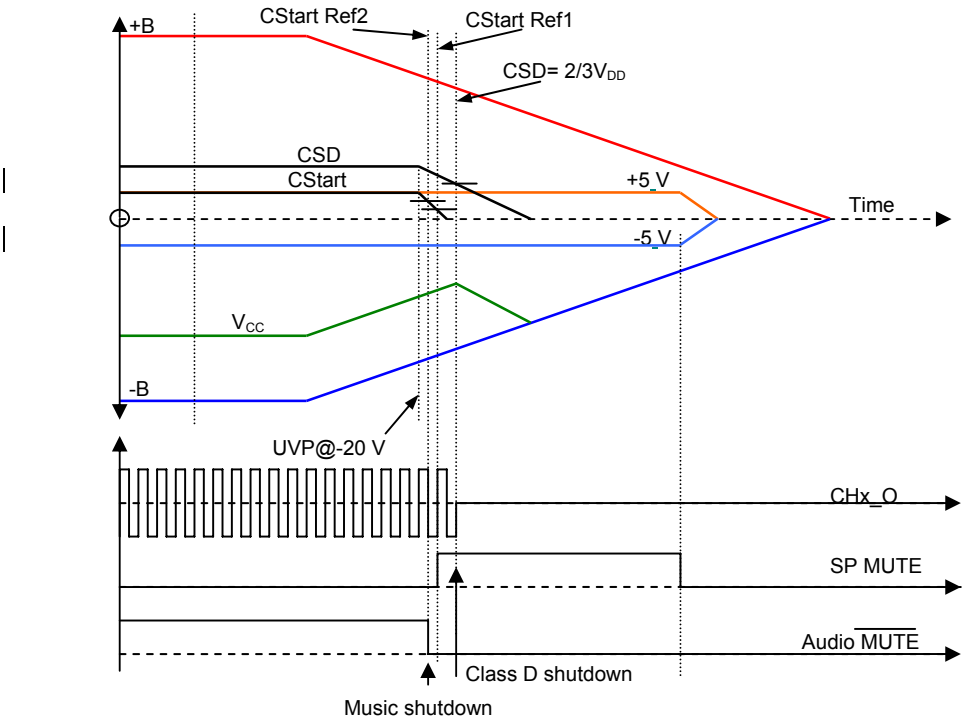


Figure 11. Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS20955 trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once CStart reaches threshold Ref1, the click-noise reduction circuit is activated (SP MUTE). It is then possible to shutdown the Class D stage (CSD reaches two-thirds V_{DD}). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

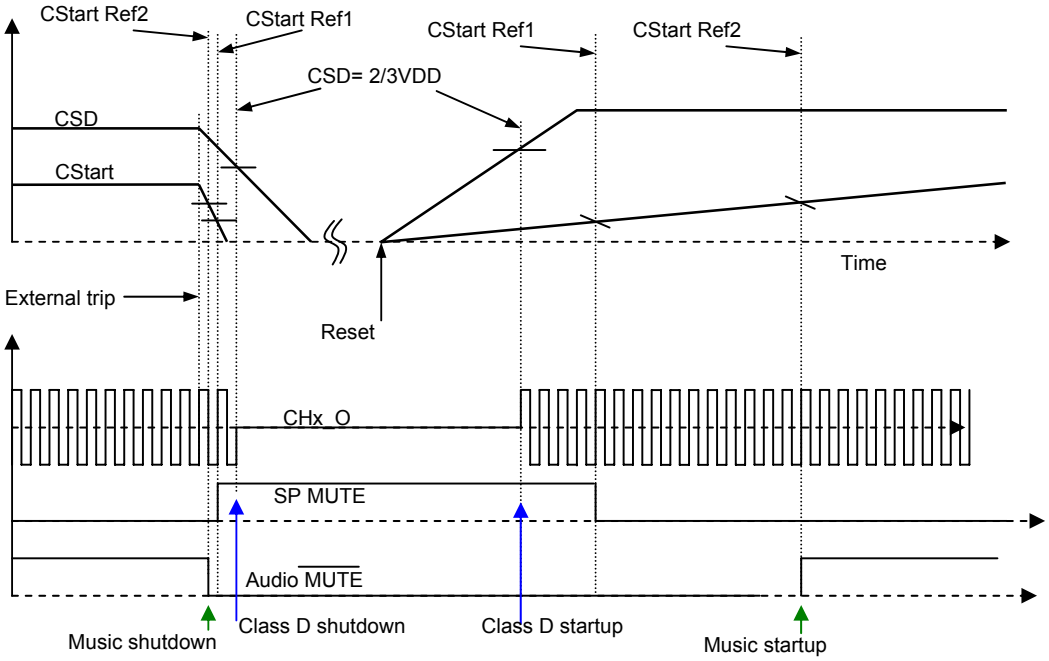


Figure 12. Conceptual Click Noise Reduction Sequencing at Trip and Reset

Protection

The IRAUDAMP4 has a number of protection circuits to safeguard the system and speaker during operation, which fall into one of two categories, internal faults and external faults, and distinguished by the manner in which a fault condition is treated. Internal faults are only relevant to the particular channel, while external faults affect the whole board. For internal faults, only the offending channel is stopped. The channel will hiccup until the fault is cleared. For external faults, the whole board is stopped using the shutdown sequencing described earlier. Here, the system will also hiccup until the fault is cleared at which time it will restart according to the startup sequencing described earlier.

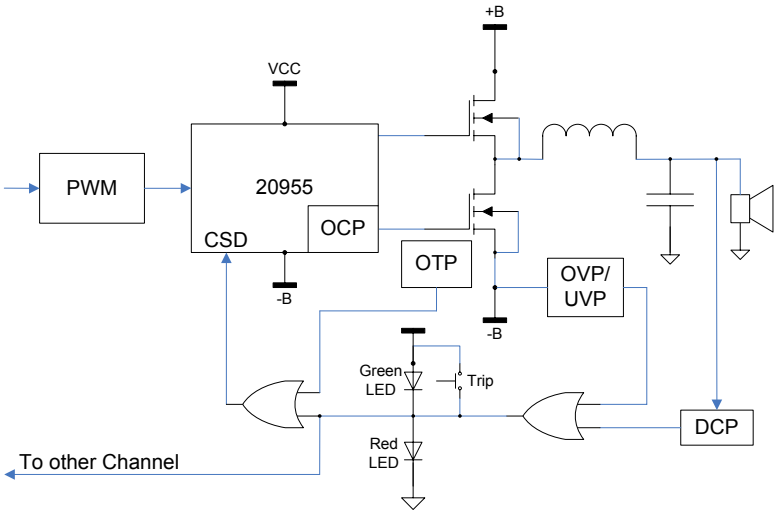


Figure 13. Functional Block Diagram of Protection Circuit Implementation

Internal Faults

OCP and OTP are considered internal faults. These internal faults will only shutdown the particular channel by pulling low the relevant CSD pin. The channel will shutdown for about one-half a second and will hiccup until the fault is cleared.

Over-Temperature Protection (OTP)

A separate PTC resistor is placed in close proximity to the high-side IRF6645 DirectFET MOSFET for each of the amplifier channels. If the resistor temperature rises above 100 °C, the OTP is activated. The OTP protection will only shutdown the relevant channel by pulling low the CSD pin and will recover once the temperature at the PTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100 °C. This setting is limited by the PCB material and not by the operating range of the MOSFET.

Over-Current Protection (OCP)

The OCP internal to the IRS20955 shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the IRS20955 datasheet. Here is a brief description:

Low-Side Current Sensing

The low-side MOSFET is protected from an overload condition and will shutdown the switching operation if the load current exceeds a preset trip level. The low-side current sensing is based on measurement of MOSFET drain-to-source voltage during the low-side MOSFET on state. The voltage set on the OCSET pin programs the threshold for low-side over-current sensing. Thus, if the V_S voltage (during low-side conduction) is higher than the OCSET voltage, the IRS20955 will trip. It is recommended to use VREF to supply a reference voltage to a resistive divider (R5 and R7 for CH1) generating a voltage to OCSET for better variability against V_{CC} fluctuations. For IRAUDAMP4, the low-side over-current trip level is set to 0.65 V. For the IRF6645 DirectFET MOSFETs with a nominal R_{DS-ON} of 28 mΩ at 25 °C, this results in a ~23 A maximum trip level. Since the R_{DS-ON} is a function of temperature, the trip level is reduced to ~15 A at 100 °C.

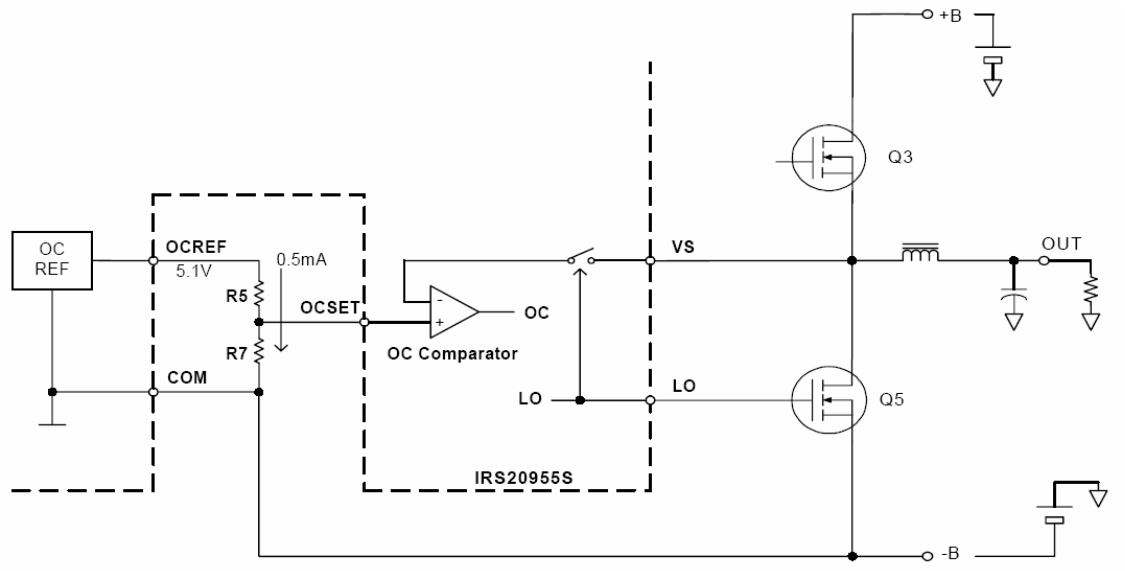


Figure 14. Simplified Functional Block Diagram of Low-Side Current Sensing (CH1)

High-Side Current Sensing

The high-side MOSFET is protected from an overload condition and will shutdown the switching operation if the load current exceeds a preset trip level. High-side over-current sensing monitors detect an overload condition by measuring drain-to-source voltage (V_{DS}) through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to engage OC protection is internally fixed at 1.2 V. An external resistive divider R23 and R25 (for Ch1) can be used to program a higher threshold. An additional external reverse blocking diode (D5 for Ch1) is required to block high-voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6 V at D5, the minimum threshold which can be set in the high-side is 0.6 V across the drain-to-source. For IRAUDAMP4, the high-side over-current trip level is set to 0.6 V across the high-side MOSFET. For the IRF6645 MOSFETs with a nominal R_{DS-ON} of 28 mΩ at 25 °C, this results in a ~21 A maximum trip level. Since the R_{DS-ON} is a function of temperature, the trip level is reduced to ~14 A at 100 °C.

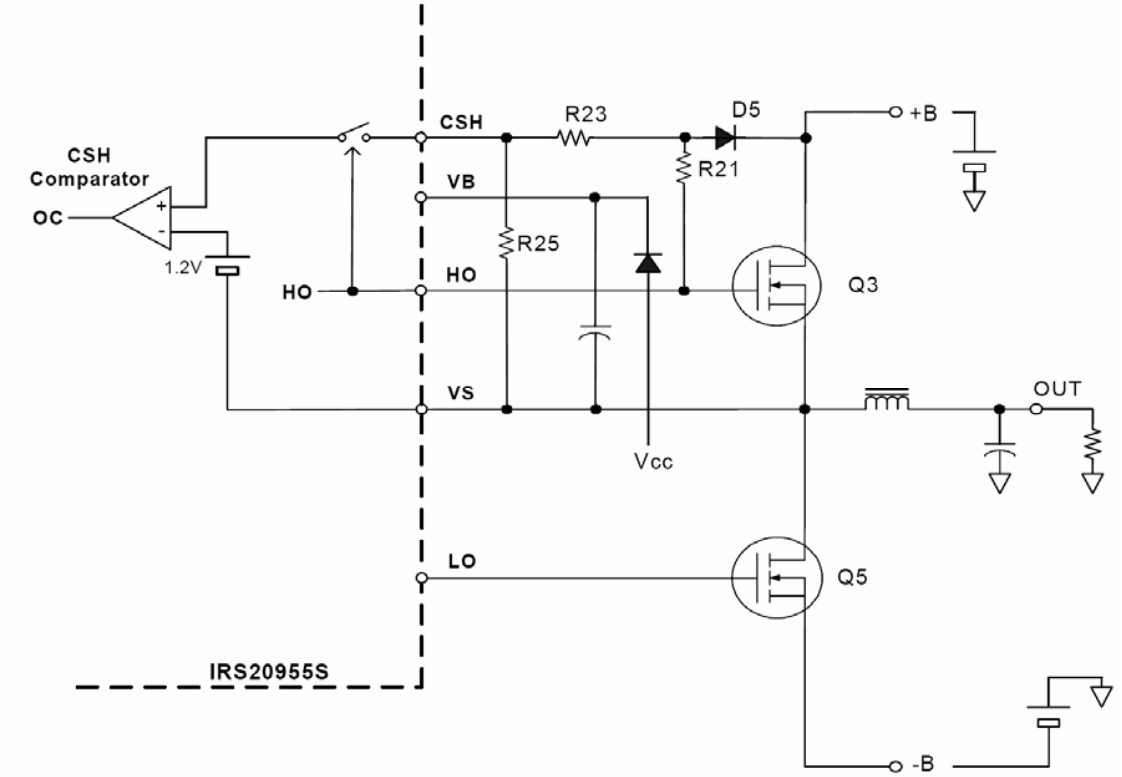


Figure 15. Simplified Functional Block Diagram of High-Side Current Sensing (CH1)

For a complete description of calculating and designing the over-current trip limits, please refer to the IRS20955 datasheet.

External Faults

OVP, UVP and DCP are considered external faults. In the event that any external fault condition is detected, the shutdown circuit will activate for about three seconds, during which time the orange “Protection” LED will turn on. If the fault condition has not cleared, the protection circuit will hiccup until fault is removed. Once the fault is cleared, the green “Normal” LED will turn on. There is no manual reset option.

Over-Voltage Protection (OVP)

OVP will shutdown the amplifier if the bus voltage between GND and -B exceeds 40 V. The threshold is determined by the voltages sum of the Zener diode Z105, R140, and V_{BE} of Q109. As a result, it protects the board from bus pumping at very low audio signal frequencies by shutting down the amplifier. OVP will automatically reset after three seconds. Since the +B and –B supplies are assumed to be symmetrical (bus pumping, although asymmetrical in time, will pump the bus symmetrically in voltage level). It is sufficient to sense one of the two supply voltages only for OVP. *It is therefore up to the user to ensure that the power supplies are symmetrical.*

Under-Voltage Protection (UVP)

UVP will shutdown the amplifier if the bus voltage between GND and -B falls below 20 V. The threshold is determined by the voltages sum of the Zener diode Z107, R145 and V_{BE} of Q110. Same as OVP, UVP will automatically reset after three seconds and only one of the two supply voltages is monitored.

Speaker DC-Voltage Protection (DCP)

DCP is provided to protect against DC current flowing into the speakers. This abnormal condition is rare and is likely caused when the power amplifier fails and one of the high-side or low-side IRF6645 DirectFET MOSFETs remain in the ON state. DCP is activated if either of the outputs has more than ±4 V DC offset (typical). Under this fault condition, it is normally required to shutdown the feeding power supplies. Since these are external to the reference design board, an isolated relay is provided (P1) for further systematic evaluation of DC-voltage protection to transmit this condition to the power supply controller and is accessible through connector J9 (pins of J9 are shorted during fault condition).

Thermal Considerations

The daughter board design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. Without the addition of a heatsink or forced air-cooling, the daughter board cannot handle continuous rated power.

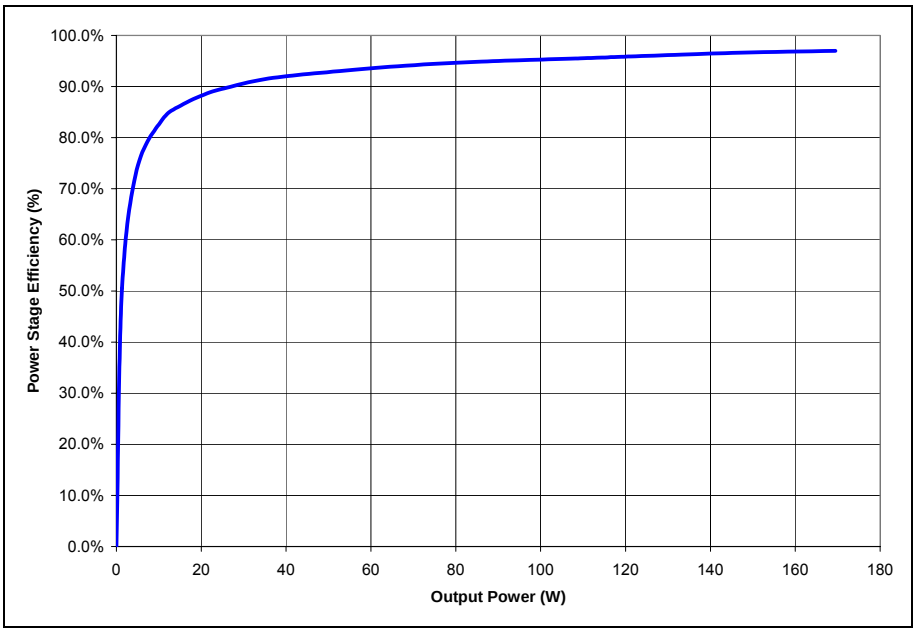


Figure 16. Efficiency FV. Output Power, 4 Ω Single Channel Driven, ±B supply = ±35 V, 1 kHz Audio Signal

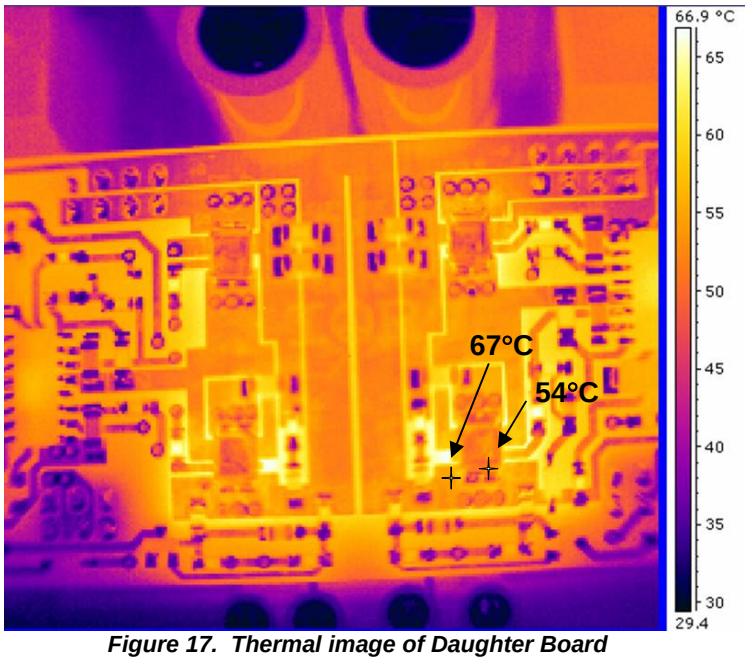
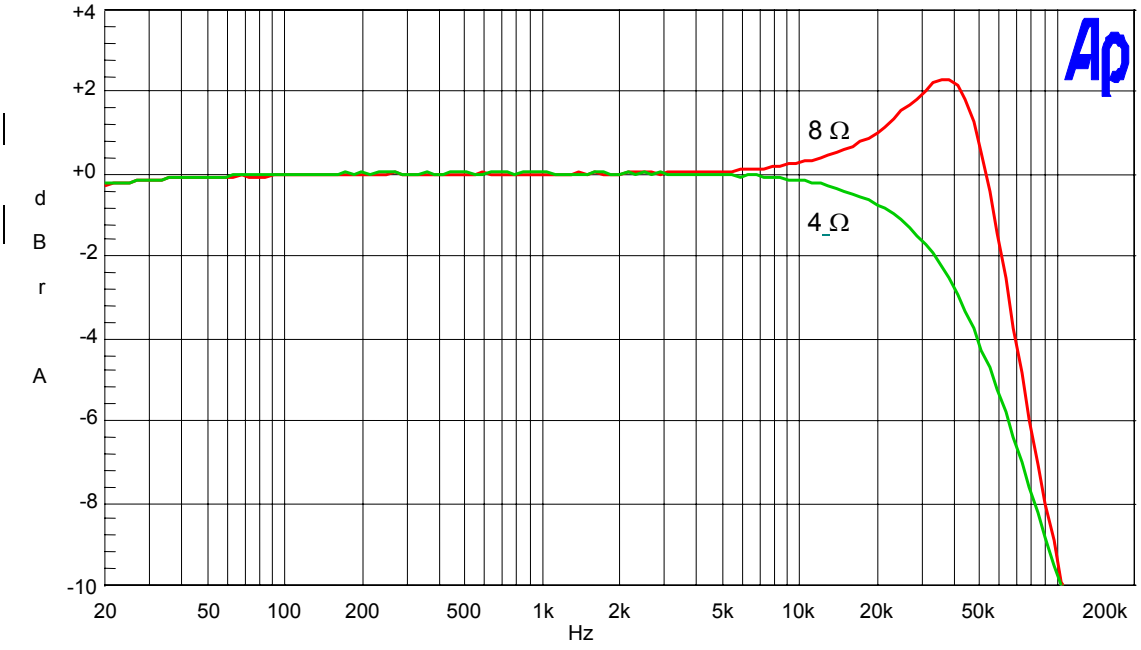


Figure 17. Thermal image of Daughter Board
Two-Channel x 1/8th Rated Power (15 W) in Operation, T_C = 54 °C at Steady State
±B supply = ±35 V, 4 Ω Load, 1 kHz audio signal, T_A = 25 °C

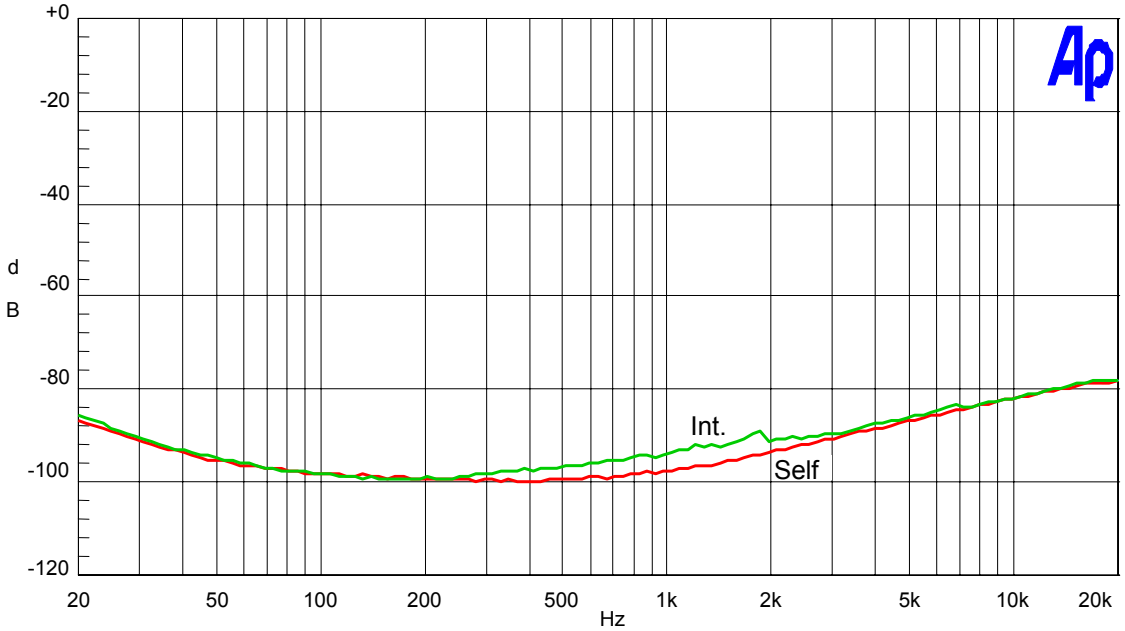
Typical Performance

±B supply = ± 35 V, load impedance = 4 Ω, 1 kHz audio signal,
Self oscillator @ 400 kHz and internal volume-control set to give required output with 1 Vrms input signal, unless otherwise noted.



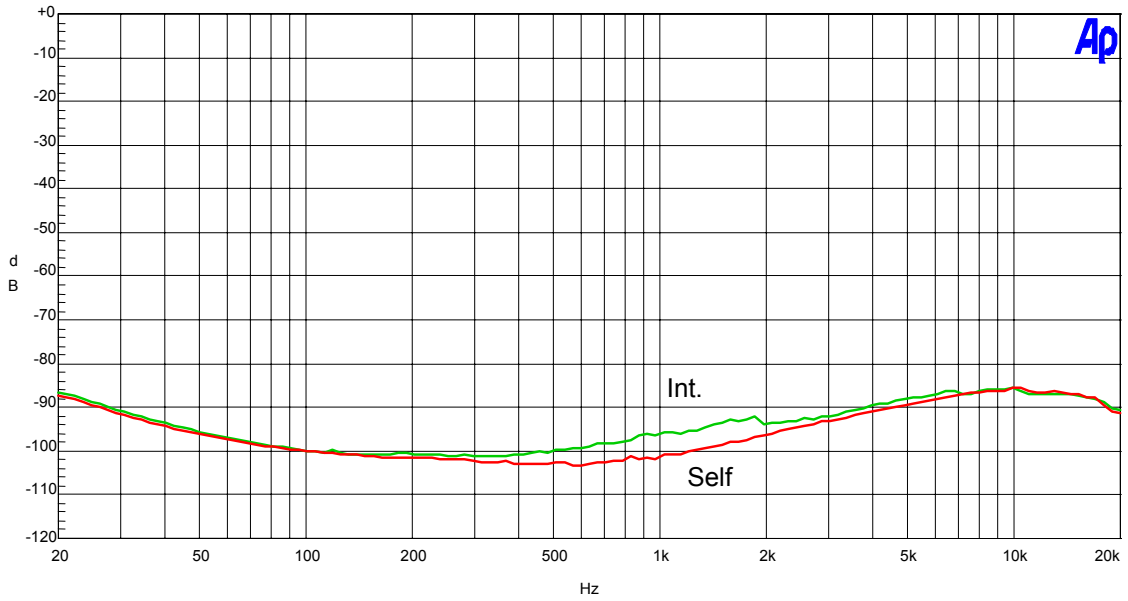
Green	CH1 - 4 Ω, 2 V Output
Red	CH1 - 8 Ω, 2 V Output

Figure 18. Frequency Characteristics vs. Load Impedance



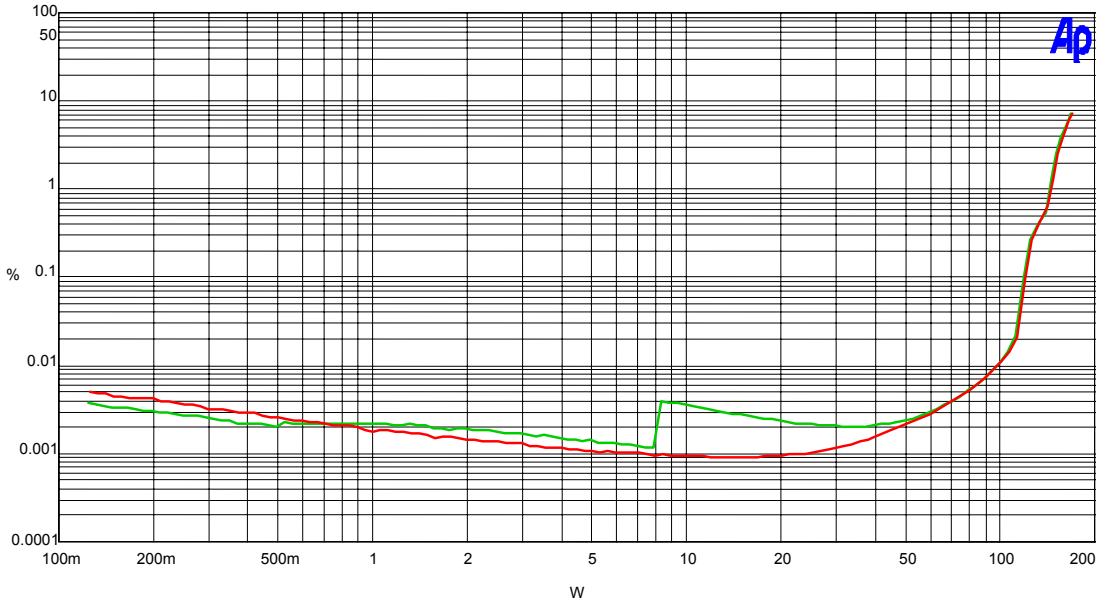
Red	CH2 – CH1, 60 W, Self Oscillator @ 400 kHz
Green	CH2 – CH1, 60 W, Internal Clock @ 300 kHz

Figure 19. Channel Separation vs. Frequency



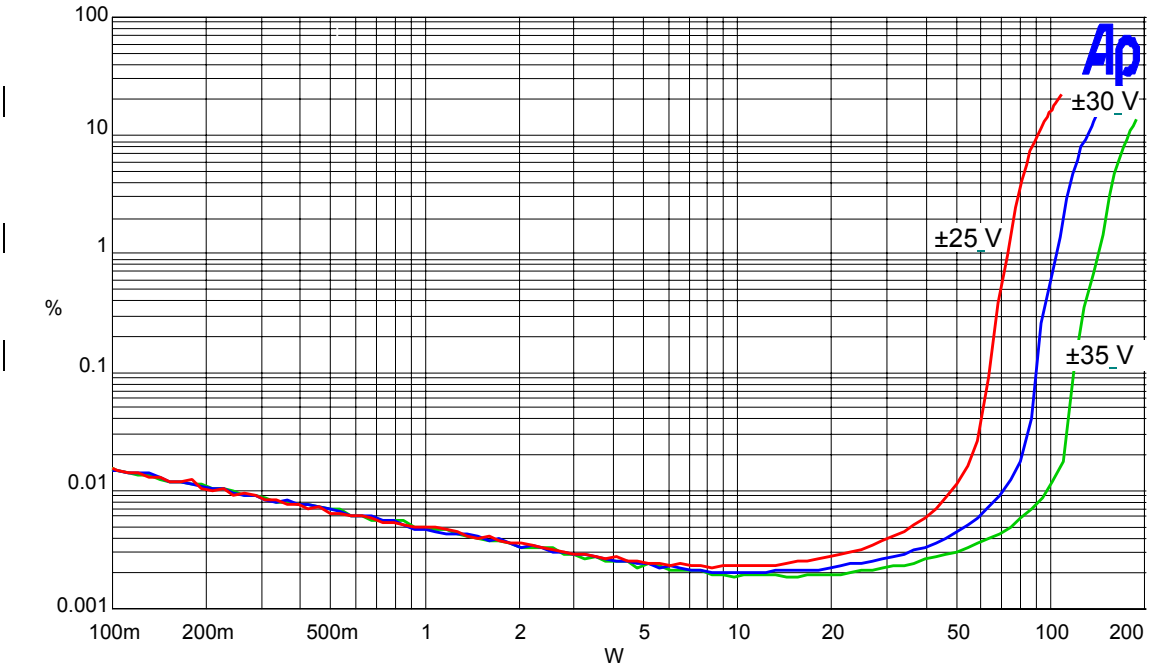
Red	CH2 – CH1, 60 W, Self Oscillator @ 400 kHz
Green	CH2 – CH1, 60 W, Internal Clock @ 300 kHz

Figure 20. Stand-alone Class D Power Stage: Channel Separation vs. Frequency



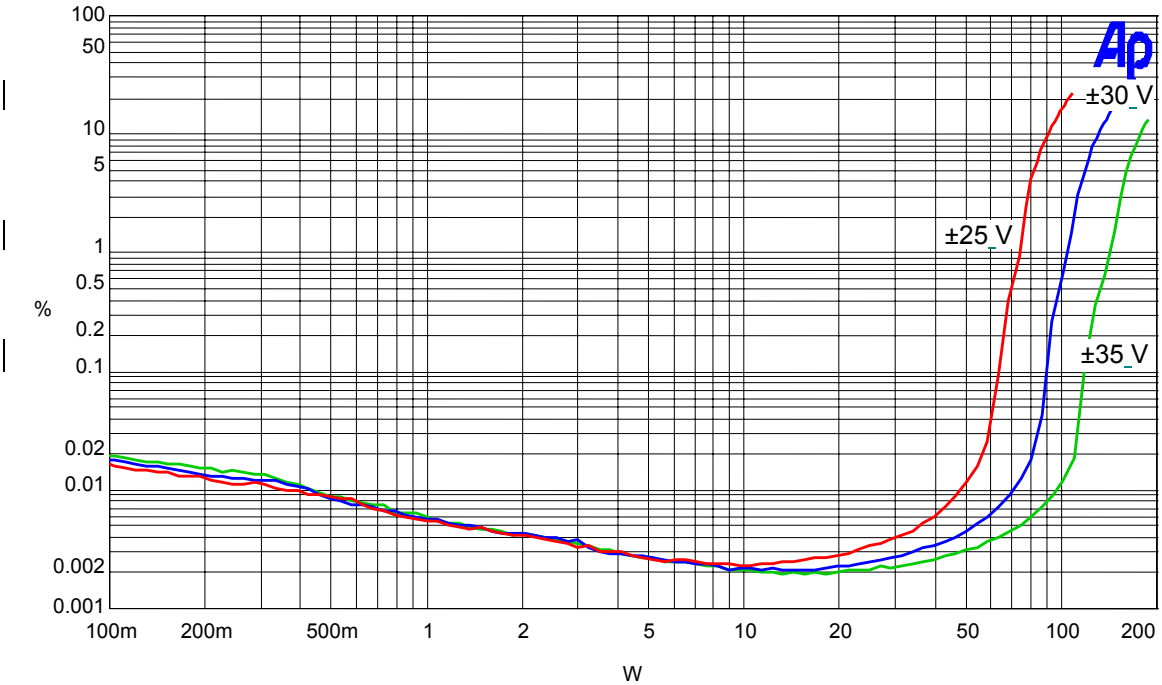
Green	CH1 - ACD, ±B = ± 35 V, Volume gain 21.9 V/V – AUX-25 filter
Red	CH1 - ACD, ±B = ± 35 V, Volume gain 21.9 V/V – 3rd order RC filter

Figure 21. Stand-alone Class D Power Stage: THD+N Ratio vs. Output Power



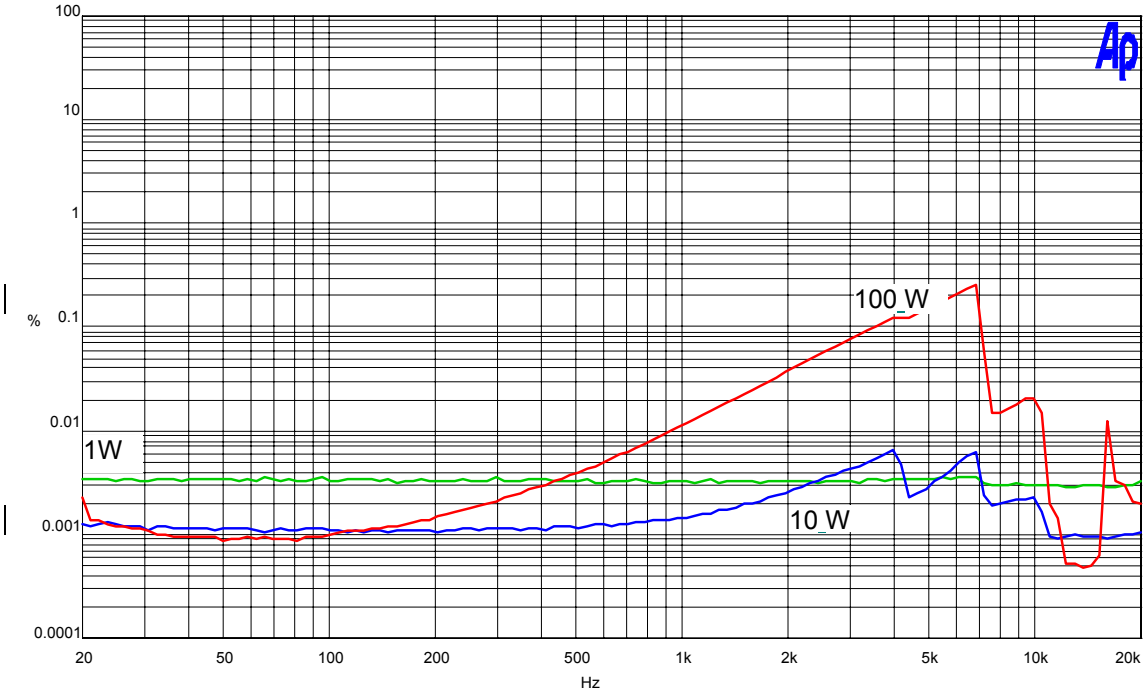
Green	CH1, ±B = ±35 V, Volume gain 21.9 V/V
Blue	CH1, ±B = ±30 V, Volume gain 21.9 V/V
Red	CH1, ±B = ±25 V, Volume gain 21.9 V/V

Figure 22. THD+N Ratio vs. Output Power



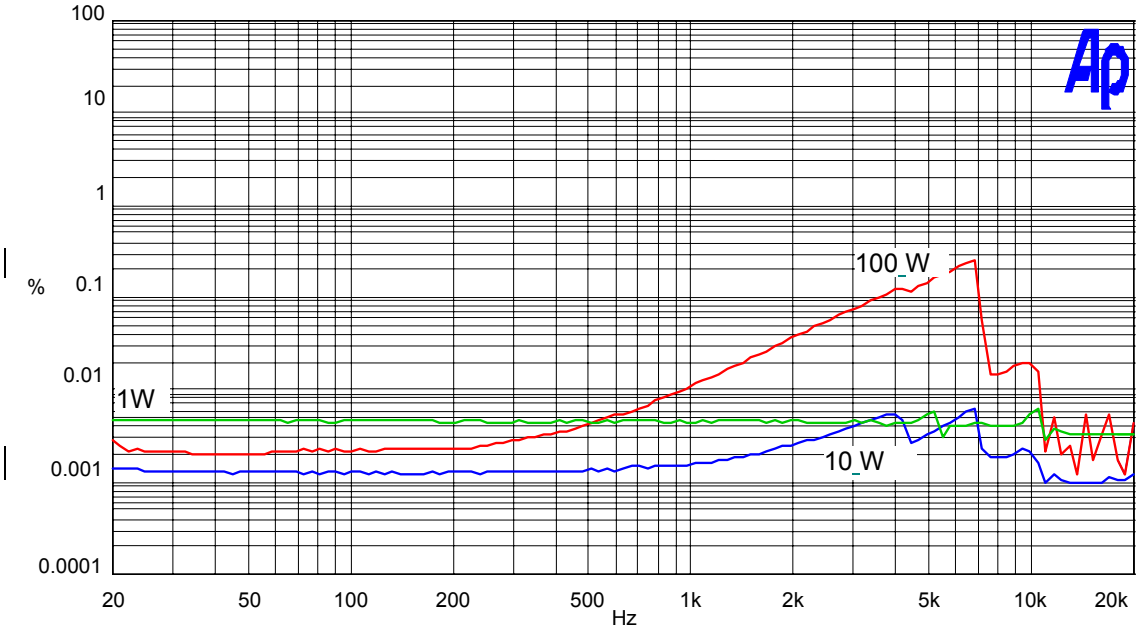
Green	CH1 - ACD, ±B = ±35 V, Volume gain 21.9 V/V
Blue	CH1 - ACD, ±B = ±30 V, Volume gain 21.9 V/V
Red	CH1 - ACD, ±B = ±25 V, Volume gain 21.9 V/V

Figure 23. THD+N Ratio vs. Output Power (ACD)



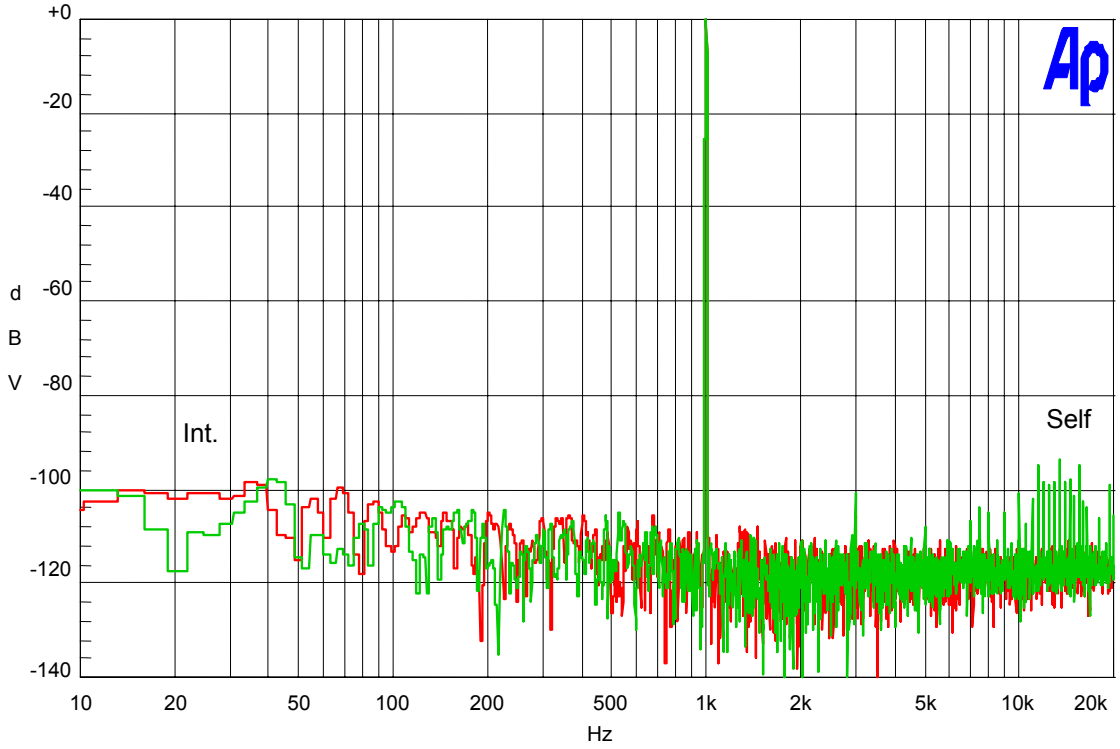
Green	CH1, 1 W Output
Blue	CH1, 10 W Output
Red	CH1, 100 W Output

Figure 24. THD+N Ratio vs. Frequency



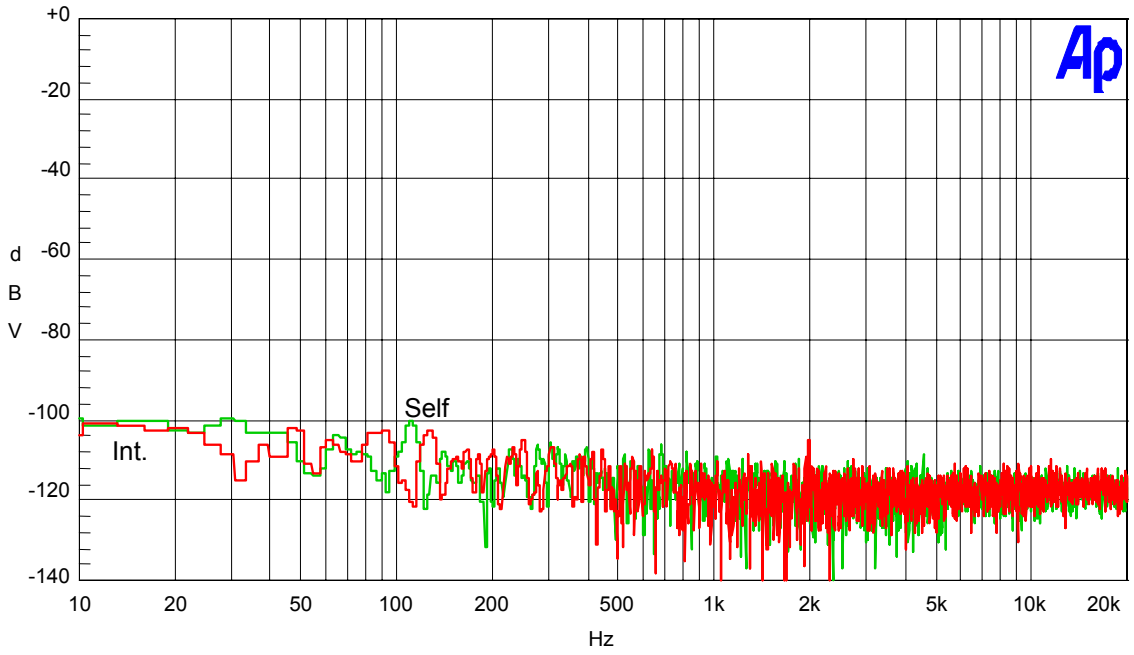
Green	CH1 - ACD, 1 W Output
Yellow	CH1 - ACD, 10 W Output
Red	CH1 - ACD, 100 W Output

Figure 25. THD+N Ratio vs. Frequency (ACD)



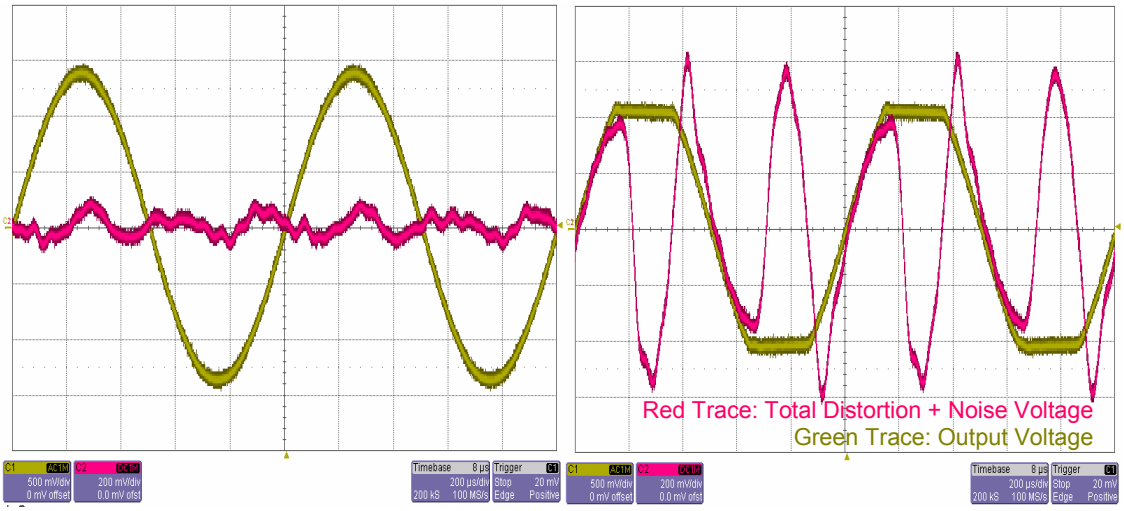
Green	CH1 - ACD, 1 V, 1 kHz, Self Oscillator @ 400 kHz
Red	CH1 - ACD, 1 V, 1 kHz, Internal Clock @ 300 kHz

Figure 26. Frequency Spectrum (ACD)



Green	CH1 - ACD, No signal, Self Oscillator @ 400 kHz
Red	CH1 - ACD, No signal, Internal Clock @ 300 kHz

Figure 27. Residual Noise (ACD)



60 W / 4 Ω, 1 kHz, THD+N=0.004% ***174 W / 4 Ω, 1 kHz, THD+N=10%***

Figure 28. Measured Output and Distortion Waveforms

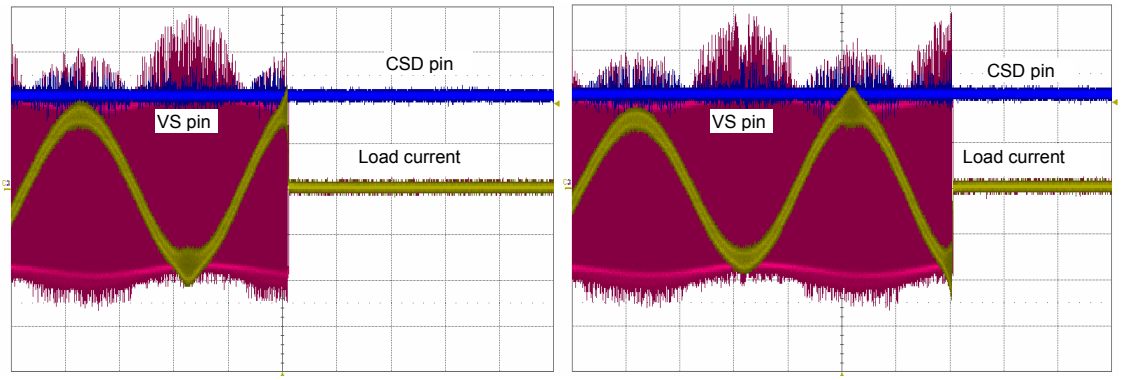


Figure 29. Typical OCP Waveforms Showing Load Current and Switch Node Voltage (V_S)

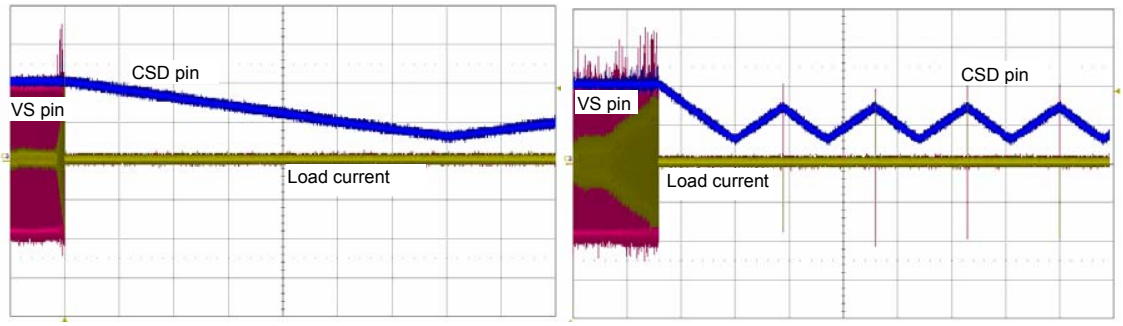


Figure 30. Typical OCP Waveforms Showing CSD Trip and Hiccup

IRAUDAMP4 Design Documents

Motherboard Schematics:

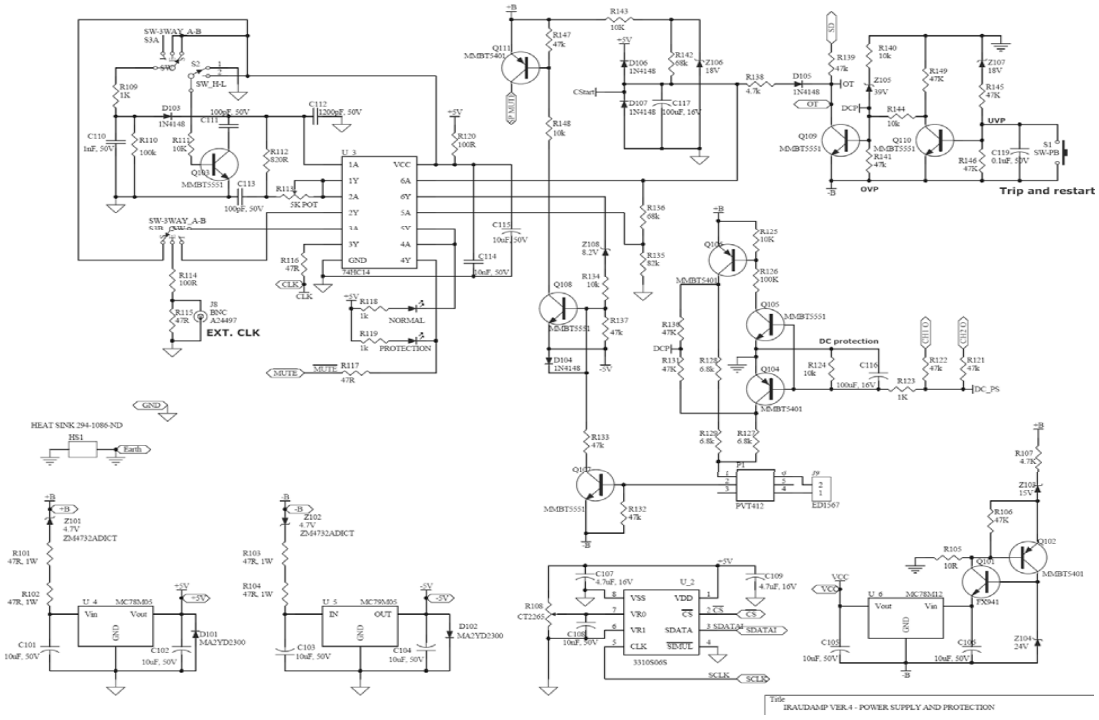


Figure 31. Housekeeping and Protection Circuits

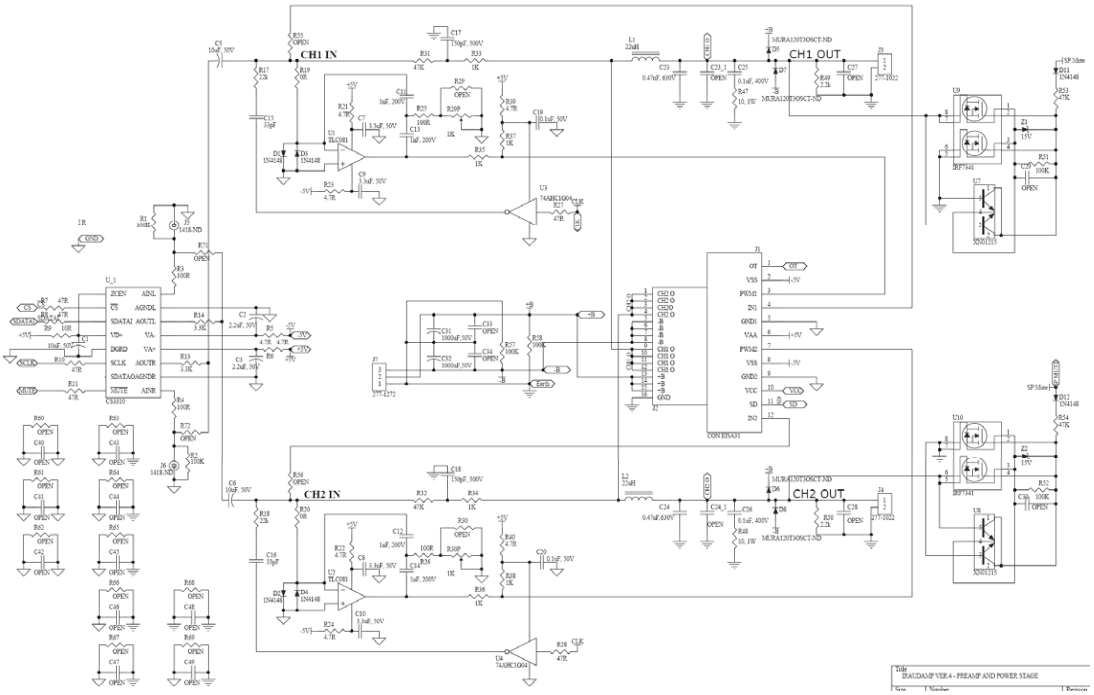


Figure 32. Audio Channels 1 and 2

Daughter Board Schematics:

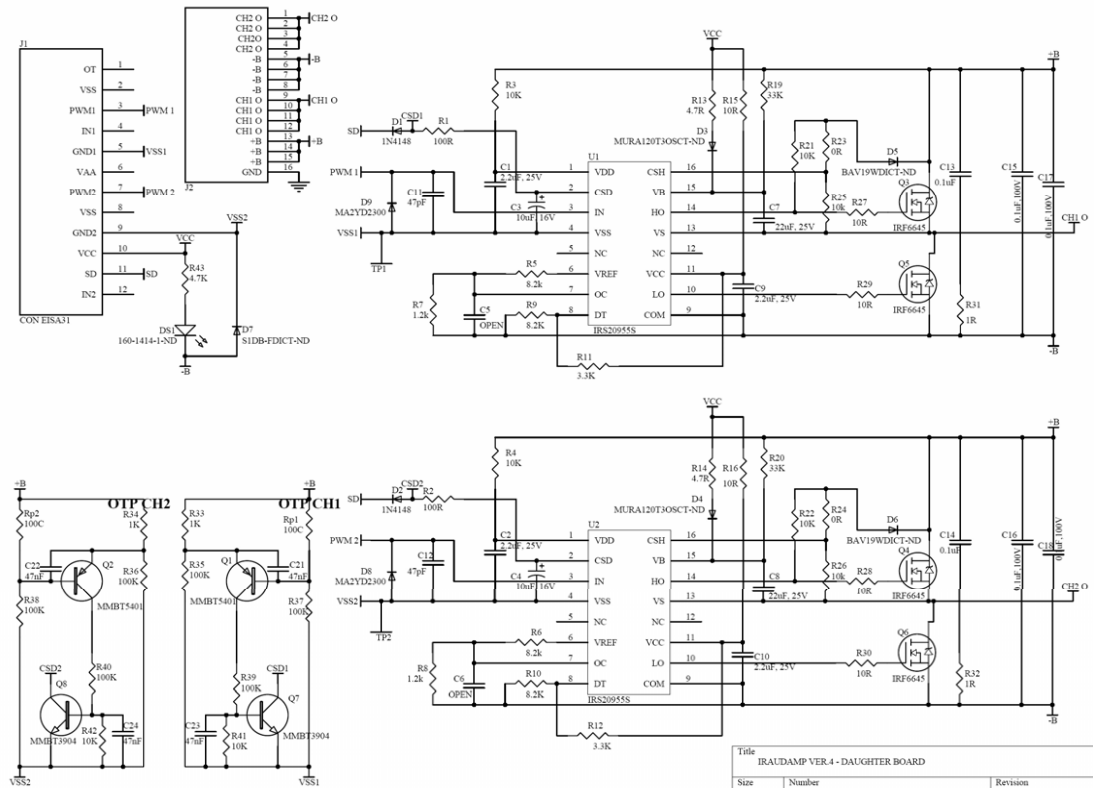


Figure 33. Daughter Board Schematic with Class D Stage for Two Audio Channels

IRAUDAMP4 Bill of Materials

Motherboard:

IRAUDAMP4 MOTHERBOARD BILL OF MATERIAL						
NO	Designator	#	Footprint	PartType	Part No	Vender
1	C1, C5, C6, C101, C102, C103, C104, C105, C106, C115	10	RB2/5	10 µF, 50 V	565-1106-ND	Digikey
2	C2, C3	2	RB2/5	2.2 µF, 50 V	565-1103-ND	Digikey
3	C7, C8, C9, C10	4	CR3225-1210	3.3 µF, 50 V	445-1432-1-ND	Digikey
4	C11, C12, C13, C14	4	1206	1 nF, 200 V	PCC2009CT-ND	Digikey
5	C15, C16	2	0805	33 pF	478-1281-1-ND	Digikey
6	C17, C18	2	AXIAL0.19R	150 pF, 500 V	338-1052-ND	Digikey
7	C19, C20, C119	3	1206	0.1 µF, 50 V	PCC104BCT-ND	Digikey
8	C23, C24	2	CAP MKP	0.47 µF, 630 V	495-1315-ND	Digikey
9	C23_1, C24_1	2	AXIAL0.2R	OPEN	-	Digikey
10	C25, C26	2	CAP MKPs	0.1 µF, 400 V	495-1311-ND	Digikey
11	C27, C28, C29, C30, C40, C41, C42, C43, C44, C45, C46, C47	12	0805	OPEN	-	Digikey
12	R29, R30, R55, R56, R60, R61, R62, R63, R64, R65, R66, R67, R71, R72	14	0805	OPEN	-	Digikey
13	C31, C32	2	RB5/12_5	1000 µF,50 V	565-1114-ND	Digikey
14	C33, C34, C48, C49	4	AXIAL0.1R	OPEN	-	Digikey
15	C107, C109	2	0805	4.7 µF, 16 V	PCC2323CT-ND	Digikey
16	C108, C114	2	0805	10 nF, 50 V	PCC103BNCT-ND	Digikey
17	C110	1	0805	1 nF, 50 V	PCC102CGCT-ND	Digikey
18	C111, C113	2	0805	100 pF, 50 V	PCC101CGCT-ND	Digikey
19	C112	1	0805	1200 pF, 50 V	478-1372-1-ND	Digikey
20	C116, C117	2	rb2/5	100 µF, 16 V	565-1037-ND	Digikey
21	D1, D2, D3, D4, D11, D12, D103, D104, D105, D106, D107	11	SOD-123	1N4148	1N4148WDICT-ND	Digikey
22	D5, D6, D7, D8	4	SMA	MURA120	MURA120T3OSCT-ND	Digikey
23	D101, D102	2	SOD-123	MA2YD2300	MA2YD2300LCT-ND	Digikey
24	HS1	1	Heat_S6in1	HEAT SINK	294-1086-ND	Digikey
25	J1A, J1B	2	CON EISA-31	CON EISA31	A26453-ND	Digikey
26	J2A, J2B	2	CON_POWER	CON_POWER	A26454-ND	Digikey
27	J3, J4	2	MKDS5/2-9.5	277-1022	277-1271-ND or 651-1714971	Digikey or Mouser
28	J5, J6	2	cp1418	1418-ND	CP-1418-ND	Digikey
29	J7	1	J HEADER3	277-1272	277-1272-ND or 651-1714984	Digikey or Mouser
30	J8	1	BNC_RA CON	BNC	A32248-ND	Digikey
31	J9	1	ED1567	ED1567	ED1567	Digikey
32	L1, L2	2	Inductor	22 µH	ETQA21ZA220 or ETQA17B220	Panasonic
33	NORMAL	1	Led rb2/5	404-1106-ND	160-1143-ND	Digikey
34	P1	1	DIP-6	PVT412	PVT412-ND	Digikey
35	PROTECTION	1	Led rb2/5	404-1109-ND	160-1140-ND	Digikey
36	Q101	1	SOT89	FX941	FCX491CT-ND	Digikey
37	Q102, Q104, Q106, Q111	4	SOT23-BCE	MMBT5401	MMBT5401DICT-ND	Digikey
38	Q103, Q105, Q107, Q108, Q109, Q110	6	SOT23-BCE	MMBT5551	MMBT5551-7DICT-ND	Digikey
39	R1, R2, R51, R52, R57, R58, R110, R126	8	0805	100 kΩ	P100KACT-ND	Digikey
40	R3, R4, R114	3	0805	100 Ω	P100ACT-ND	Digikey
41	R5, R6	2	1206	4.7 Ω	P4.7ECT-ND	Digikey
42	R7, R8, R10, R11, R27, R28, R115, R116, R117	9	0805	47 Ω	P47ACT-ND	Digikey
43	R9, R105	2	0805	10 Ω	P10ACT-ND	Digikey
44	R13, R14	2	0805	3.3 kΩ, 1%	P3.3KZCT-ND	Digikey
45	R17, R18	2	0805	22 kΩ	P22KACT-ND	Digikey
46	R53, R54, R106, R121, R122, R130, R131, R132, R133, R137, R139, R141, R145, R146, R147, R149	16	0805	47 kΩ	P47KACT-ND	Digikey
47	R19, R20	2	0805	0 Ω	P0.0ACT-ND	Digikey
48	R21, R22, R23, R24, R39, R40	6	0805	4.7 Ω	P4.7ACT-ND	Digikey
49	R25, R26, R120	3	1206	100 Ω	P100ECT-ND	Digikey
50	R29P, R30P	2	POT_SRM	1 kΩ	3361P-102GCT-ND	Digikey
51	R31, R32	2	2512	47 kΩ, 1%	PT47KAFCT-ND	Digikey
52	R33, R34	2	1206	1 kΩ	P1.0KECT-ND	Digikey
53	R35, R36, R37, R38, R109, R118, R119, R123	8	0805	1 kΩ	P1.0KACT-ND	Digikey
54	R47, R48	2	2512	10, 1 W	PT10XCT	Digikey

55	R49, R50	2	1206	2.2 kΩ	P2.2KECT-ND	Digikey
56	R68, R69	2	AXIAL-0.3	OPEN	-	Digikey
57	R101, R102, R103, R104	4	2512	47 Ω, 1 W	PT47XCT-ND	Digikey
58	R107, R138	2	0805	4.7 kΩ	P4.7KACT-ND	Digikey
59	R108	1	V_Control	CT2265	CT2265-ND	Digikey
60	R111, R124, R125, R134, R140, R143, R144, R148	8	0805	10 kΩ	P10KACT-ND	Digikey
61	R112	1	0805	820 Ω	P820ACT-ND	Digikey
62	R113	1	POTs	5 kΩ POT	3362H-502-ND	Digikey
63	R127, R128, R129	3	1206	6.8 kΩ	P6.8KECT-ND	Digikey
64	R135	1	0805	82 kΩ	P82KACT-ND	Digikey
65	R136, R142	2	0805	68 kΩ	P68KACT-ND	Digikey
66	S1	1	Switch	SW-PB	P8010S-ND	Digikey
67	S2	1	SW-EG1908-ND	SW_H-L	EG1908-ND	Digikey
68	S3	1	SW-EG1944-ND	SW-3WAY	EG1944-ND	Digikey
69	U1, U2	2	SO-8	TLC081	296-7264-1-ND	Digikey
70	U3, U4	2	SOT25	74AHC1G04	296-1089-1-ND	Digikey
71	U7, U8	2	MINI5	XN01215	XN0121500LCT-ND	Digikey
72	U9, U10	2	SO-8	IRF7341	IRF7341	IR
73	U_1	1	SOIC16	CS3310	73C8016 or 72J5420	Newark
74	U_2	1	N8A	3310S06S	3310-IR01	*Tachyonix
75	U_3	1	M14A	74HC14	296-1194-1-ND	Digikey
76	U_4	1	TO-220 Fullpak	MC78M05	MC78M05BTOS-ND	Digikey
77	U_5	1	TO-220 Fullpak	MC79M05	MC79M05CTOS-ND	Digikey
78	U_6	1	TO-220 Fullpak	MC78M12	MC78M12CTOS-ND	Digikey
79	Z1, Z2, Z103	3	SOD-123	15 V	BZT52C15-FDICT-ND	Digikey
80	Z101, Z102	2	DL-41	4.7 V	22H3923	Newark
81	Z104	1	SOD-123	24 V	BZT52C24-FDICT-ND	Digikey
82	Z105	1	SOD-123	39 V	BZT52C39-13-FDICT-ND	Digikey
83	Z106, Z107	2	SOD-123	18 V	BZT52C18-FDICT-ND	Digikey
84	Z108	1	SOD-123	8.2 V	BZT52C8V2-FDICT-ND	Digikey
85	Volume Knob	1			MCCPMB1	Newark
86	Thermalloy TO-220 mounting kit with screw	3			46F4081	Newark
87	1/2" Standoffs 4-40	5			8401K-ND	Digikey
88	4-40 Nut	5	100 per bag		H724-ND	Digikey

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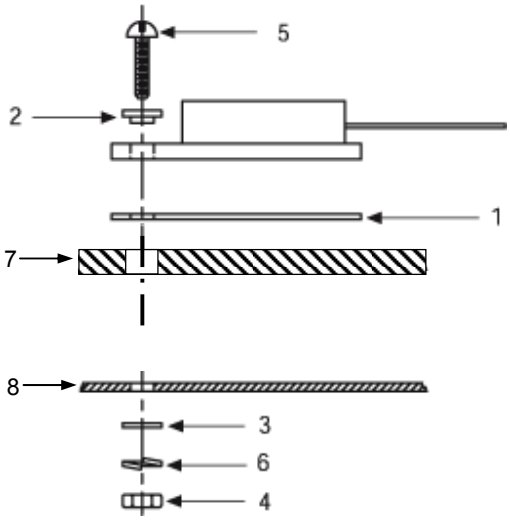
Ama-gun Aichi, JAPAN 490-1111

http://www.tachyonix.co.jp
info@tachyonix.co.jp

Voltage regulator mounting:



Item	Description
1	Insulator Thermalfilm
2	Shoulder Washer
3	Flat Washer #4
4	No. 4-40 UNC-2B Hex Nut
5	No. 4-40 UNC-2A X 1/2 Long Phillips Pan Head Screw
6	Lockwasher, No.4
7	Heatsink
8	PCB

Daughter Board:

IRAUDAMP4 DAUTHER-BOARD BILL OF MATERIAL						
NO	Designator	#	Footprint	Part Type	Part No	Vendor
1	C1, C2, C9, C10	4	1206	2.2 µF, 25 V	490-3368-1-ND	Digikey
2	C3, C4	2	T491	10 µF, 16 V	399-3706-1-ND	Digikey
3	C5, C6	2	0805	OPEN		
4	C7, C8	2	1812	22 µF, 25 V	445-1607-1-ND	Digikey
5	C11, C12	2	0805	47 pF	PCC470CGCT-ND	Digikey
6	C13, C14	2	0805	0.1 µF	PCC1840CT-ND	Digikey
7	C15, C16, C17, C18	4	1206	0.1 µF,100 V	PCC2239CT-ND	Digikey
8	C21, C22, C23, C24	4	0805	47 nF	PCC1836CT-ND	Digikey
9	D1, D2	2	SOD-123	1N4148	1N4148WDICT-ND	Digikey
10	D3, D4	2	SMA	MURA120T3OSCT-ND	MURA120T3OSCT-ND	Digikey
11	D5, D6	2	SOD-123	BAV19WDICT-ND	BAV19W-FDICT-ND	Digikey
12	D7	1	SMB	S1DB-FDICT-ND	RS1DB-FDICT-ND	Digikey
13	D8, D9	2	SOD-123	MA2YD2300	MA2YD2300LCT-ND	Digikey
14	DS1	1	LED	160-1414-1-ND	160-1414-1-ND	Digikey
15	J1	1	CON EISA-31	CON EISA31	2011-03-ND	Digikey
16	J2	1	CON_POWER	CON_POWER	2011-04-ND	Digikey
17	Q1, Q2	2	SOT23-BCE	MMBT5401	MMBT5401DICT-ND	Digikey
18	Q3, Q4, Q5, Q6	4	DirectFET MOSFET6645	IRF6645	IRF6645	IR
19	Q7, Q8	2	SOT23-BCE	MMBT3904	MMBT3904-FDICT-ND	Digikey
20	R1, R2	2	0805	100 Ω	P100ACT-ND	Digikey
21	R3, R4, R25, R26	4	1206	10 kΩ	P10KECT-ND	Digikey
22	R5, R6, R9, R10	4	0805	8.2 kΩ	P8.2KACT-ND	Digikey
23	R7, R8	2	0805	1.2 kΩ	P1.2KACT-ND	Digikey
24	R11, R12	2	0805	3.3 kΩ	P3.3KACT-ND	Digikey
25	R13, R14	2	0805	4.7 Ω	P4.7ACT-ND	Digikey
26	R15, R16, R27, R28, R29, R30	6	0805	10 Ω	P10ACT-ND	Digikey
27	R19, R20	2	0805	33 kΩ	P33KACT-ND	Digikey
28	R21, R22, R41, R42	4	0805	10 kΩ	P10KACT-ND	Digikey
29	R23, R24	2	0805	0 Ω	P0.0ACT-ND	Digikey
30	R31, R32	2	0805	1 Ω	P1.0ACT-ND	Digikey
31	R33, R34	2	0805	1 kΩ	P1.0KACT-ND	Digikey
32	R35, R36, R37, R38, R39, R40	6	0805	100 kΩ	P100KACT-ND	Digikey
33	R43	1	0805	4.7 kΩ	P4.7KACT-ND	Digikey
34	Rp1, Rp2	2	0805	100 C	594-2322-675-21007	Mouser
35	U1, U2	2	M16A	IRS20955SPBF	IRS20955SPBF	IR

IRAUDAMP4 PCB Specifications

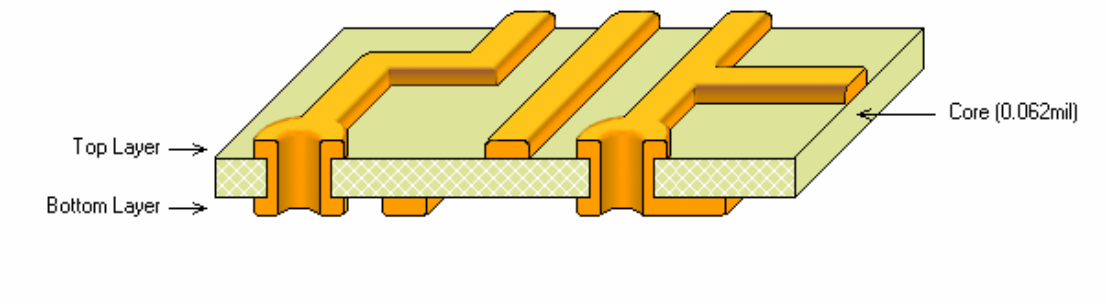


Figure 34. Motherboard and Daughter Board Layer Stack

Motherboard:

Material:	FR4, UL 125 °C
Layer stack:	2 layers, 1 oz. Cu
Dimensions:	5.2 in x 5.8 in x 0.062 in
Solder mask:	LPI solder mask, SMOBC on top and bottom layers
Plating:	Open copper solder finish
Silkscreen:	On top and bottom layers

Daughter board:

Material:	FR4, UL 125 °C
Layer stack:	2 Layers, 1 oz. Cu each, through-hole plated
Dimensions:	3.125 in x 1.52 in x 0.062 in
Solder mask:	LPI solder mask, SMOBC on top and bottom layers
Plating:	Open copper solder finish
Silkscreen:	On top and bottom layers

IRAUDAMP4 PCB Layers

Motherboard:

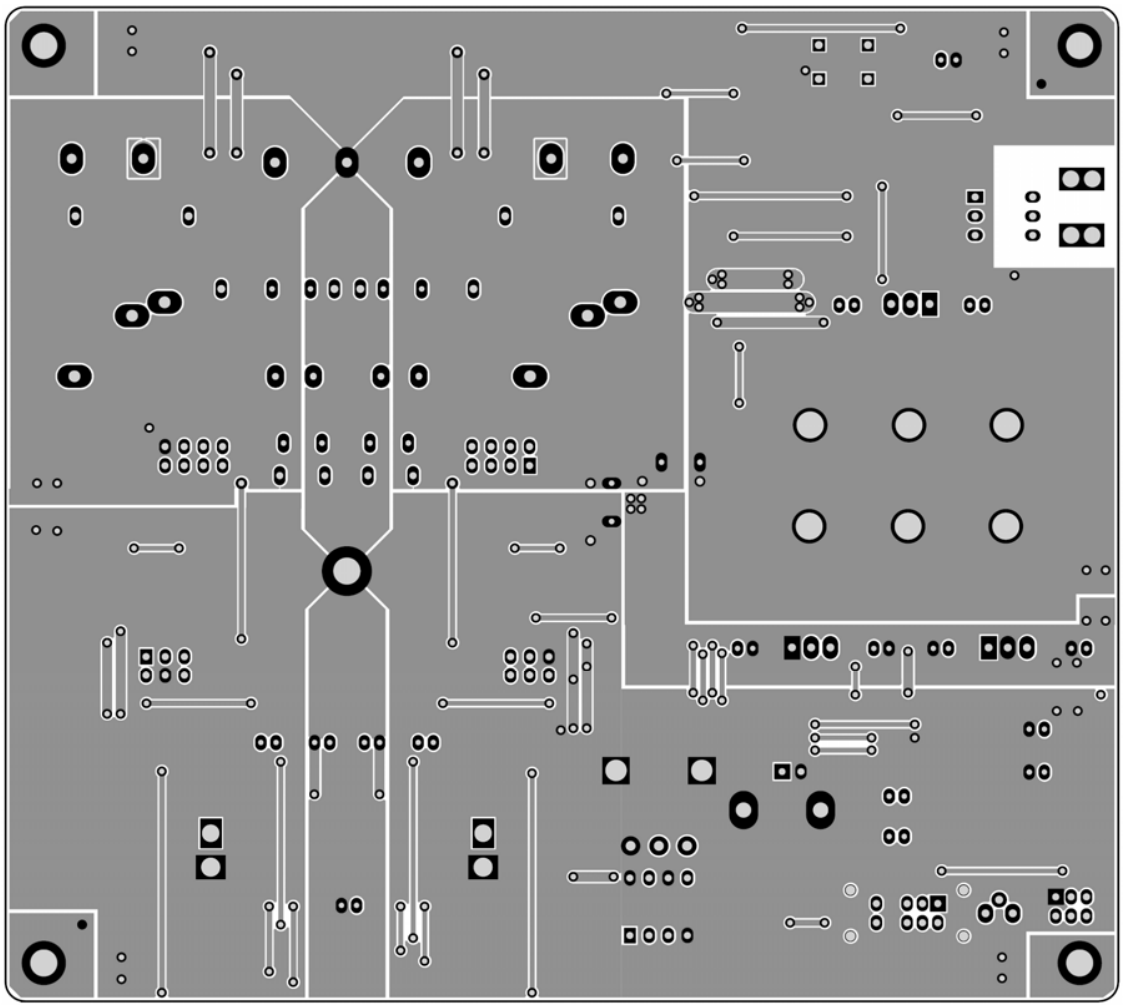


Figure 35. Top Layer and Pads

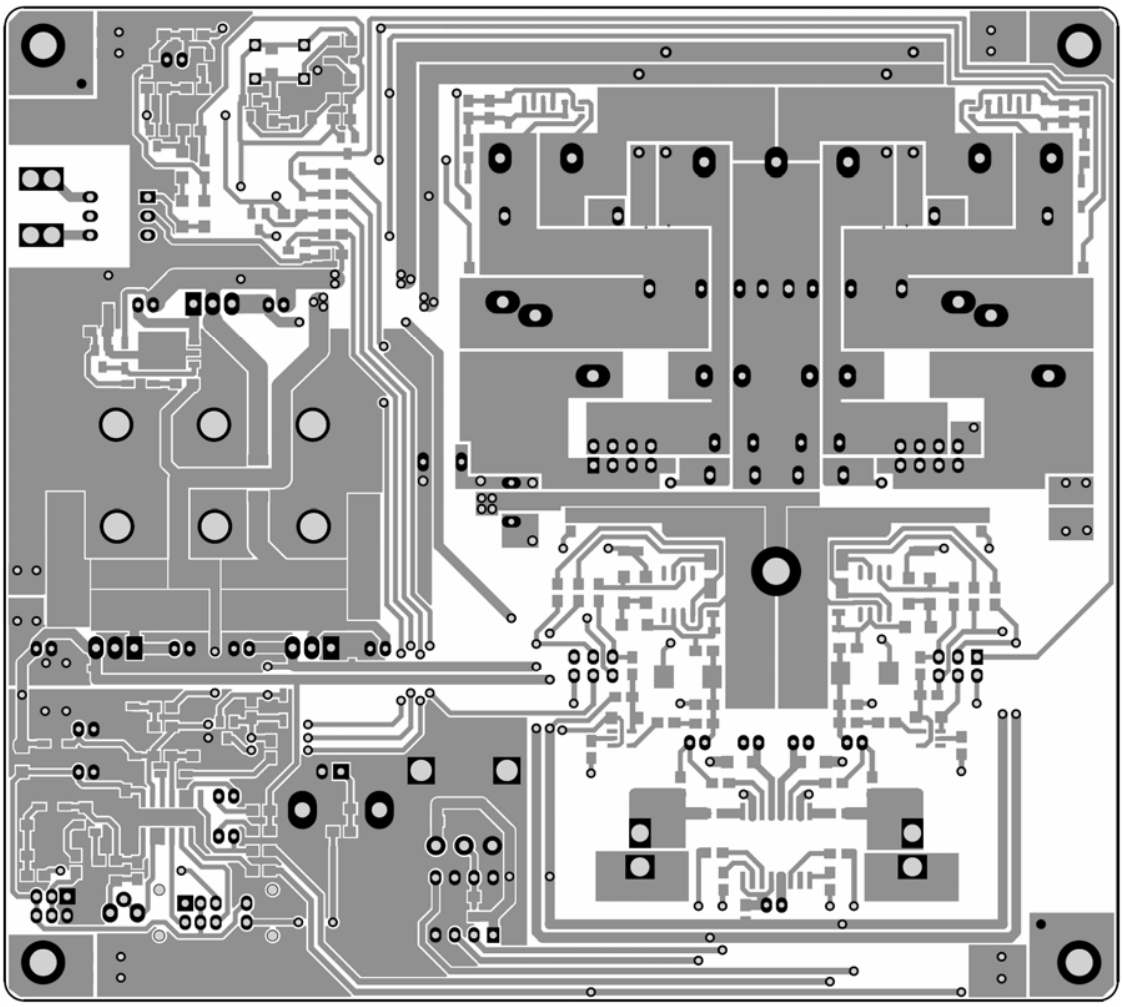


Figure 36. Bottom Layer and Pads

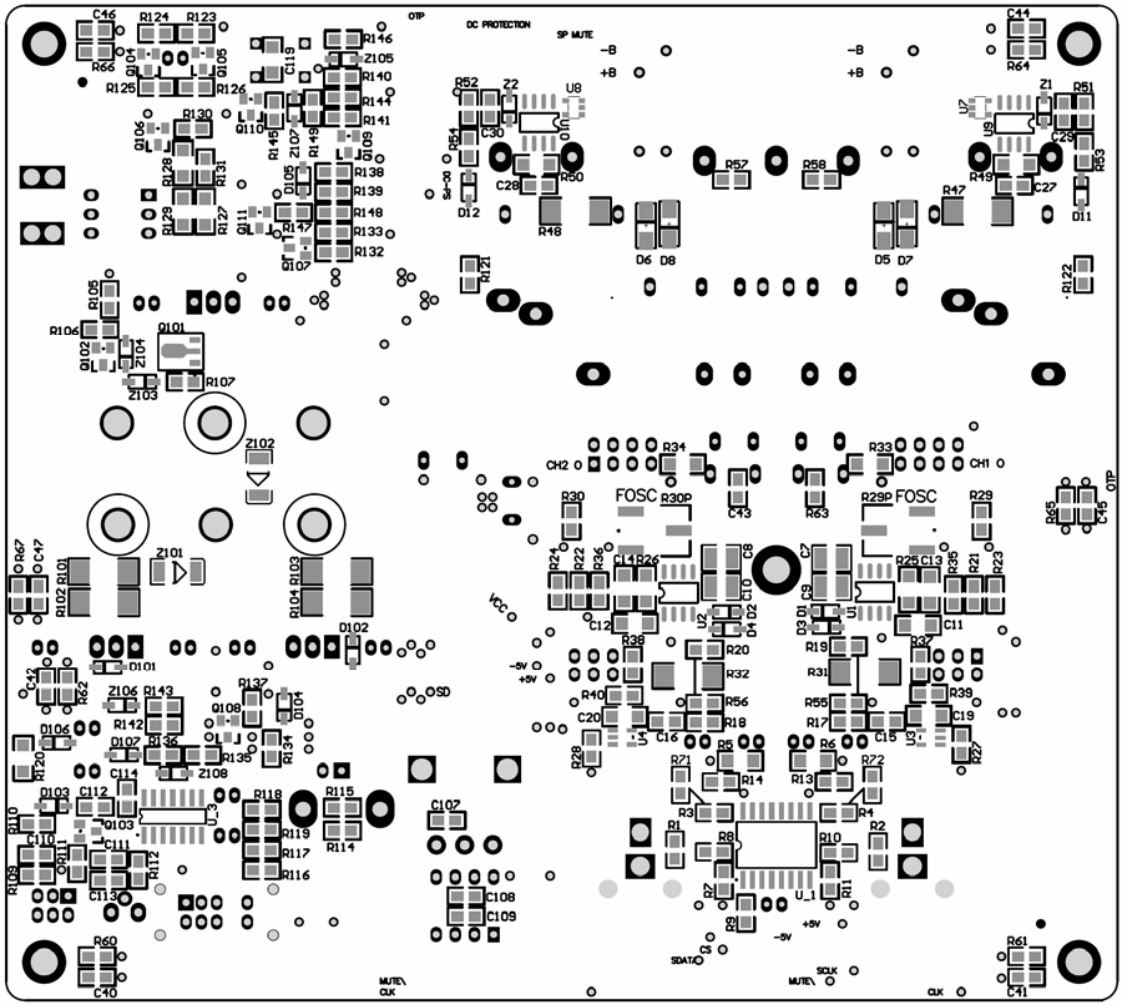


Figure 37. Bottom-Side Solder-Mask and Silkscreen

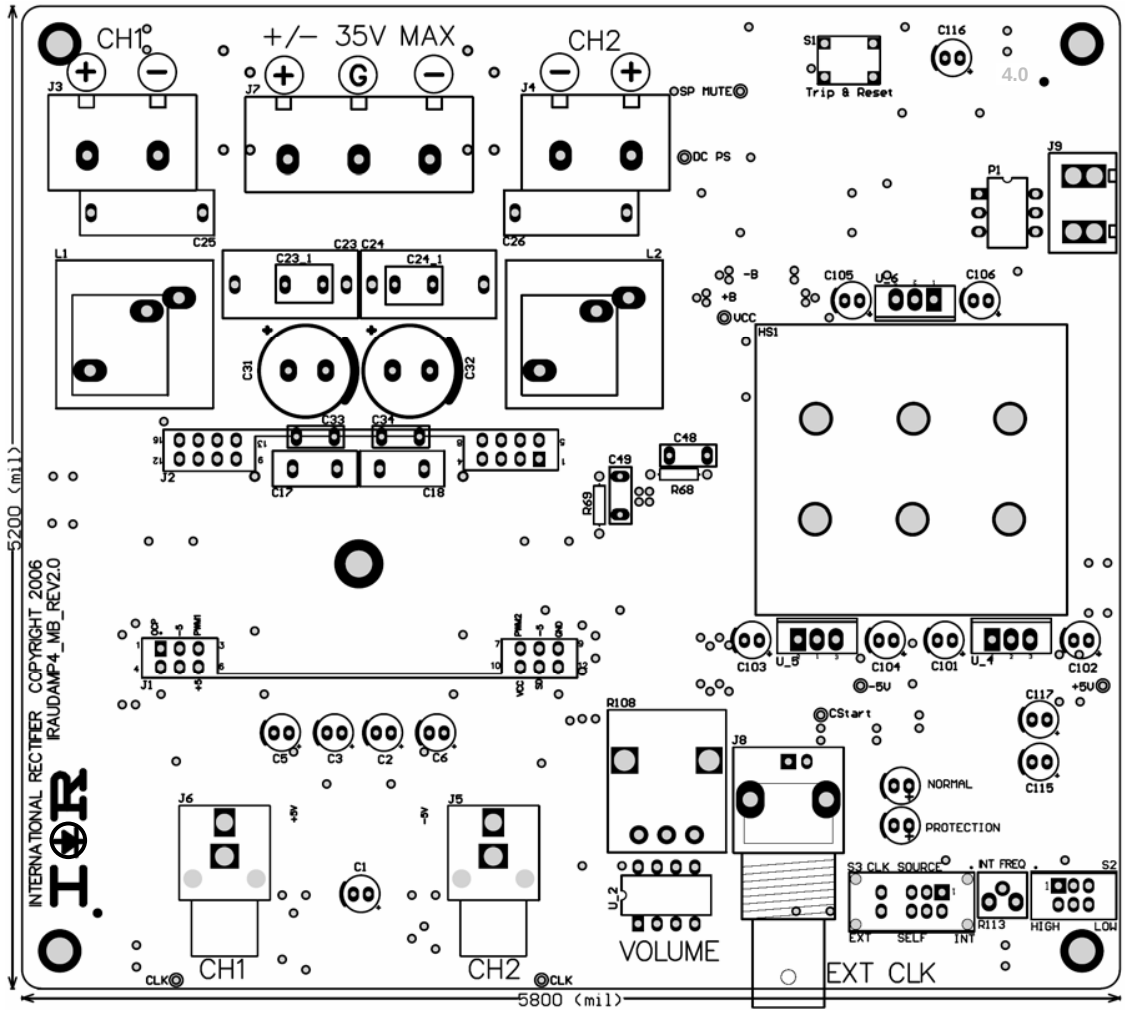


Figure 38. Top-Side Solder-Mask and Silkscreen

Daughter Board:

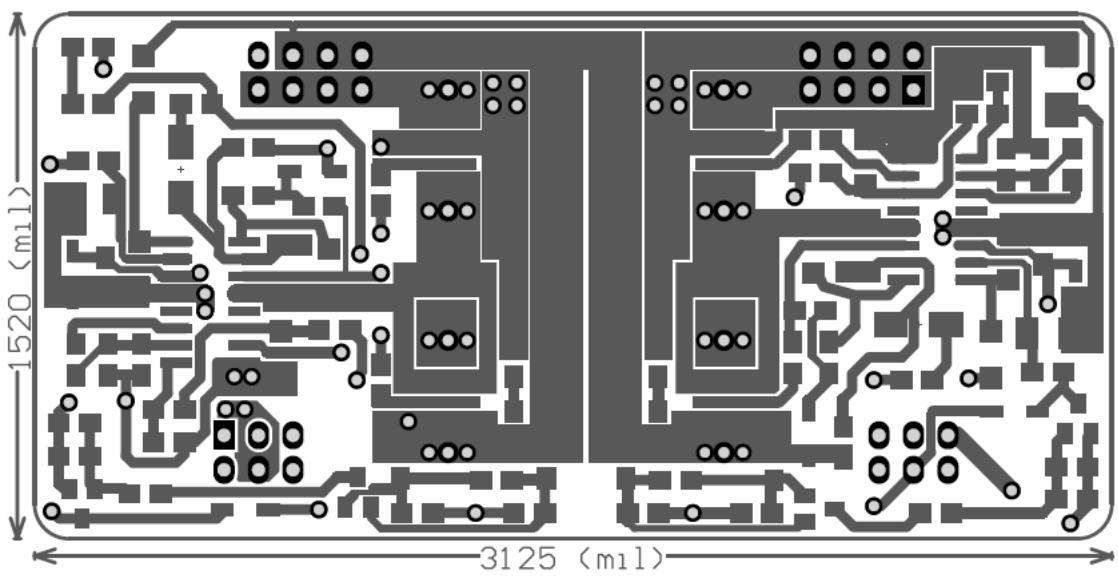


Figure 39. PCB Layout – Top Layer and Pads

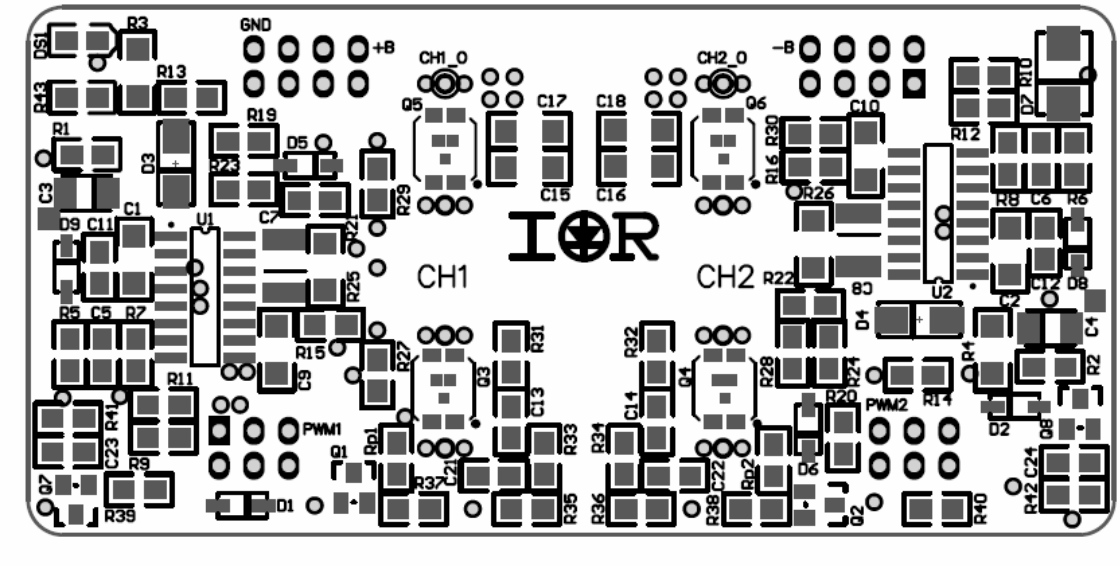


Figure 40. PCB Layout – Top-Side Solder-Mask and Silkscreen

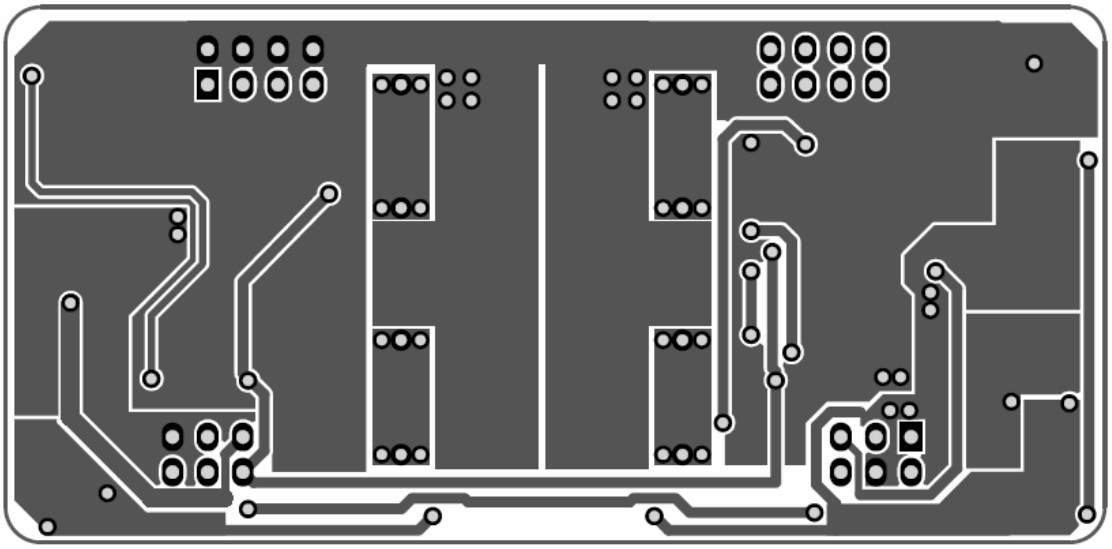


Figure 41. PCB Layout – Bottom Layer and Pads

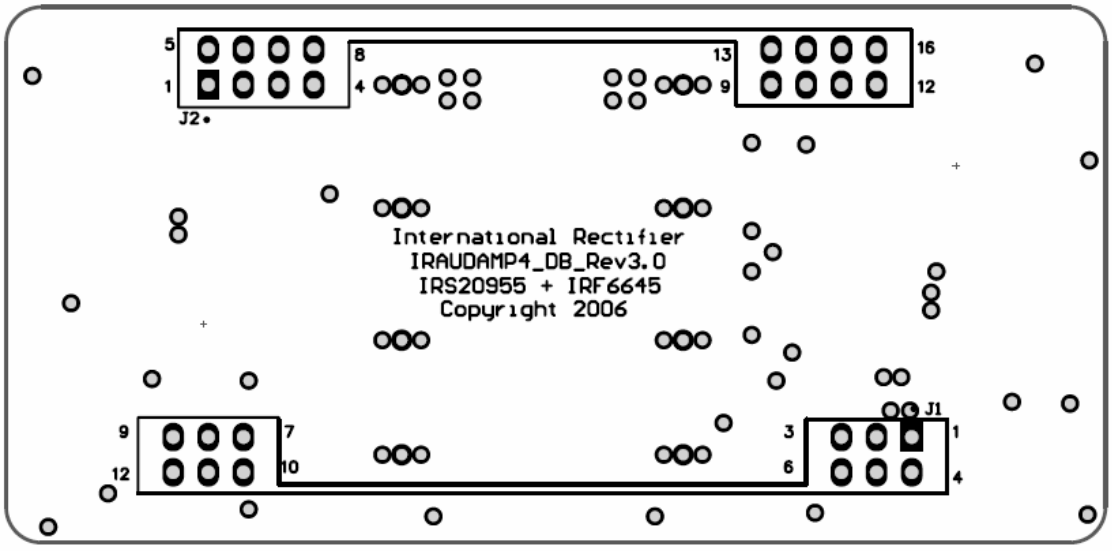


Figure 42. PCB Layout – Bottom-Side Solder-Mask and Silkscreen

IRAUDAMP4 Mechanical Construction

Motherboard

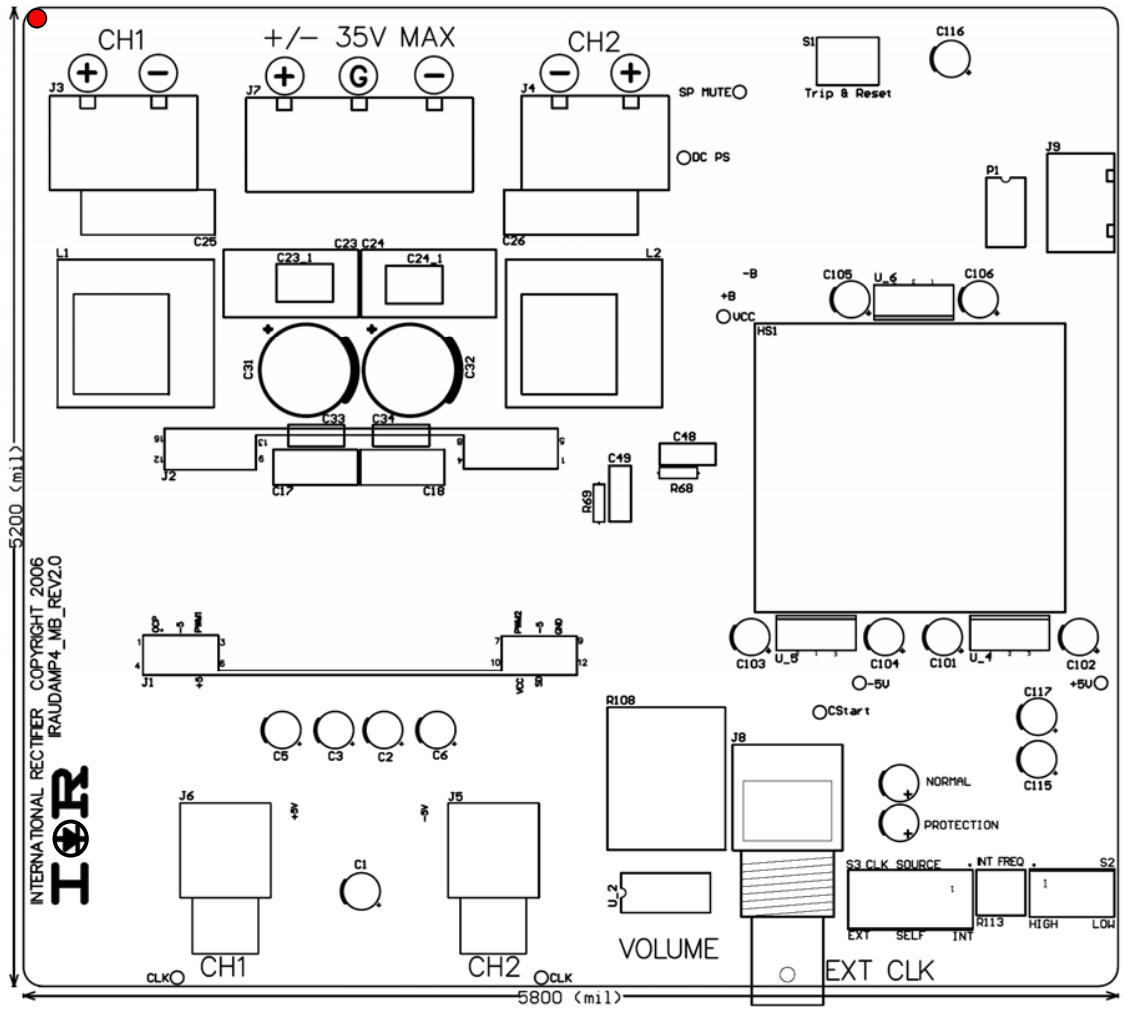


Figure 43. Top Side of Motherboard Showing Component Locations

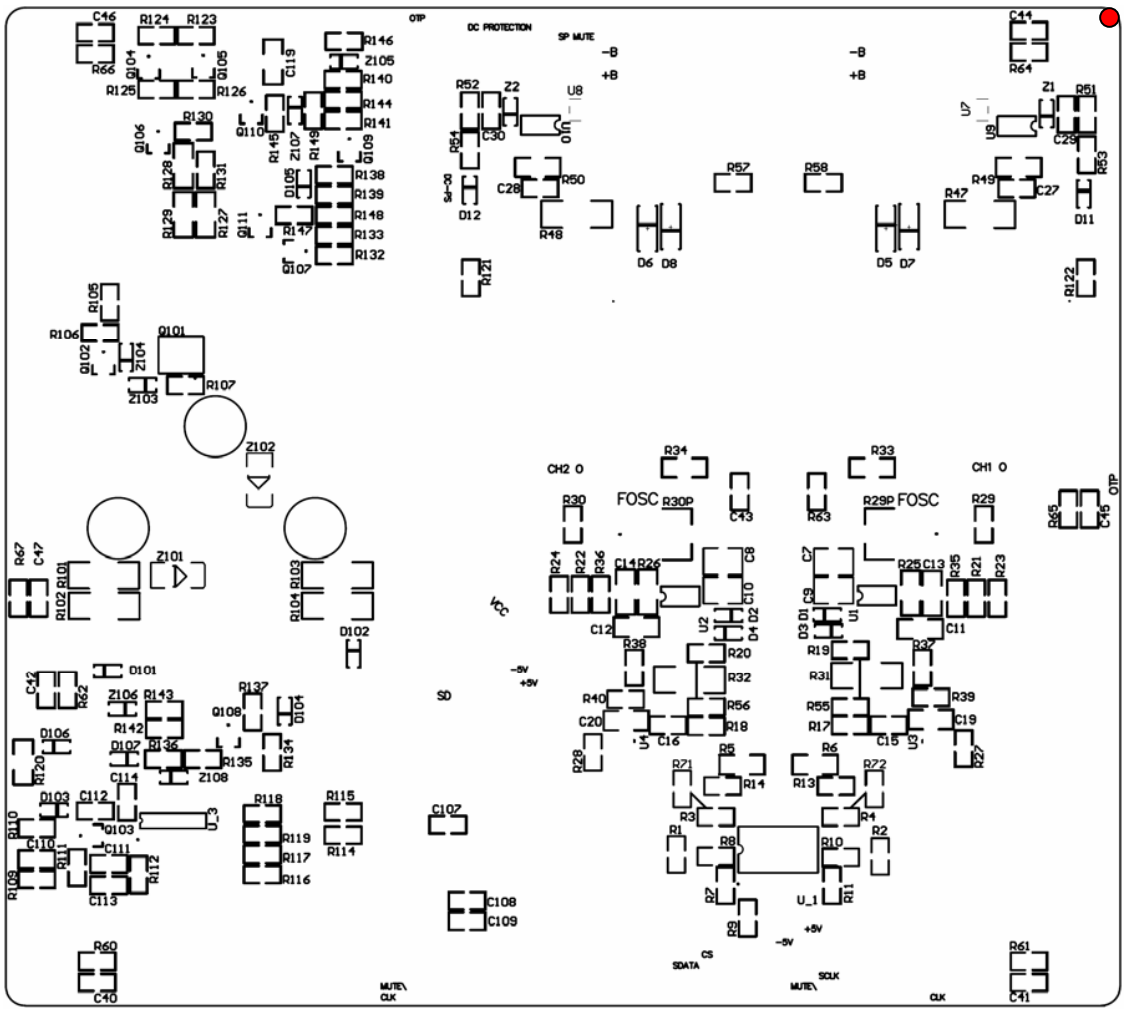


Figure 44. Bottom Side of Motherboard Showing Component Locations

Daughter Board

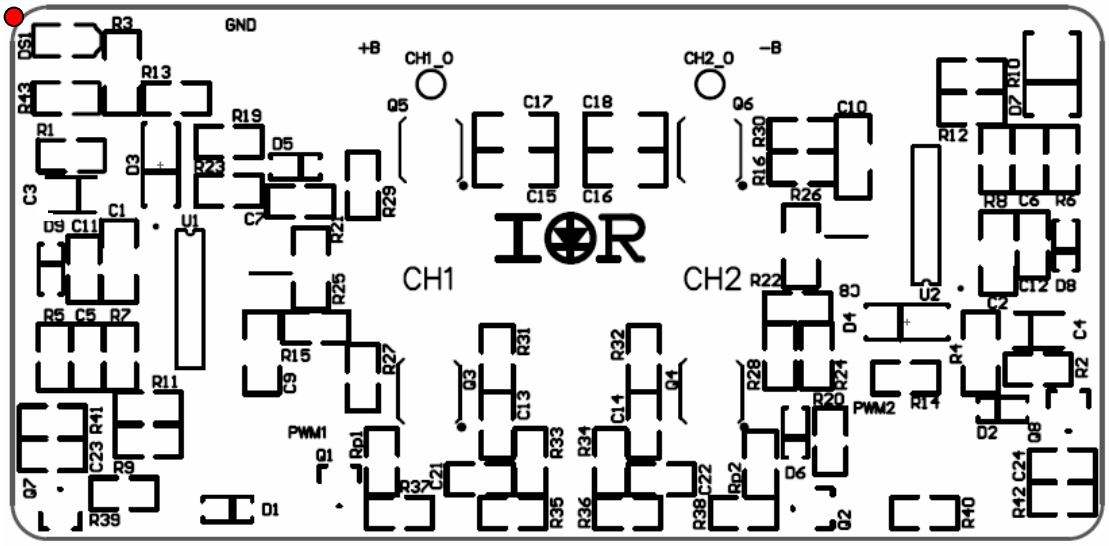


Figure 45. Top Side Showing Component Locations

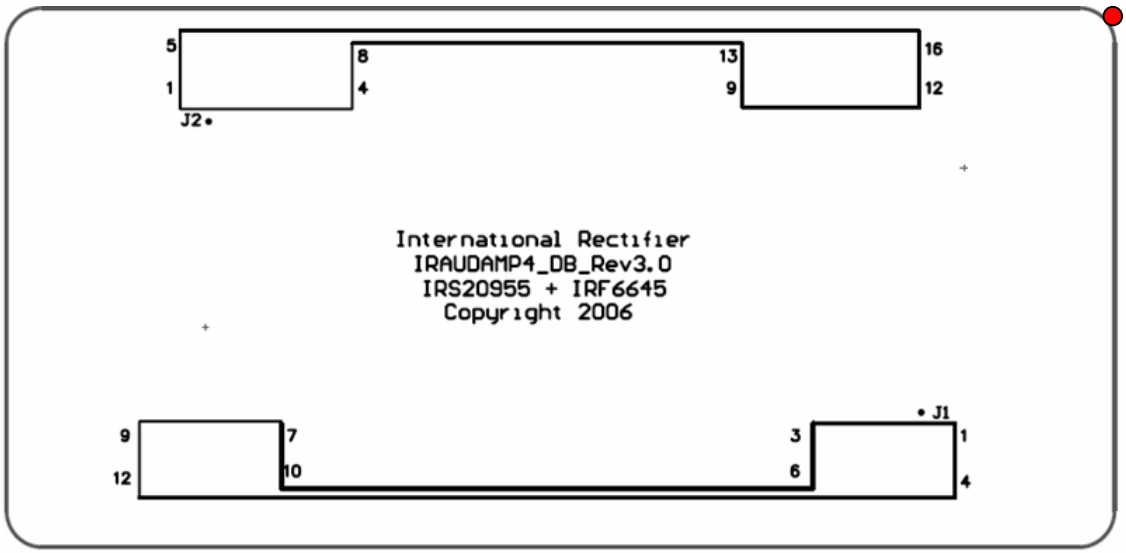


Figure 46. Bottom Side Showing Connector Locations

02/15/2007