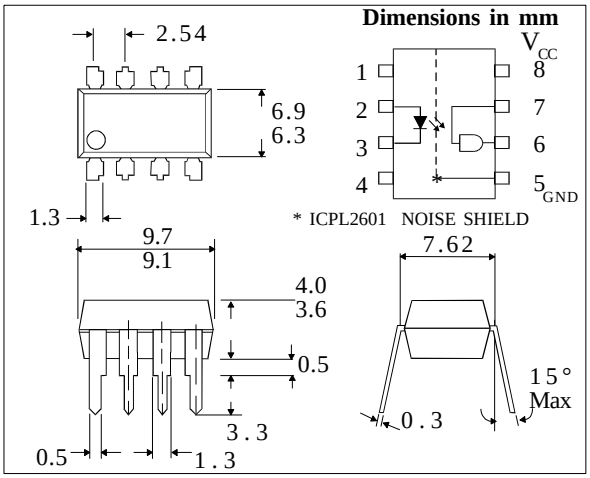
ICPL2611

HIGH CMR, HIGH SPEED OPTO ISOLATOR



DESCRIPTION

The ICPL 2611 consists of a GaAsP emitting diode and a unique integrated detector. The photons are detected by a photodiode and then amplified by a high gain linear amplifier that drives a logic gate with a strobable output. This output features a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated. This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA will sink an eight gate fan-out (13mA) at the output with 5 volt Vcc supplied to the detector. This isolation and coupling is achieved with a typical propagation delay of 39ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 35ns typical.

FEATURES

- LSTTL/TTL Compatible
- High Speed
- Low Input Current Required
- Guaranteed Performance over Temperature
- 2500 V_{RMS} Withstand Test Voltage (1 Minute)
- Internal Shield for High Common Mode Rejection

TRUTHTABLE

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

A 0.1µF bypass capacitor must be connected between pins 8 and 5 (See note 1)

ABSOLUTE MAXIMUM RATINGS

(25 °C unless otherwise noted)

Storage Temperature	-55 to +125°C
Operating Temperature	-0°C to +70°C
Lead Solder Temperature	260°C for 10secs
(1.6mm below the seating plate)	

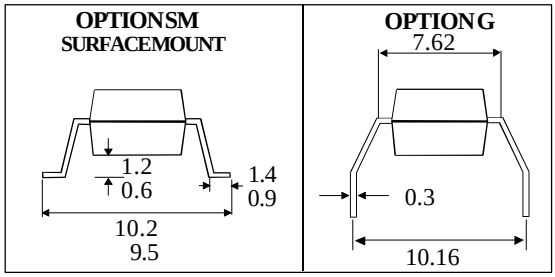
INPUT DIODE

Forward Current	20mA (2)
Reverse Voltage	5V
Enable Voltage	5.5V
(Not to exceed Vcc by more that 500mV)	

OUTPUT PHOTOTRANSISTOR

Supply Voltage Vcc	7V (1 Min Max)
Current - Io	25mA
Collector Power Dissipation	40mW
Collector Voltage - Vo	7V

All electrical parameters are 100 % tested
Specifications are guaranteed to a cumulative 0.65% AQL



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ELECTRICAL CHARACTERISTICS (Over recommended temperature 0°C to70°C unless specified)

PARAMETER	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	FIG	NOTE
High Level Output Current I_{OH}		7	250	µA	Vcc =5.5V, Vo = 5.5V. IF = 250µA VE= 2.0V		
Low Level Output Voltage V_{OL}		0.4	0.6	V	Vcc =5.5V, IF = 5mA, VE = 2.0V I_{0L} (sinking) = 13mA		
High Level Enable Current I_{EH}		-1.0		mA	Vcc =5.5V, VE = 2.0V		
Low Level Enable Current I_{EL}		-1.6	-2.0	mA	Vcc =5.5V, VE = 0.5V		
High Level Supply Current I_{CCH}		10	15	mA	Vcc =5.5V, IF = 0, VE = 0.5V		
Low Level Supply Current I_{CCL}		15	19	mA	Vcc =5.5V, IF =10 mA, VE = 0.5V		
Input - Output Insulation Leakage Current - I_{IO}			1.0	µA	Relative Humidity = 45% TA = 25 °C, t = 5s, VI0 = 3000 V DC mA,		3
Withstand Insulation Test Voltage V_{ISO}	2500			V	R_H < 50%, T_A = 25°C, t = 1 Min		3
Resistance - R_{IO}		10^{12}		ohm	VI0 = 500V, t = 5s, TA = 25 °C		3
Capacitance - C_{IO}		0.6		pF	f = 1MHz, TA = 25 °C		3
Input Forward Voltage - V_F		1.5	1.75	V	IF = 10mA, TA = 25°C		
Input Reverse Breakdown Voltage - B_{VR}	5			V	IR = 10 µA, TA = 25°C		
Input Capacitance - C_{IN}		60		pF	VF = 0, f, = 1MHz		
Current Transfer Ratio - CTR		700		%	IF= 5mA, RL= 100Ω		12
High Level Enable Voltage - V_{EH}	2.0			V	Vcc =5.5V, IF =10 mA		11
Low Level Enable Voltage - V_{EL}			0.8	V_{RMS}	Vcc =5.5V, IF =10 mA		11
Input Diode Temperature Coefficient $\frac{\Delta VF}{\Delta TA}$		-1.4			lF = 10mA,		

*All typicals are at V_{CC} = 5V, T_A = 25°C

1 Bypassing of the power supply line is required, with a 0.01 µ F ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be seperate from the bus for any active loads. Otherwise a larger value of bypass capacitor (up to 0.1 µ F)may be needed to supress regenerative feedback via the power supply.

2 Peaking circuits may produce transient input currents up to 50mA, 50ns maximum pulse width, provided average current does not exceed 20mA

3 Device considered a two terminal device; pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

4 The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

5 The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.

6 The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

7 The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.

8 CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (ie Vout> 2.0V).

9 CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (ie Vout< 0.8V)

10 For sinusoidal voltages $\left(\frac{dv_{CM}}{dt}\right)_{max} = \pi f_{CM} V_{CM}(p\text{-}p)$

11 No external pull up is required for a high logic state on the enable input.

12 DC current transfer ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.

SWITCHING CHARACTERISTICS (AT T_A = 25°C, V_{CC} = 5V)

PARAMETER	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	FIG	NOTE
Propagation Delay to High Output Level - t_{PLH}		35	75	ns	R_L = 350Ω C_L = 15pF, 1_F = 7.5mA		4
Propagation Delay Time to Low Output Level - t_{PHL}		39	75	ns	R_L = 350Ω C_L = 15 pF, I_F = 7.5mA		5
Output rise time (10 -90%) - t_r		27		ns	R_L =350ΩC_L = 15pF I_F= 7.5mA		
Output Fall Time (90 - 10% - t_f		16		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL} - t_{ELH}		25		ns	R_L = 350Ω C_L = 15pF, I_F= 7.5mA, V_{EH} = 3.0V, V_{EL} = 0		6
Propagation Delay time of Enable from V_{EL} to to V_{EH} - t_{EHL}		14		ns	R_L = 350 Ω C_L = 15 pF, I_F = 7.5mA, V_{EH} = 3.0V, V_{EL} = 0		7
Common Mode Transient Immunity at High Output Level -CM_H		12000		V/µs	V_{CM} =400V (peak), R_L = 350Ω I_F = 0mA, Vo (min) = 2V		8,10
Common Mode Transient Immunity at Low Output Level - CM_L		11000		V/µs	V_{CM} = 400V (peak) R_L = 350Ω I_F = 7.5mA, Vo (max) = 0.8V		9,10

RECOMMENDED OPERATING CONDITIONS

	SYM	MIN	MAX	UNITS
Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	6.3*	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL)	N		8	
Operating Temperature	T_A	0	70	°C

*6.3mA condition permits at least 20% CTR degradation guardband
Initial switching threshold is 5mA or less

TEST CIRCUIT FOR t_{PHL} AND t_{PLH}