

### 32K x 16 LOW VOLTAGE CMOS STATIC RAM

**NOVEMBER 1997** 

#### **FEATURES**

- High-speed access time: 10, 12, 15, and 20 ns
- CMOS low power operation
  - 150 mW (typical) operating
  - 150 μW (typical) standby
- · TTL compatible interface levels
- Single 3.3V ± 10% power supply
- Fully static operation: no clock or refresh required
- · Three state outputs
- Industrial temperature available
- Available in 44-pin 400-mil SOJ package and 44-pin TSOP (Type 2)

#### **DESCRIPTION**

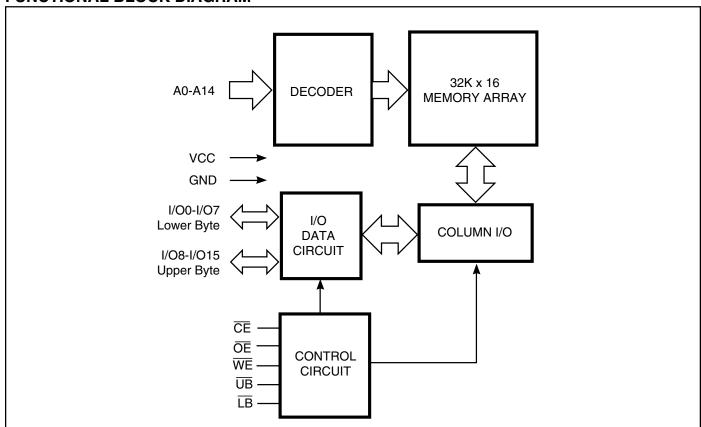
The *ISSI* IS61LV3216 is a high-speed, 512K static RAM organized as 32,768 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields fast access times with low power consumption.

When  $\overline{\text{CE}}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs,  $\overline{CE}$  and  $\overline{OE}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS61LV3216 is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type 2).

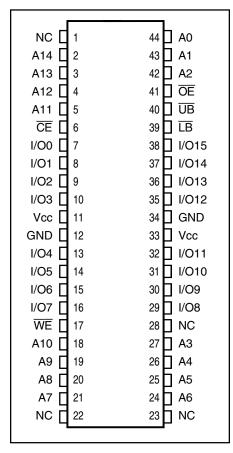
#### **FUNCTIONAL BLOCK DIAGRAM**



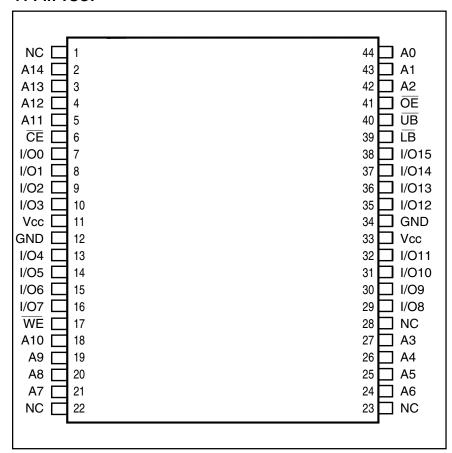
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# PIN CONFIGURATIONS 44-Pin SOJ



#### 44-Pin TSOP



#### **PIN DESCRIPTIONS**

A0-A14	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input

LB	Lower-byte Control (I/O0-I/O7)
ŪB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

#### **TRUTH TABLE**

						PIN	חוי		
Mode	WE	Œ	ŌĒ	LB	<del>UB</del>	1/00-1/07	I/O8-I/O15	Vcc Current	
Not Selected	Х	Н	Х	Х	Х	High-Z	High-Z	Isb1, Isb2	
Output Disabled	Н	L	Н	Х	Χ	High-Z	High-Z	Icc	
•	Χ	L	Χ	Н	Н	High-Z	High-Z		
Read	Н	L	L	L	Н	<b>D</b> оит	High-Z	Icc	
	Н	L	L	Н	L	High-Z	<b>D</b> out		
	Н	L	L	L	L	<b>D</b> ouт	<b>D</b> оит		
Write	L	L	Х	L	Н	DIN	High-Z	Icc	
	L	L	Χ	Н	L	High-Z	ĎіN		
	L	L	Χ	L	L	DIN	DIN		



#### ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage with Respect to GND	-0.5 to +4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
Тѕтс	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.0	W
Іоит	DC Output Current (LOW)	20	mA

#### Note:

 Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **OPERATING RANGE**

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 10%

### DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = Min., Iон = -4.0 mA	2.4	_	V
Vol	Output LOW Voltage	Vcc = Min., IoL = 8.0 mA	_	0.4	V
VIH	Input HIGH Voltage		2.2	Vcc + 0.3	V
VIL	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
Li	Input Leakage	GND - Vin - Vcc	-2	2	μA
ILO	Output Leakage	GND - Vout - Vcc, Outputs Disabled	-2	2	μΑ

#### Notes:

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

				-10	) ns	-12	ns ns	-15	ns	-20	ns	
Symbol	Parameter	<b>Test Conditions</b>		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Icc	Vcc Dynamic Operating Supply Current	Vcc = Max., lout = 0 mA, f = fmax	Com. Ind.	_	220 —	_	200 230	_	180 200	_	160 180	mA
ISB1	TTL Standby Current (TTL Inputs)	$\begin{aligned} & \text{Vcc} = \text{Max.}, \\ & \underline{\text{Vin}} = \text{ViH or Vil} \\ & \overline{\text{CE}} \bullet \text{ViH} , \ \ \text{f} = 0 \end{aligned}$	Com. Ind.	_	10 —	_	10 20	_	10 20	_	10 20	mA
ISB2	CMOS Standby Current (CMOS Inputs)	Vcc = Max., Œ • Vcc − 0.2V, Vin • Vcc − 0.2V, or Vin - 0.2V, f = 0	Com. Ind.	_	5 —	_	5 10	_	5 10	_	5 10	mA

#### Note:

<sup>1.</sup>  $V_{IL}$  (min.) = -3.0V for pulse width less than 10 ns.

<sup>1.</sup> At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.



#### CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	$V_{IN} = 0V$	6	pF
Соит	Input/Output Capacitance	Vout = 0V	8	pF

#### Note:

### READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

		-1	0	-12	2	-1:	 5	-2	0	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
trc	Read Cycle Time	10	_	12	_	15	_	20	_	ns
taa	Address Access Time	_	10	_	12	_	15	_	20	ns
tона	Output Hold Time	3	_	3	_	3	_	3	_	ns
tace	CE Access Time	_	10	_	12	_	15	_	20	ns
tdoe	OE Access Time	_	5	_	6	_	7	_	8	ns
thzoe(2)	OE to High-Z Output	0	5	0	6	0	7	0	8	ns
tLZOE <sup>(2)</sup>	OE to Low-Z Output	0	_	0	_	0	_	0	_	ns
thzce(2	CE to High-Z Output	0	5	0	6	0	7	0	8	ns
tLZCE <sup>(2)</sup>	CE to Low-Z Output	4	_	4	_	4	_	4	_	ns
<b>t</b> BA	LB, UB Access Time	_	5	_	6	_	7	_	8	ns
<b>t</b> HZB	LB, UB to High-Z Output	0	5	0	6	0	7	0	8	ns
tızı	LB, UB to Low-Z Output	5	_	5	_	5	_	5	_	ns

#### Notes:

#### **AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

#### **AC TEST LOADS**

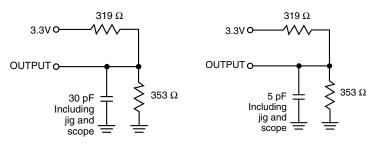


Figure 1a.

Figure 1b.

<sup>1.</sup> Tested initially and after any design or process changes that may affect these parameters.

<sup>1.</sup> Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.

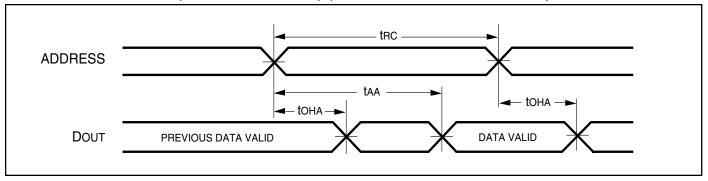
<sup>2.</sup> Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

<sup>3.</sup> Not 100% tested.

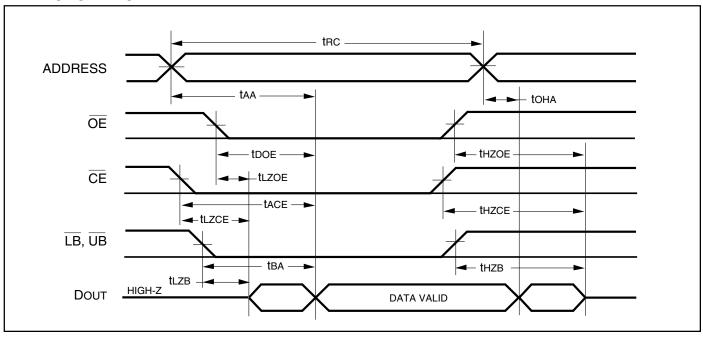


#### **AC WAVEFORMS**

### **READ CYCLE NO.** $1^{(1,2)}$ (Address Controlled) ( $\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{UB}$ or $\overline{LB} = V_{IL}$ )



### **READ CYCLE NO. 2<sup>(1,3)</sup>**



- Notes:
  1. WE is HIGH for a Read Cycle.
- 2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{UB}$ , or  $\overline{LB}$  = V<sub>IL</sub>.
- 3. Address is valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.



### WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

		-1	0	-1:	2	-1	5	-20	)	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	10	_	12	_	15	_	20	_	ns
tsce	CE to Write End	9	_	10	_	11	_	12	_	ns
taw	Address Setup Time to Write End	9	_	10	_	11	_	12	_	ns
tha	Address Hold from Write End	0	_	0	_	0	_	0	_	ns
tsa	Address Setup Time	0	_	0	_	0	_	0	_	ns
<b>t</b> PWB	LB, UB Valid to End of Write	9	_	10	_	11	_	12	_	ns
<b>t</b> PWE	WE Pulse Width	7	_	8	_	10	_	11	_	ns
tsp	Data Setup to Write End	5	_	6	_	7	_	_	8	ns
<b>t</b> HD	Data Hold from Write End	0	_	0	_	0	_	0	_	ns
thzwe <sup>(2)</sup>	WE LOW to High-Z Output	_	5	_	6	_	7	_	8	ns
tLZWE <sup>(2)</sup>	WE HIGH to Low-Z Output	1	_	1	_	1	_	1	_	ns

#### Notes:

<sup>1.</sup> Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.

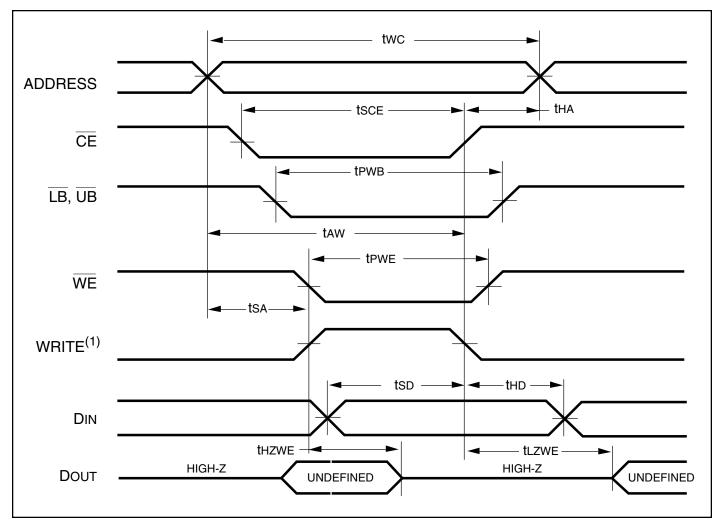
<sup>2.</sup> Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

<sup>3.</sup> The internal write time is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{UB}}$  or  $\overline{\text{LB}}$ , and  $\overline{\text{WE}}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.



#### **AC WAVEFORMS**

## WRITE CYCLE NO. 1 (WE Controlled)(1,2)



#### Notes:

- 1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  inputs and at least one of the  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  inputs being in the LOW state.
- 2. WRITE =  $(\overline{CE})$  [  $(\overline{LB})$  =  $(\overline{UB})$  ]  $(\overline{WE})$ .

IS61LV3216



#### ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61LV3216-10T	Plastic TSOP (Type 2)
10	IS61LV3216-10K	400-mil Plastic SOJ
12	IS61LV3216-12T	Plastic TSOP (Type 2)
12	IS61LV3216-12K	400-mil Plastic SOJ
15	IS61LV3216-15T	Plastic TSOP (Type 2)
15	IS61LV3216-15K	400-mil Plastic SOJ
20	IS61LV3216-20T	Plastic TSOP (Type 2)
20	IS61LV3216-20K	400-mil Plastic SOJ

#### ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61LV3216-12TI	Plastic TSOP (Type 2)
12	IS61LV3216-12KI	400-mil Plastic SOJ
15	IS61LV3216-15TI	Plastic TSOP (Type 2)
15	IS61LV3216-15KI	400-mil Plastic SOJ
20	IS61LV3216-20TI	Plastic TSOP (Type 2)
20	IS61LV3216-20KI	400-mil Plastic SOJ

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