IS61VPD51232
IS61VPD51236
IS61VPD10018

ISSI®

512K x 32, 512K x 36, 1024K x 18 SYNCHRONOUS PIPELINED, DOUBLE CYCLE DESELECT STATIC RAM

ADVANCE INFORMATION
MAY 2001

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +2.5V, ±5% operation
- Auto Power-down during deselect
- Double cycle deselect
- Snooze MODE for reduced-power standby
- JTAG Boundary Scan for PBGA package

DESCRIPTION

The *ISSI* IS61VPD51232, IS61VPD51236, and IS61VPD10018 are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61VPD51232 is organized as 524,288 words by 32 bits and the IS61VPD51236 is organized as 524,288 words by 36 bits. The IS61VPD10018 is organized as 1,048,576 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$).input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

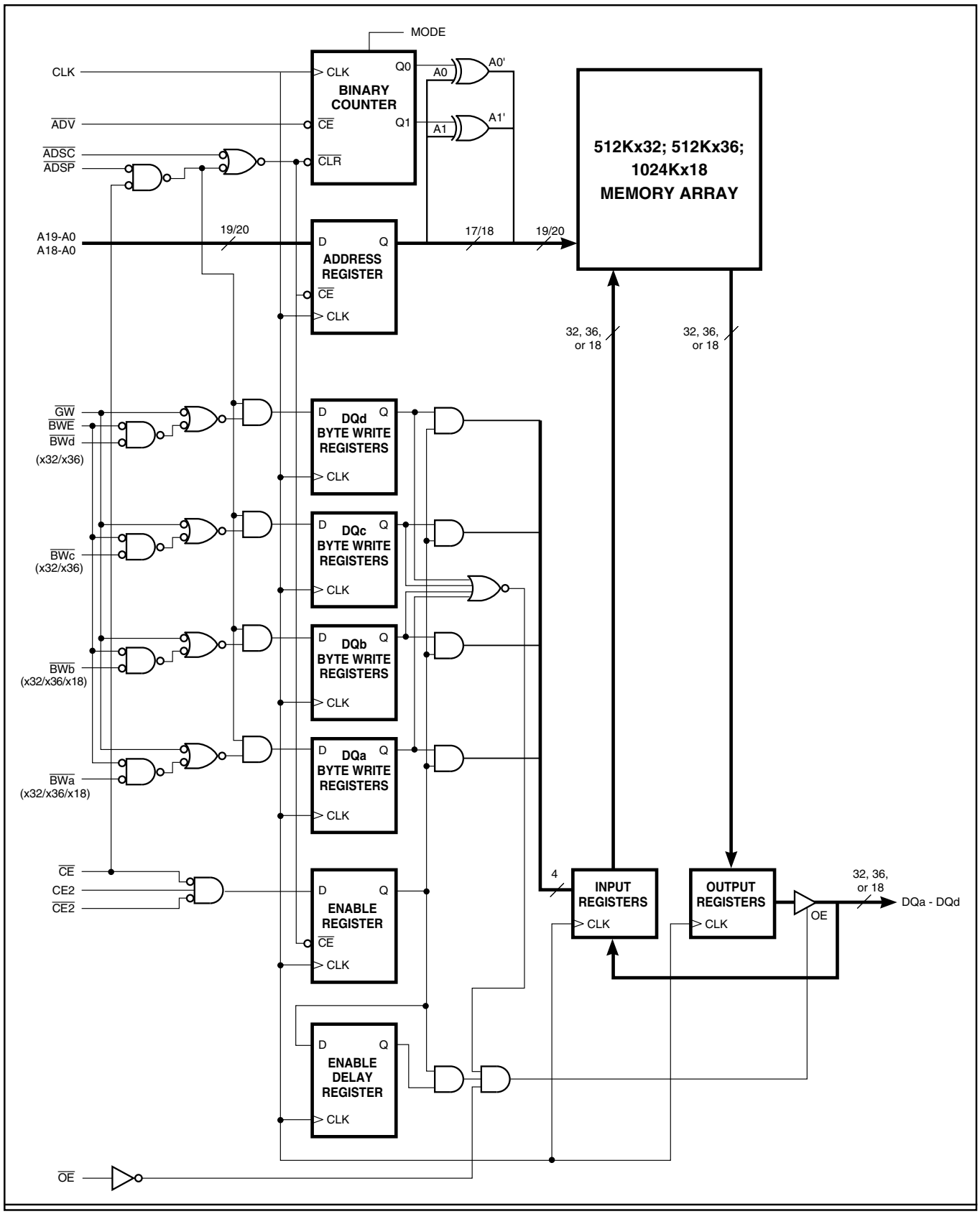
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

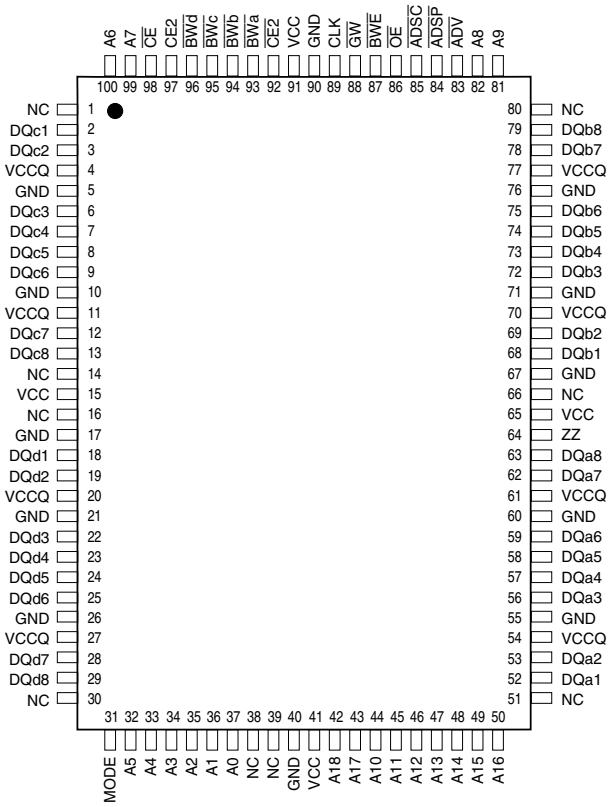
Symbol	Parameter	-200	-166	Units
t_{KQ}	Clock Access Time	3.1	3.5	ns
t_{KC}	Cycle Time	5	6	ns
	Frequency	200	166	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin TQFP



512K x 32

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
CLK	Synchronous Clock

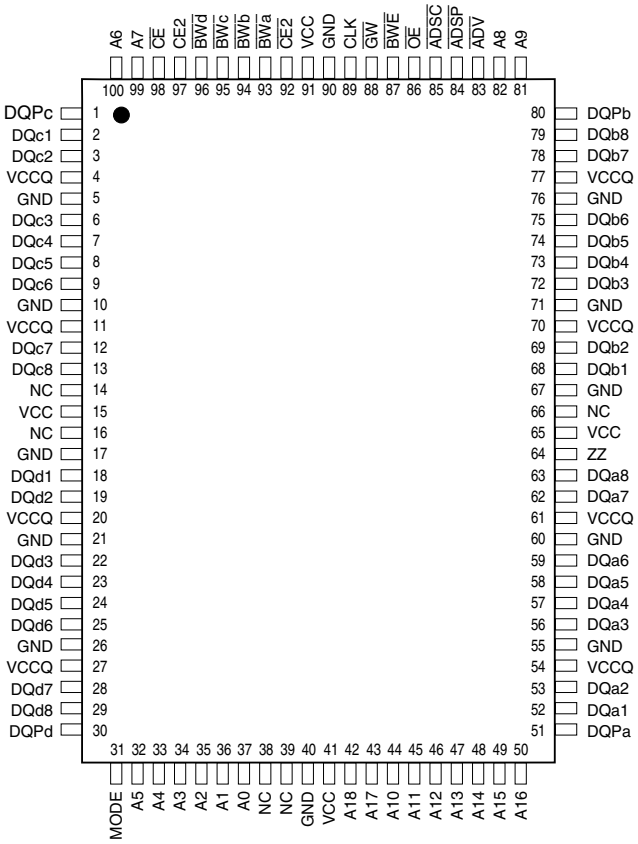
DQa-DQd	Synchronous Data Input/Output
GND	Ground
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
V_{CC}	+2.5V Power Supply
V_{CCQ}	Isolated Output Buffer Supply: +2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	$\overline{ADSP}$	A8	A16	VCCQ
B	NC	A18	A3	$\overline{ADSC}$	A9	A17	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQc1	DQPc	GND	NC	GND	DQPb	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VCCQ
G	DQc5	DQc6	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BWd}$	NC	$\overline{BWa}$	DQa5	DQa6
M	VCCQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VCCQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	DQPd	GND	A0	GND	DQPa	DQa1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	VCCQ	TMS	TDI	TCK	TDO	NC	VCCQ

100-Pin TQFP



512K x 36

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQd	Synchronous Data Input/Output

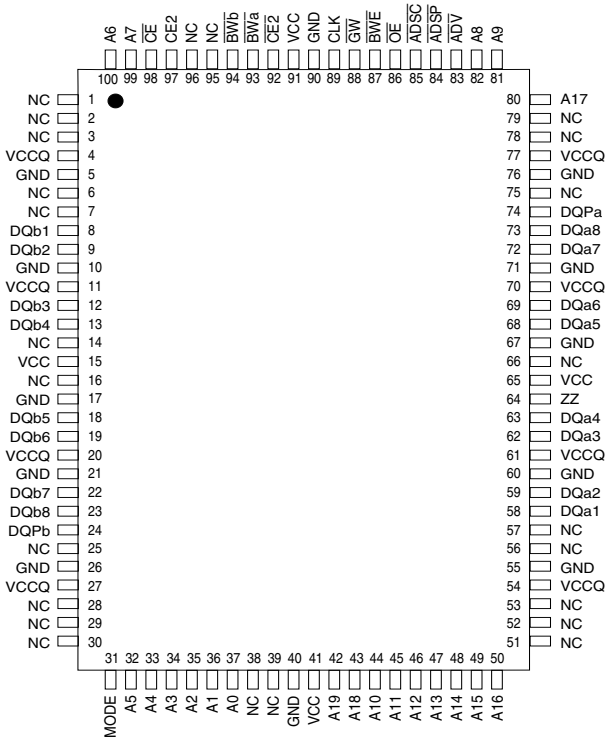
DQPa-DQPd	Parity Data Input/Output
GND	Ground
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
TMS, TDI, TCK, TDO	JTAG Boundary Scan Pins
V_{CC}	+2.5V Power Supply
V_{CCQ}	Isolated Output Buffer Supply: +2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	$\overline{ADSP}$	A8	A16	VCCQ
B	NC	A19	A3	$\overline{ADSC}$	A9	A18	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQb1	NC	GND	NC	GND	DQPa	NC
E	NC	DQb2	GND	$\overline{CE}$	GND	NC	DQa8
F	VCCQ	NC	GND	$\overline{OE}$	GND	DQa7	VCCQ
G	NC	DQb3	BWb	$\overline{ADV}$	GND	NC	DQa6
H	DQb4	NC	GND	$\overline{GW}$	GND	DQa5	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	NC	DQb5	GND	CLK	GND	NC	DQa4
L	DQb6	NC	GND	NC	BWa	DQa3	NC
M	VCCQ	DQb7	GND	$\overline{BWE}$	GND	NC	VCCQ
N	DQb8	NC	GND	A1	GND	DQa2	NC
P	NC	DQPb	GND	A0	GND	NC	DQa1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	A11	A10	NC	A14	A17	ZZ
U	VCCQ	TMS	TDI	TCK	TDO	NC	VCCQ

100-Pin TQFP



1024K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A19	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQd	Synchronous Data Input/Output

DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
GND	Ground
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
TMS, TDI, TCK, TDO	JTAG Boundary Scan Pins
Vcc	+2.5V Power Supply
VccQ	Isolated Output Buffer Supply: +2.5V
ZZ	Snooze Enable

TRUTH TABLE[1-8] (3CE option)

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

TRUTH TABLE[1-8] (1CE option)

NEXT CYCLE	ADDRESS	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE	$\overline{OE}$	DQ
Deselected	None	H	X	L	X	X	X	High-Z
Read, Begin	External	L	L	X	X	X	L	Q
Read, Begin	External	L	L	X	X	X	H	High-Z
Write, Begin	Current	L	H	L	X	Write	X	D
Read, Begin	External	L	H	L	X	Read	L	Q
Read, Begin	External	L	H	L	X	Read	H	High-Z
Read, Burst	Next	X	H	H	L	Read	L	Q
Read, Burst	Next	X	H	H	L	Read	H	High-Z
Read, Burst	Next	H	X	H	L	Read	L	Q
Read, Burst	Next	H	X	H	L	Read	H	High-Z
Write, Burst	Next	X	H	H	L	Write	X	D
Write, Burst	Next	H	X	H	L	Write	X	D
Read, Suspend	Current	X	H	H	H	Read	L	Q
Read, Suspend	Current	X	H	H	H	Read	H	High-Z
Read, Suspend	Current	H	X	H	H	Read	L	Q
Read, Suspend	Current	H	X	H	H	Read	H	High-Z
Write, Suspend	Current	X	H	H	H	Write	X	D
Write, Suspend	Current	H	X	H	H	Write	X	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

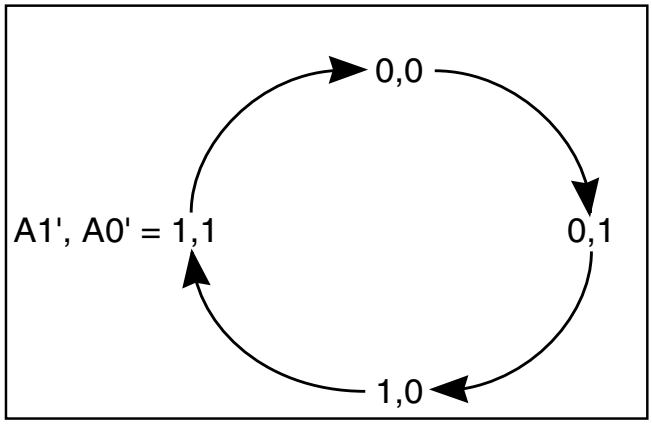
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = Vcc or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.5	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{CC} + 0.5	V
V_{CC}	Voltage on Vcc Supply Relatiive to GND	–0.5 to 3.2	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc	VccQ
Commercial	0°C to +70°C	2.375–2.625V	2.375–2.625V
Industrial	–40°C to +85°C	2.375–2.625V	2.375–2.625V

DC ELECTRICAL CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CCQ} = 2.5V		1.7	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, V_{CCQ} = 2.5V		—	0.7	V
V_{IH}	Input HIGH Voltage	V_{CCQ} = 2.5V		1.7	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CCQ} = 2.5V		–0.3	0.7	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CCQ}[2]	Com. Ind.	–2 –5	2 5	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CCQ}, $\overline{OE}$ = V_{IH}	Com. Ind.	–2 –5	2 5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-200 Max.	-166 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, Vcc = Max. Cycle Time ≥ t_{KC} min.	Com. Ind.	300 325	275 300	mA mA
I_{SB}	Standby Current	Device Deselected, Vcc = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.	Com. Ind.	70 80	60 70	mA mA

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to Vcc.
2. The MODE pin should be tied to Vcc or GND. It exhibits ±10 µA maximum leakage current when tied to - GND + 0.2V or ≥ Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	V_{CCQ}/2V
Output Load	See Figures 1 and 2

AC TEST LOADS

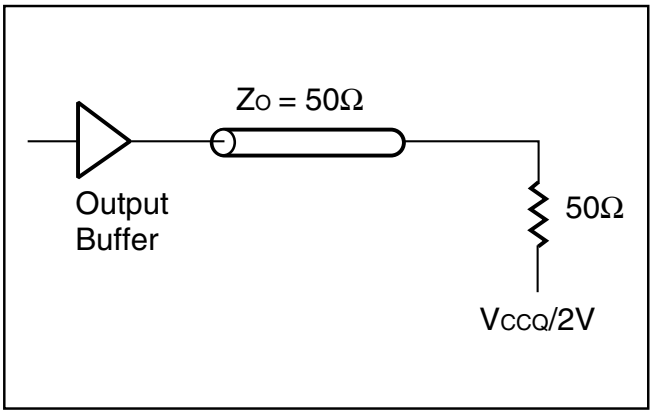


Figure 1

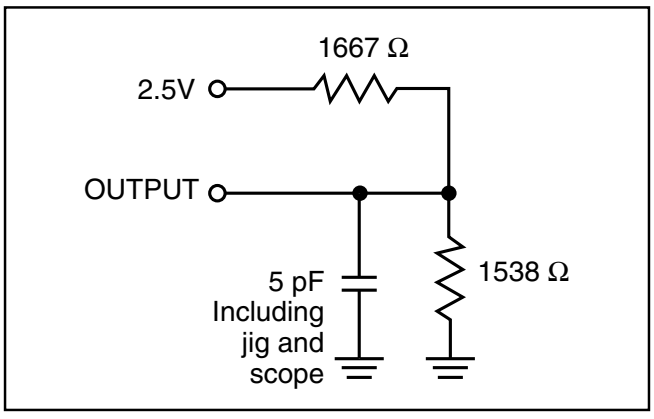


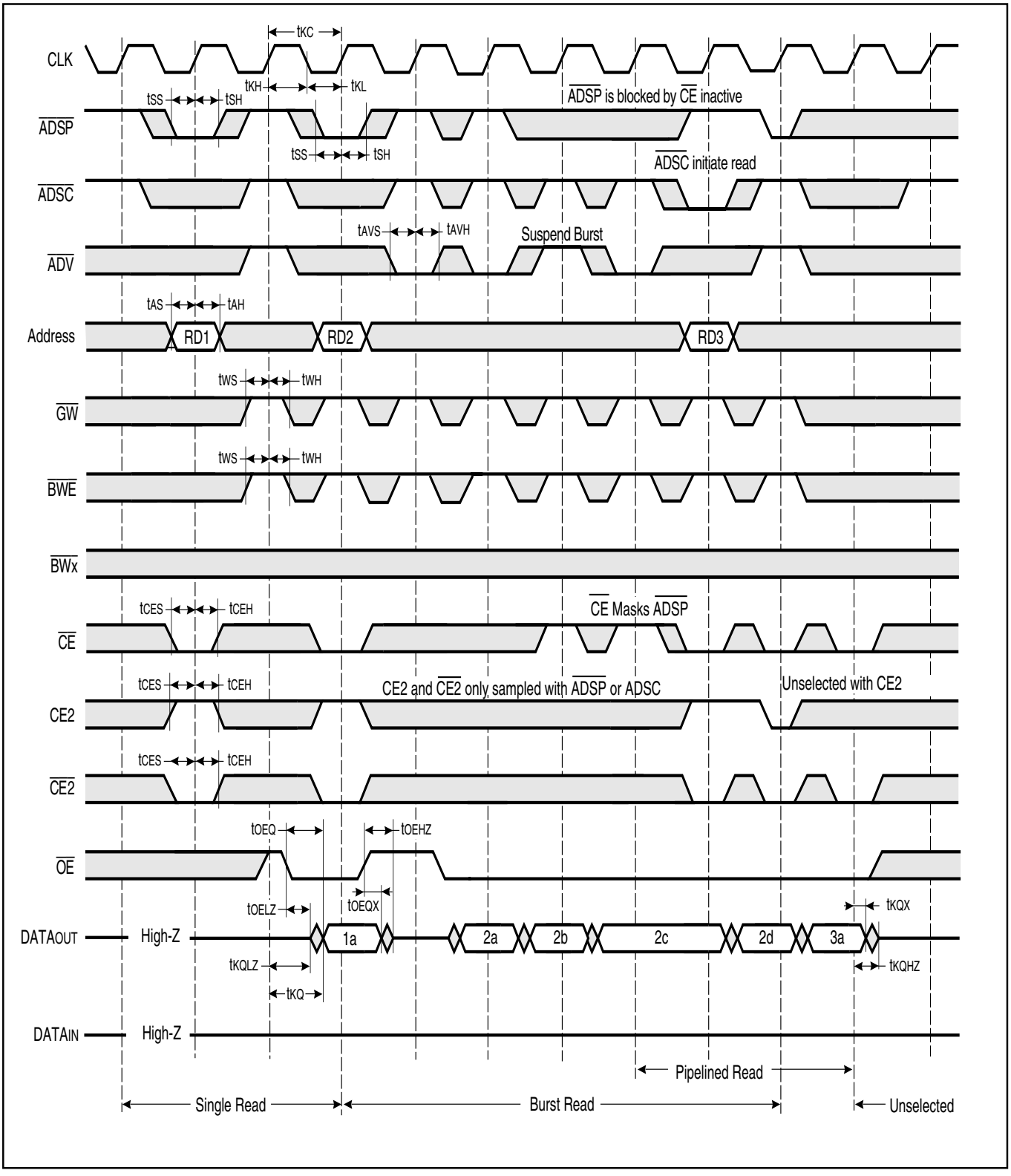
Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-200 Min.	-200 Max.	-166 Min.	-166 Max.	Unit
f_{MAX}	Clock Frequency	—	200	—	166	MHz
t_{KC}	Cycle Time	5	—	6	—	ns
t_{KH}	Clock High Pulse Width	2	—	2.3	—	ns
t_{KL}	Clock Low Pulse Width	2	—	2.3	—	ns
t_{KQ}	Clock Access Time	—	3.1	—	3.5	ns
t_{KQX}(1)	Clock High to Output Invalid	1.0	—	1.5	—	ns
t_{KQLZ}(1,2)	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}(1,2)	Clock High to Output High-Z	—	3.1	—	3.5	ns
t_{OEQ}	Output Enable to Output Valid	—	3.1	—	3.5	ns
t_{OELZ}(1,2)	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}(1,2)	Output Enable to Output High-Z	—	3.0	—	3.2	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

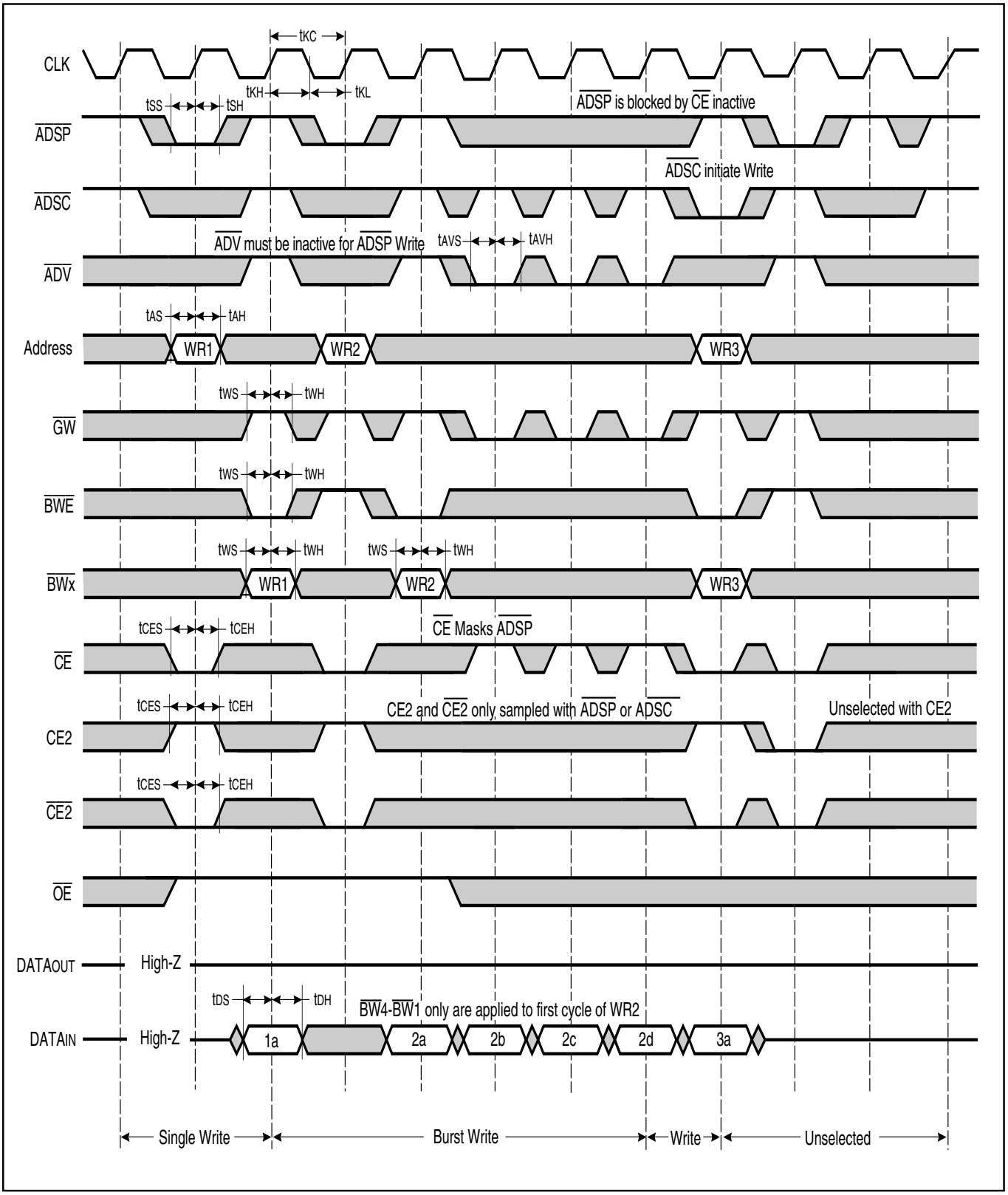
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-200		-166		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{KC}	Cycle Time	5	—	6	—	ns
t_{KH}	Clock High Pulse Width	2	—	2.3	—	ns
t_{KL}	Clock Low Pulse Width	2	—	2.3	—	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	ns
t_{DS}	Data In Setup Time	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data In Hold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns

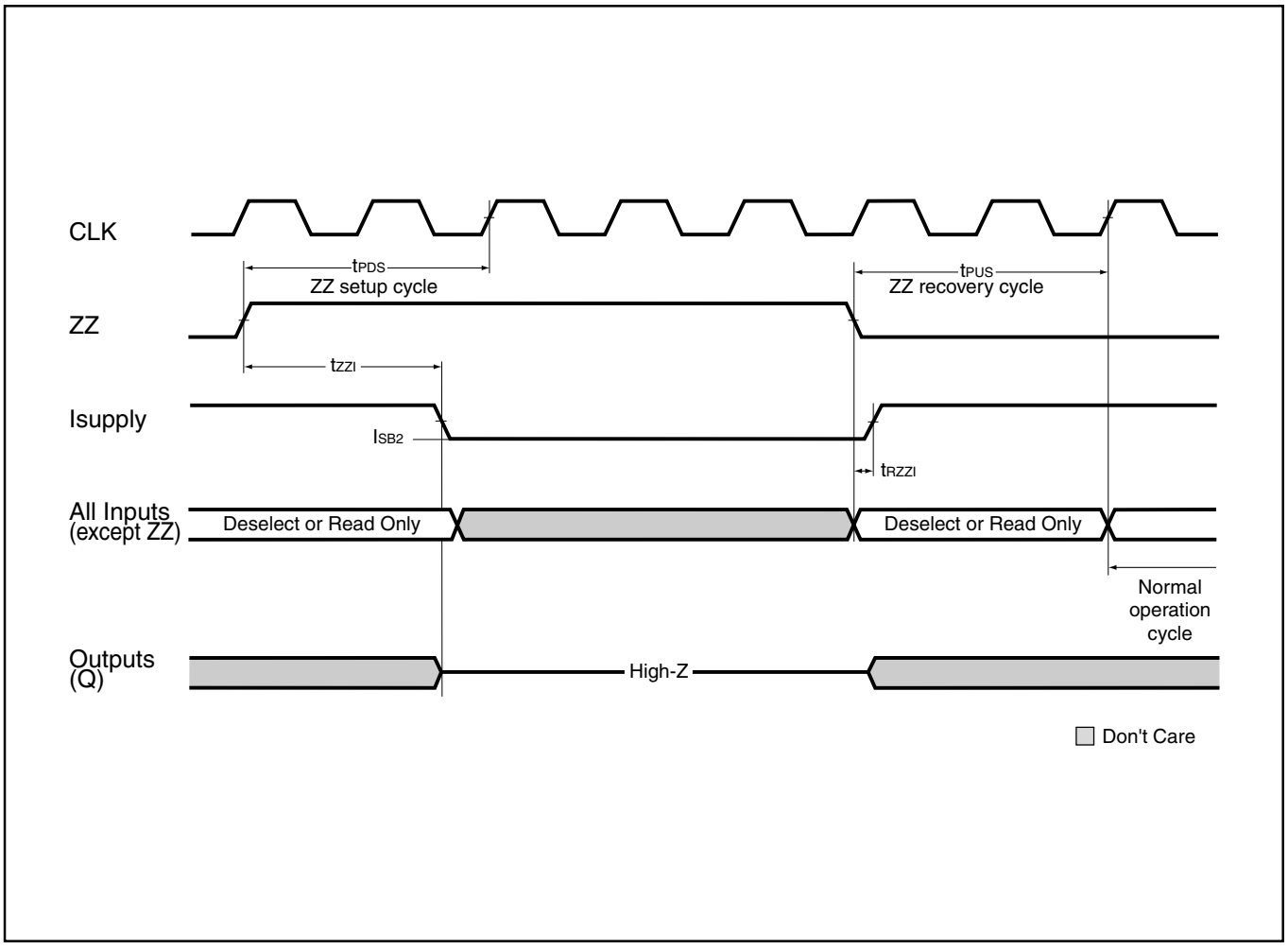
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ Vih	—	15	mA
t_{PDS}	ZZ active to input ignored		—	2	cycle
t_{PUS}	ZZ inactive to input sampled		2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0	—	ns

SNOOZE MODE TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The IS61VPS51236 and IS61VPS10018 have a serial boundary scan Test Access Port (TAP) in the PBGA package only. (Not available in TQFP package or with the IS61VPS51232.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (GND) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{CC} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

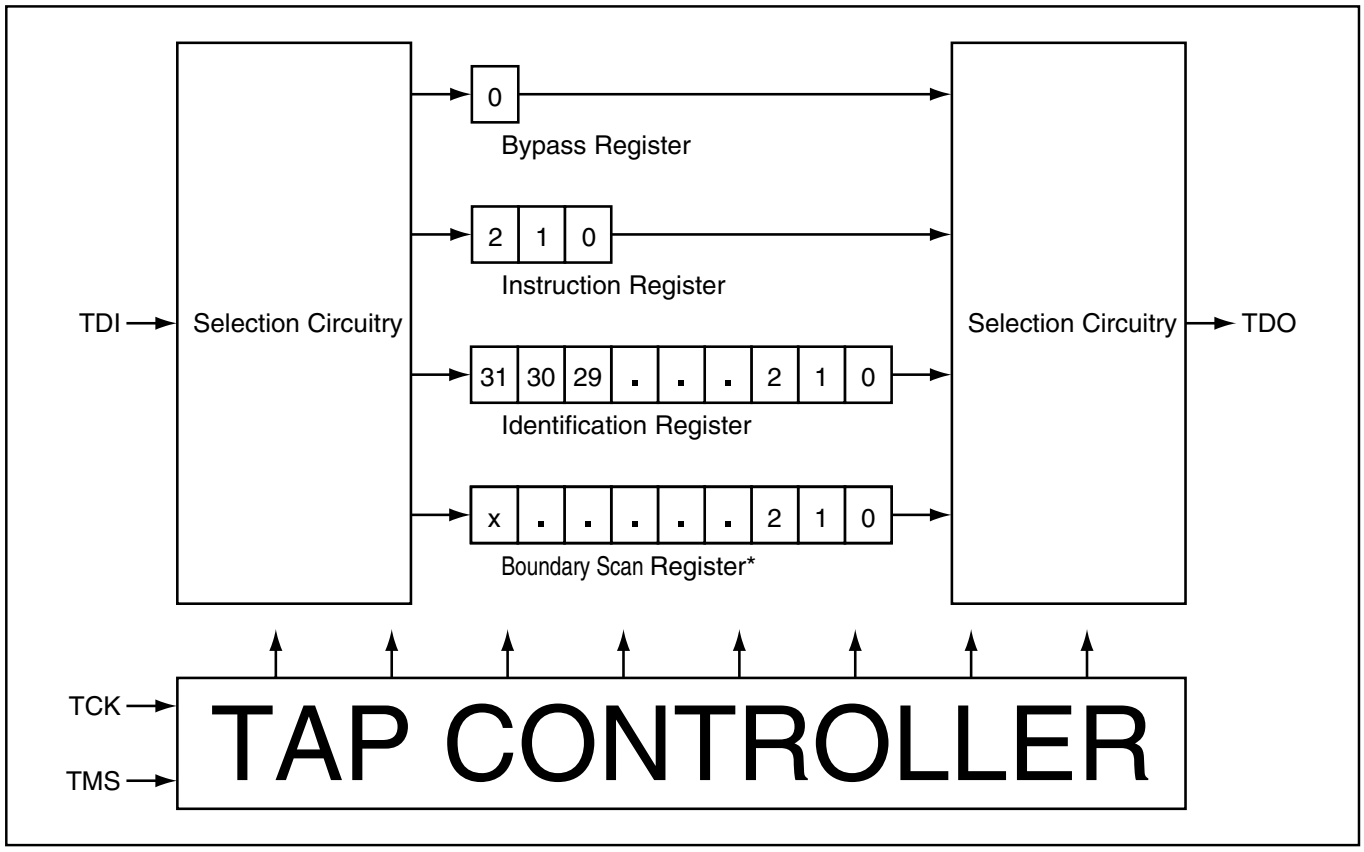
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{CC}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuit**ry.** Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (GND) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 70-bit-long register and the x18 configuration has a 51-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION REGISTER DEFINITIONS

Instruction Field	Description	512K x 36	1M x 18
Revision Number (31:28)	Reserved for version number.	xxxx	xxxx
Device Depth (27:23)	Defines depth of SRAM. 512K or 1M	00111	01000
Device Width (22:18)	Defines with of the SRAM. x36 or x18	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	xxxxx	xxxxx
ISSI JEDEC ID (11:1)	Allows unique identification of SRAM vendor.	00011010101	00011010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1

TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK and $\overline{CLK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

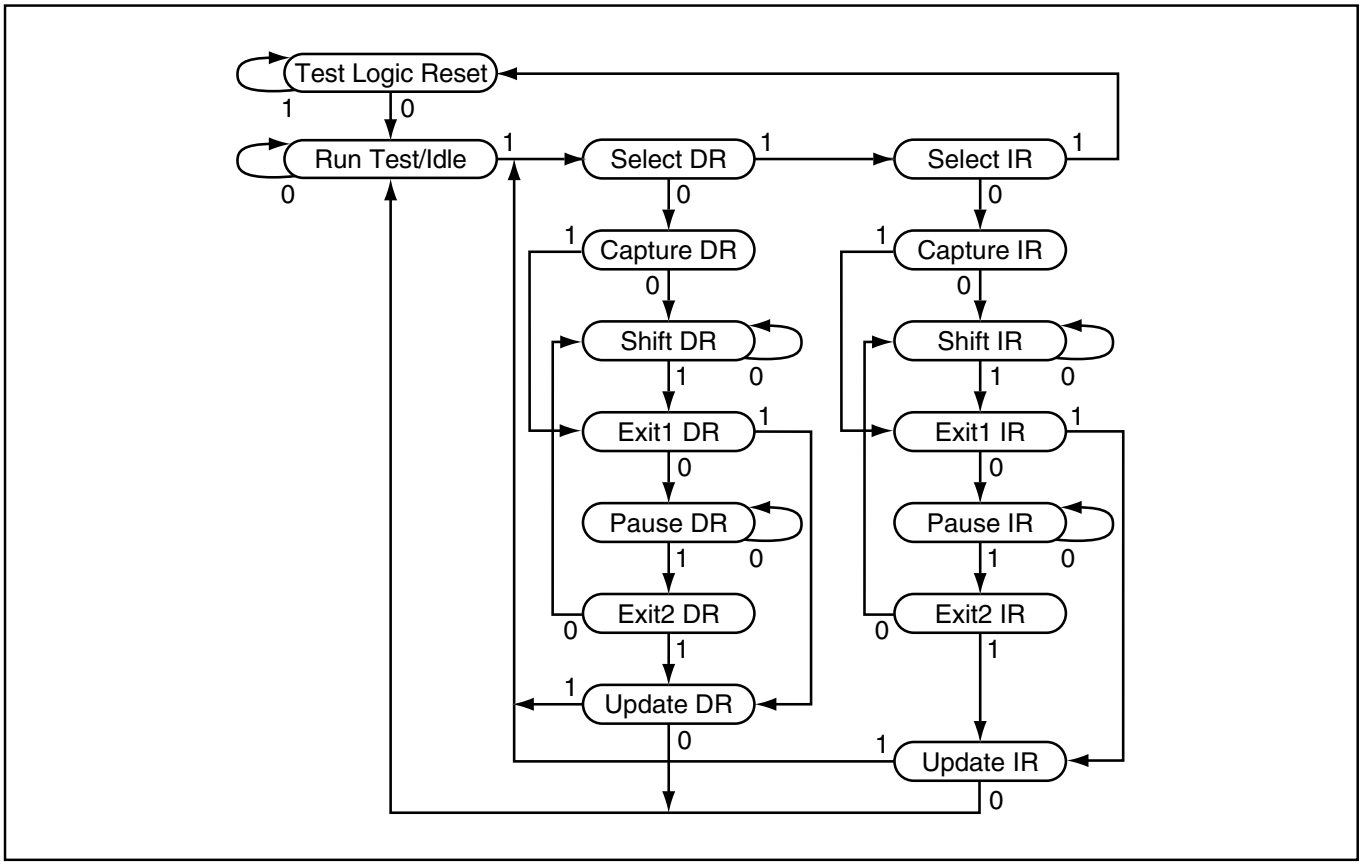
RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

INSTRUCTION CODES

Code	Instruction	Description
000	EXTEST	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
001	IDCODE	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
010	SAMPLE Z	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
011	RESERVED	Do Not Use: This instruction is reserved for future use.
100	SAMPLE/PRELOAD	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
101	RESERVED	Do Not Use: This instruction is reserved for future use.
110	RESERVED	Do Not Use: This instruction is reserved for future use.
111	BYPASS	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

TAP CONTROLLER STATE DIAGRAM



TAP Electrical Characteristics Over the Operating Range[1,2]

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.7	—	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 mA	2.1	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA	—	0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 mA	—	0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	I_{OLT} = 2mA	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V I ≤ V_{DDQ}	–5	5	mA

Notes:
1. All Voltage referenced to Ground.
2. Overshoot: V_{IH} (AC) ≤ V_{DD} +1.5V for t ≤ t_{TCYC}/2,
   Undershoot:V_{IL} (AC) ≤ 0.5V for t ≤ t_{TCYC}/2,
   Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

TAP AC ELECTRICAL CHARACTERISTICS[1] (OVER OPERATING RANGE)

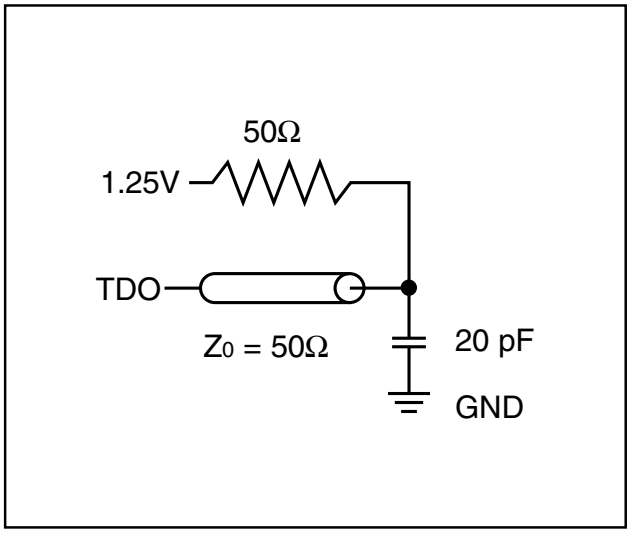
Symbol	Parameter	Min.	Max.	Unit
t_{TCYC}	TCK Clock cycle time	100	—	ns
f_{TF}	TCK Clock frequency	—	10	MHz
t_{TH}	TCK Clock HIGH	40	—	ns
t_{TL}	TCK Clock LOW	40	—	ns
t_{TMSS}	TMS setup to TCK Clock Rise	10	—	ns
t_{TDIS}	TDI setup to TCK Clock Rise	10	—	ns
t_{CS}	Capture setup to TCK Rise	10	—	ns
t_{TMSH}	TMS hold after TCK Clock Rise	10	—	ns
t_{TDIH}	TDI Hold after Clock Rise	10	—	ns
t_{CH}	Capture hold after Clock Rise	10	—	ns
t_{TDOV}	TCK LOW to TDO valid	—	20	ns
t_{TDOX}	TCK LOW to TDO invalid	0	—	ns

Notes:
7. t_{CS} and t_{CH}refer to the set-up and hold time requirements of latching data from the boundary scan register.
8. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

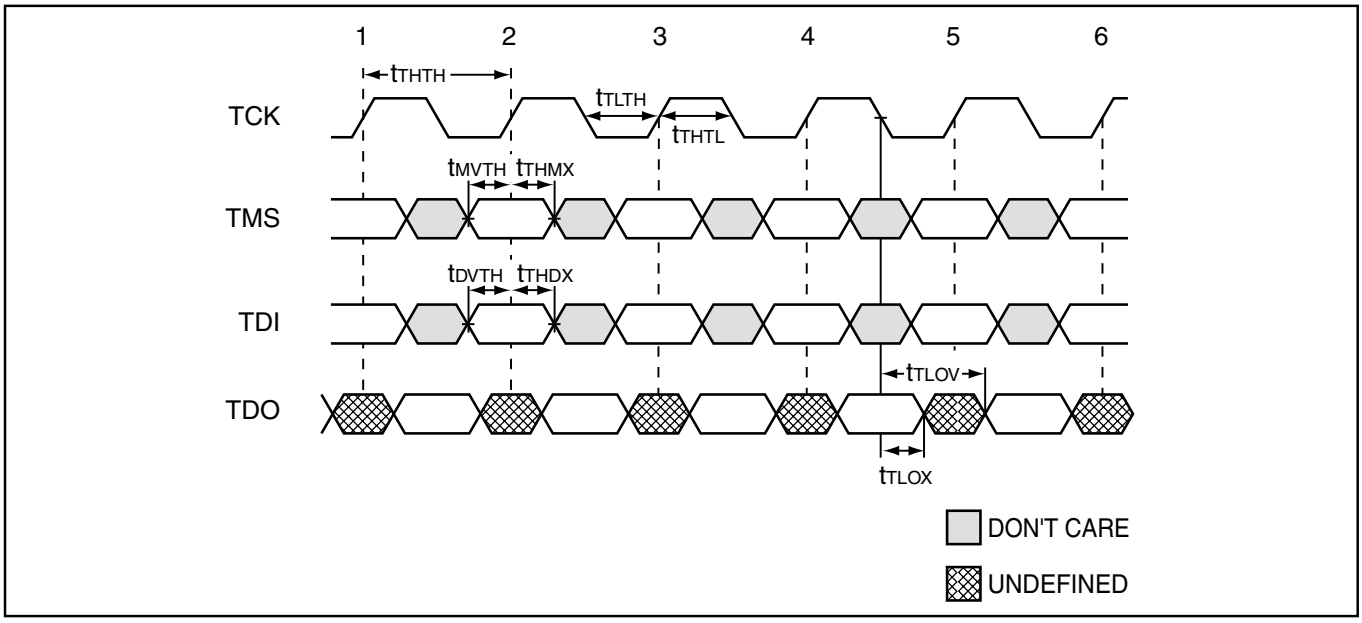
TAP AC TEST CONDITIONS

Input pulse levels	0 to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

TAP Output Load Equivalent



TAP TIMING



BOUNDARY SCAN ORDER (512K X 36)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	19	DQb	7G	37	BWa	5L	55	DQd	2K
2	A	3T	20	DQb	6F	38	BWb	5G	56	DQd	1L
3	A	4T	21	DQb	7E	39	BWc	3G	57	DQd	2M
4	A	5T	22	DQb	6D	40	BWd	3L	58	DQd	1N
5	A	6R	23	DQb	7H	41	A	2B	59	DQd	2P
6	A	3B	24	DQb	6G	42	CE	4E	60	DQd	1K
7	A	5B	25	DQb	6E	43	A	3A	61	DQd	2L
8	DQa	6P	26	DQb	7D	44	A	2A	62	DQd	2N
9	DQa	7N	27	A	6A	45	DQc	2D	63	DQd	1P
10	DQa	6M	28	A	5A	46	DQc	1E	64	MODE	3R
11	DQa	7L	29	ADV	4G	47	DQc	2F	65	A	2C
12	DQa	6K	30	ADSP	4A	48	DQc	1G	66	A	3C
13	DQa	7P	31	ADSC	4B	49	DQc	1D	67	A	5C
14	DQa	6N	32	OE	4F	50	DQc	1D	68	A	6C
15	DQa	6L	33	BWE	4M	51	DQc	2E	69	A1	4N
16	DQa	7K	34	GW	4H	52	DQc	2G	70	A0	4P
17	ZZ	7T	35	CLK	4K	53	DQc	1H			
18	DQb	6H	36	A	6B	54	NC	5R			

BOUNDARY SCAN ORDER (1M X 18)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	14	DQa	7G	27	CLK	4K	40	DQb	2K
2	A	2T	15	DQa	6F	27	A	6B	41	DQb	1L
3	A	3T	16	DQa	7E	29	BWa	5L	42	DQb	2M
4	A	5T	17	DQa	6D	30	BWb	3G	43	DQb	1N
5	A	6R	18	A	6T	31	A	2B	44	DQb	2P
6	A	3B	19	A	6A	32	CE	4E	45	MODE	3R
7	A	5B	20	A	5A	33	A	3A	46	A	2C
8	DQa	7P	21	ADV	4G	34	A	2A	47	A	3C
9	DQa	6N	22	ADSP	4A	35	DQb	1D	48	A	5C
10	DQa	6L	23	ADSC	4B	36	DQb	2E	49	A	6C
11	DQa	7K	24	OE	4F	37	DQb	2G	50	A1	4N
12	ZZ	7T	25	BWE	4M	38	DQb	1H	51	A0	4P
13	DQa	6H	26	GW	4H	39	NC	5R			

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
200 MHz	IS61VPD51232-200TQ	TQFP
166 MHz	IS61VPD51232-166TQ	TQFP

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
200 MHz	IS61VPD51232-200TQI	TQFP
166 MHz	IS61VPD51232-166TQI	TQFP

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
200 MHz	IS61VPD51236-200TQ	TQFP
	IS61VPD51236-200B	PBGA
166 MHz	IS61VPD51236-166TQ	TQFP
	IS61VPD51236-166B	PBGA

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
200 MHz	IS61VPD51236-200TQI	TQFP
	IS61VPD51236-200BI	PBGA
166 MHz	IS61VPD51236-166TQI	TQFP
	IS61VPD51236-166BI	PBGA

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
200 MHz	IS61VPD10018-200TQ	TQFP
	IS61VPD10018-200B	PBGA
166 MHz	IS61VPD10018-166TQ	TQFP
	IS61VPD10018-166B	PBGA

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
200 MHz	IS61VPD10018-200TQI	TQFP
	IS61VPD10018-200BI	PBGA
166 MHz	IS61VPD10018-166TQI	TQFP
	IS61VPD10018-166BI	PBGA

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