IS62V6416BLL

64K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

MARCH 2000

FEATURES

- Access time: 100 and 120 ns
- CMOS low power operation
- TTL compatible interface levels
- Single 2.7V-3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in Jedec Std 44-pin SOJ package, 44-pin TSOP (Type II), and 48-pin mini BGA

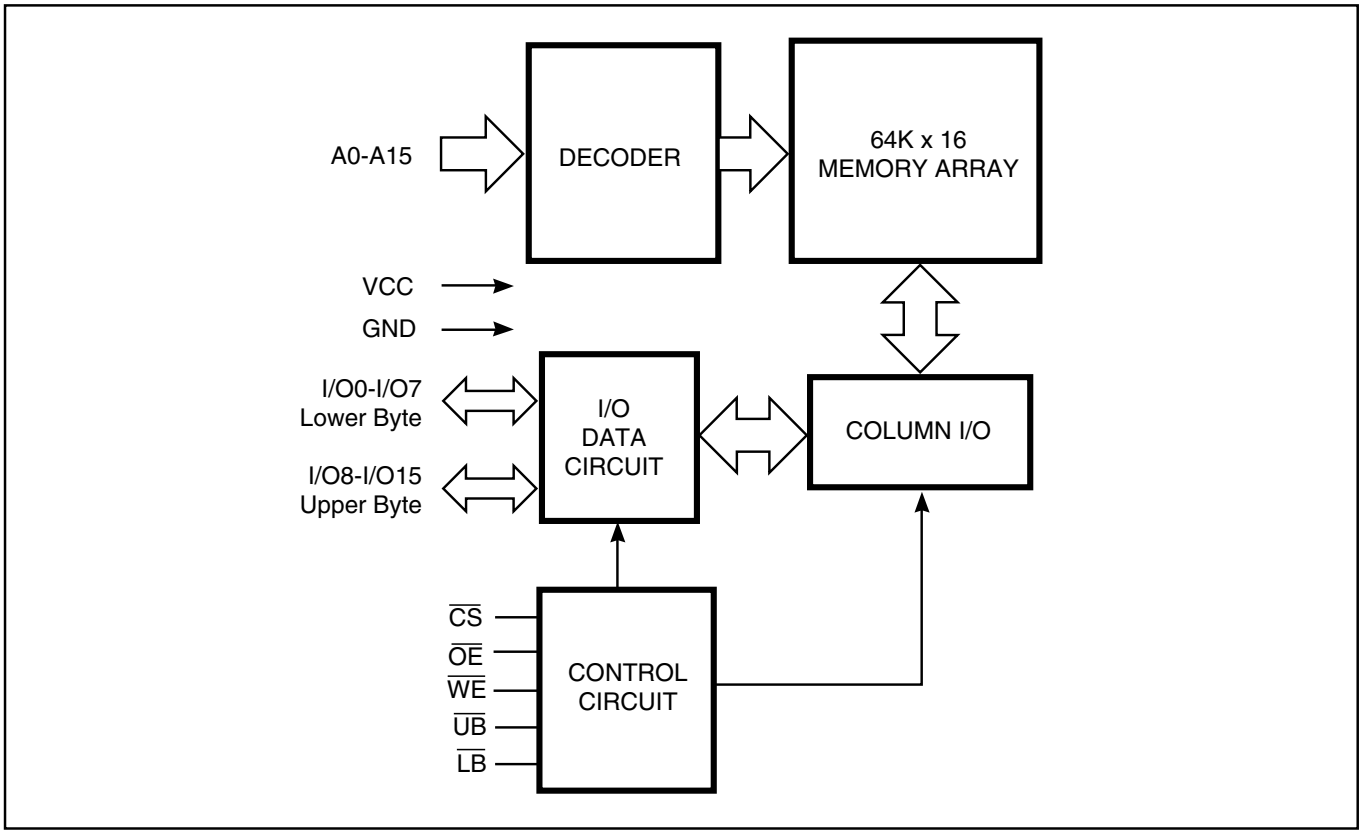
DESCRIPTION

The *ISSI* IS62V6416BLL is an ultra-low power, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques yields access times as fast as 100 ns with low power consumption.

When $\overline{CS}$ is HIGH (deselected) or when $\overline{CS}$ is LOW and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

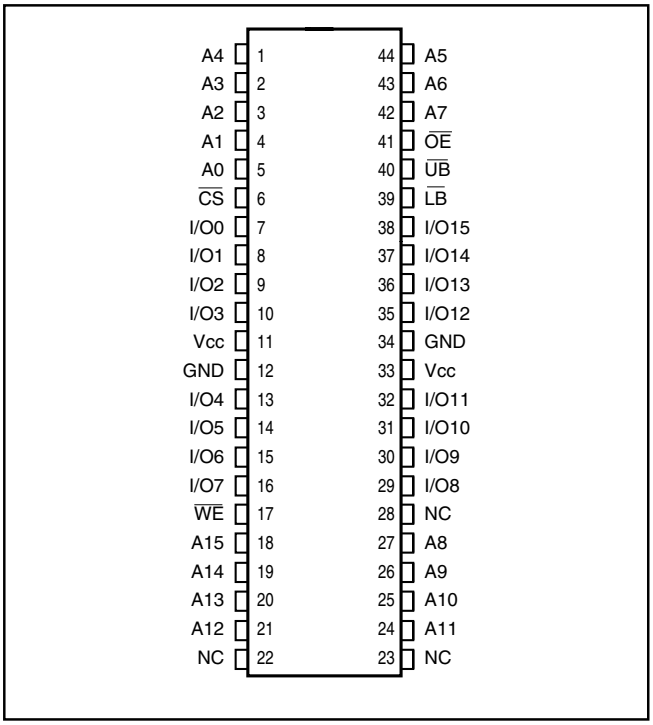
Easy memory expansion is provided by using Chip Select and Output Enable inputs, $\overline{CS}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

FUNCTIONAL BLOCK DIAGRAM

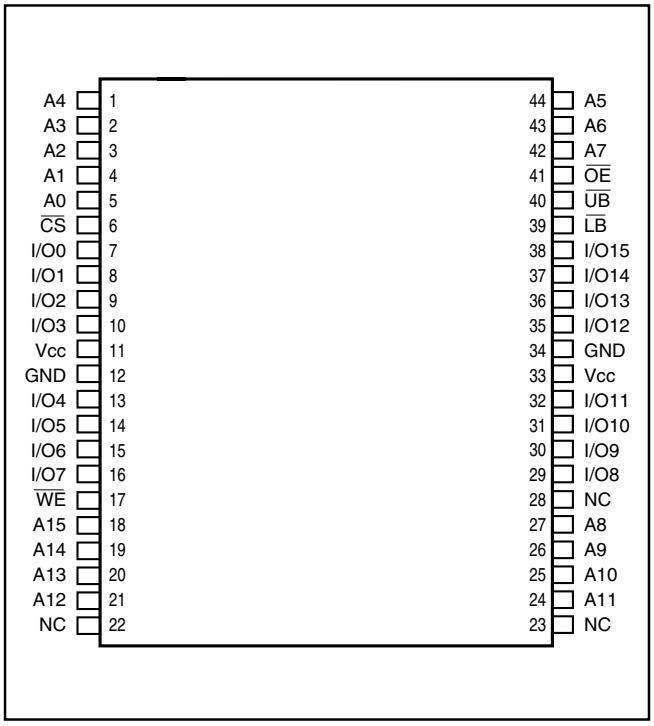


PIN CONFIGURATIONS

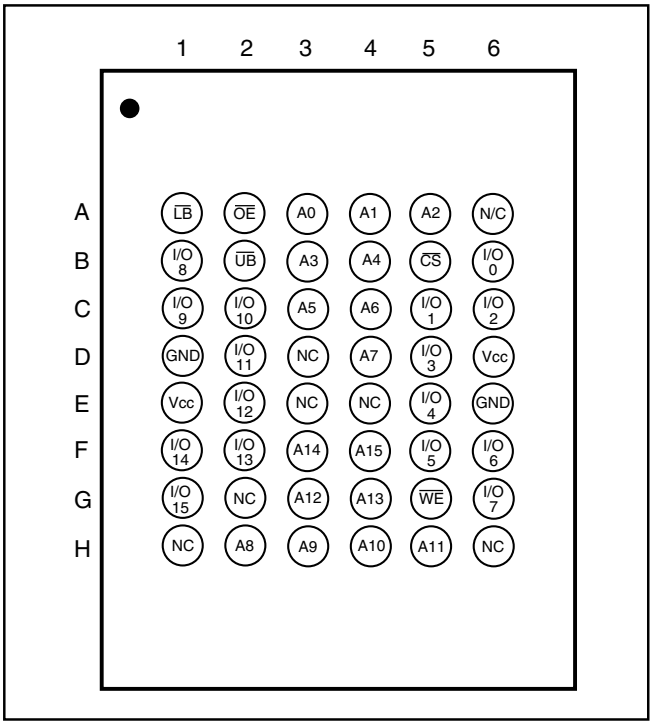
44-Pin SOJ



44-Pin TSOP



48-Pin mini BGA (Top View)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin I/O0-I/O7	I/O Pin I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	L	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	L	L	High-Z	High-Z	I_{CC}
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0 to 3V[1]
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V[1]
Output Load	See Figures 1 and 2

AC TEST LOADS

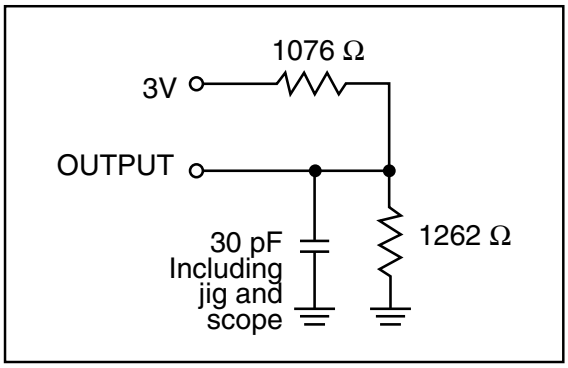


Figure 1.

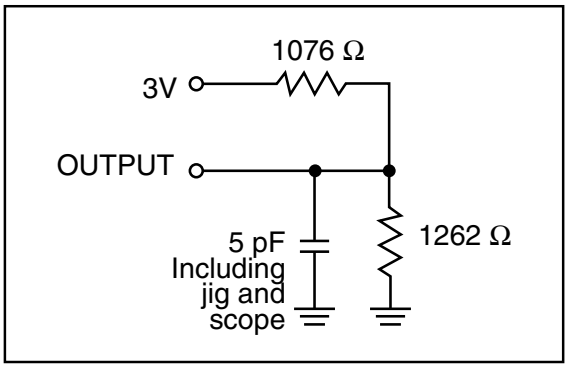


Figure 2.

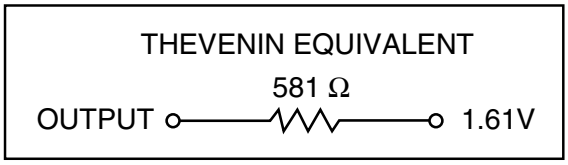


Figure 3.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V (Min.) to 3.3V (Max.)
Industrial	–40°C to +85°C	2.7V (Min.) to 3.3V (Max.)

DC ELECTRICAL CHARACTERISTICS (Over Operating Range Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA	2.2	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –1.5V for pulse width less than 30 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range Unless Otherwise Specified)

Symbol	Parameter	Test Conditions		-100 Min.	-100 Max.	-120 Min.	-120 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} $\overline{CS}$ = V_{IH}	Com.	—	35	—	30	mA
			Ind.	—	45	—	40	
$I_{SB}1$	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS}$ ≥ V_{IH}, f = 0	Com.	—	0.3	—	0.3	mA
			Ind.	—	0.3	—	0.3	
	OR							
	ULB Control	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}						
$I_{SB}2$	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} – 0.2V V_{IN} ≤ 0.2V, f = 0	Com.	—	5	—	5	µA
			Ind.	—	5	—	5	
	OR							
	ULB Control	V_{CC} = Max., $\overline{CS}$ = V_{IL} V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{CC} – 0.2V						

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency; f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

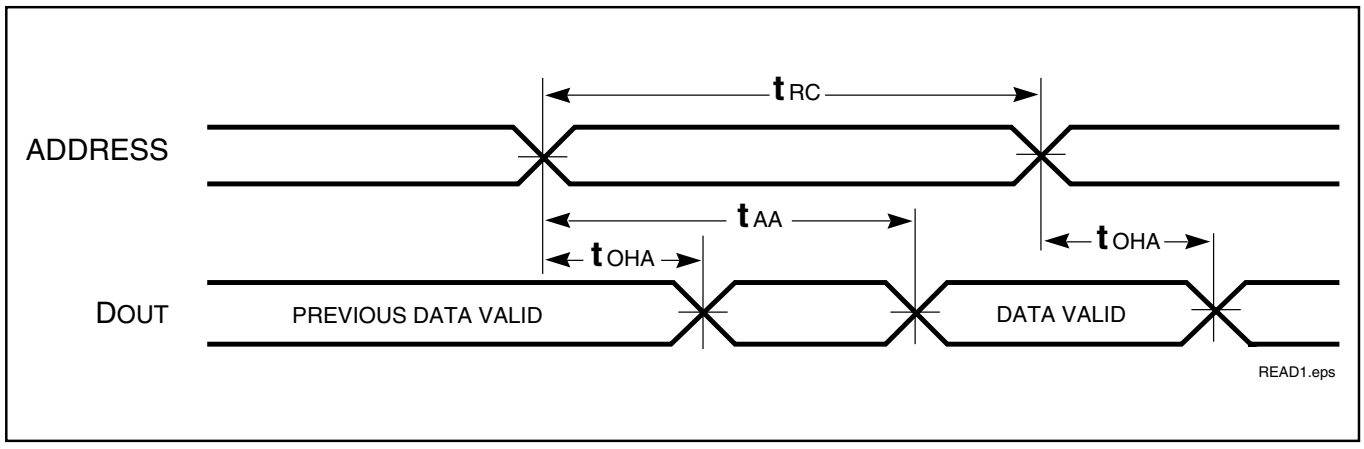
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-100 Min.	-100 Max.	-120 Min.	-120 Max.	Unit
t_{RC}	Read Cycle Time	100	—	120	—	ns
t_{AA}	Address Access Time	—	100	—	120	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS}	$\overline{CS}$ Access Time	—	100	—	120	ns
t_{DOE}	$\overline{OE}$ Access Time	—	50	—	70	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	30	0	35	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS}[2]	$\overline{CS}$ to High-Z Output	0	30	0	35	ns
t_{LZCS}[2]	$\overline{CS}$ to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	100	—	120	ns
t_{HZB}[2]	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	40	0	45	ns
t_{LZB}[2]	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	10	—	10	—	ns

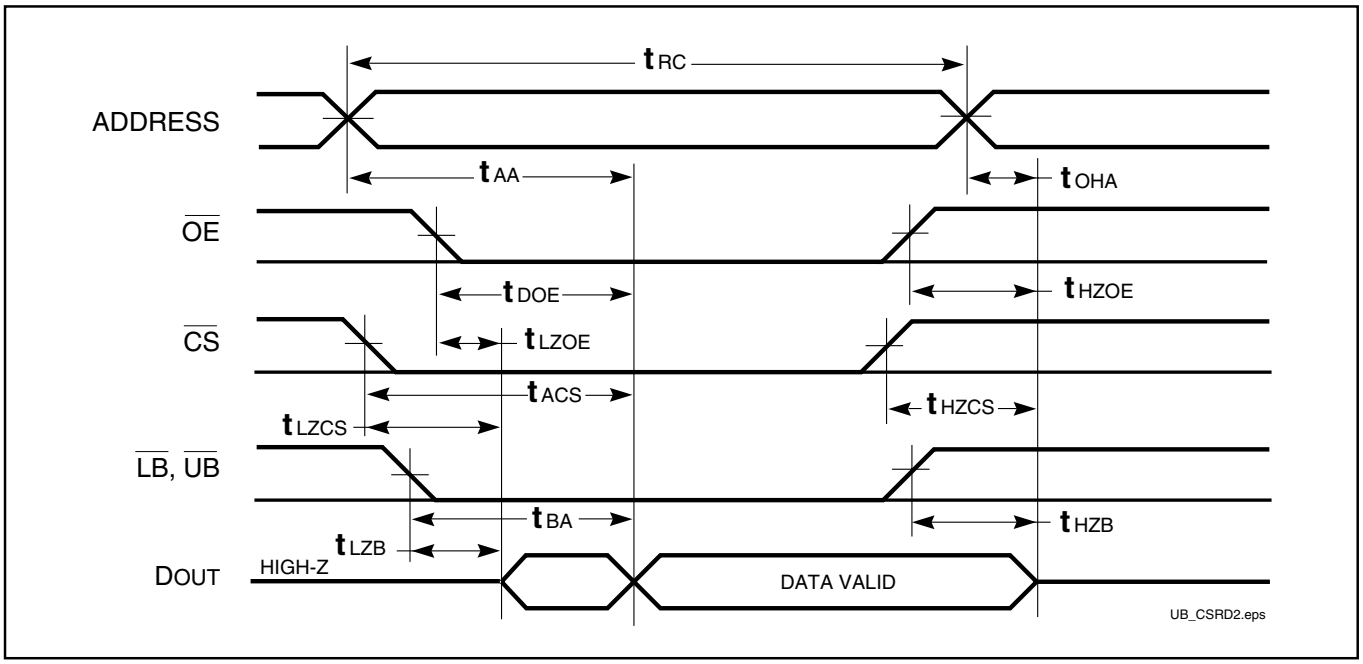
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ / $\overline{LB}$ Controlled)



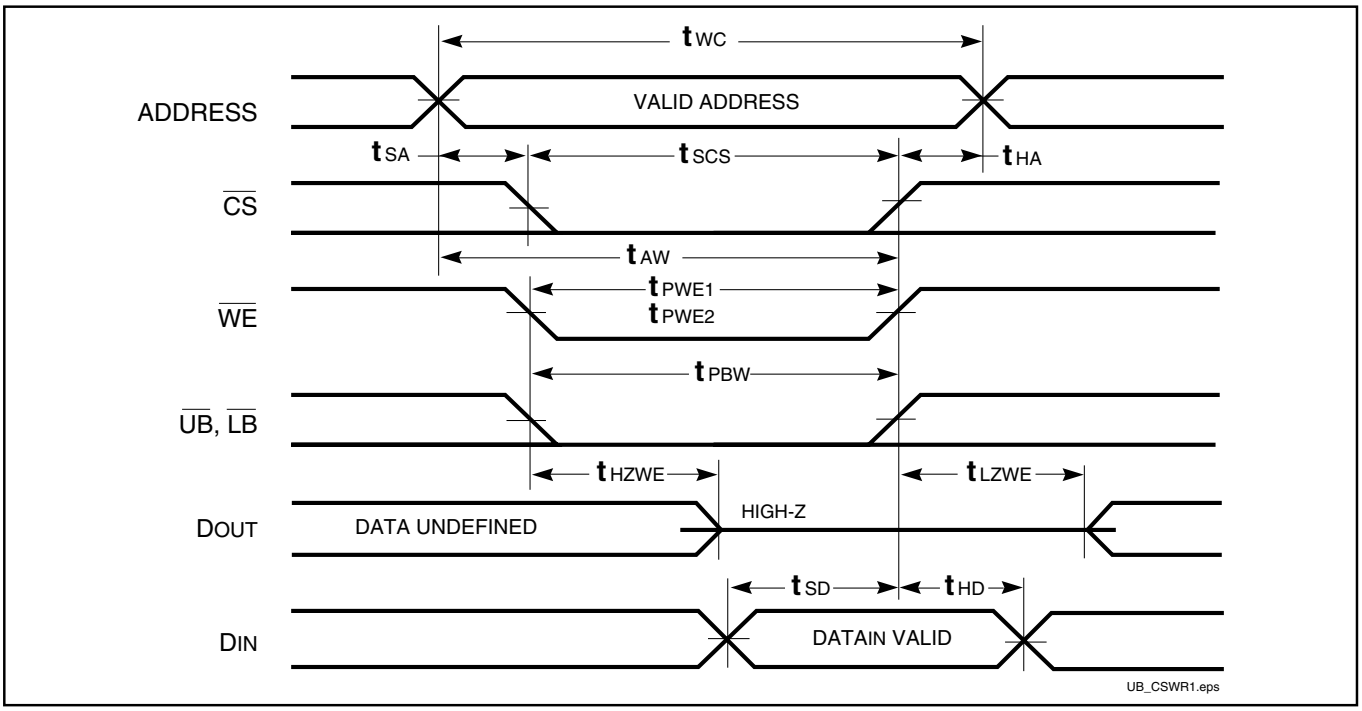
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CS}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-100 Min.	-100 Max.	-120 Min.	-120 Max.	Unit
t_{WC}	Write Cycle Time	100	—	120	—	ns
t_{SCS}	$\overline{CS}$ to Write End	80	—	100	—	ns
t_{AW}	Address Setup Time to Write End	80	—	100	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	80	—	100	—	ns
$t_{PWE1,2}$	$\overline{WE}$ Pulse Width	80	—	100	—	ns
t_{SD}	Data Setup to Write End	60	—	60	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	0	30	0	—	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

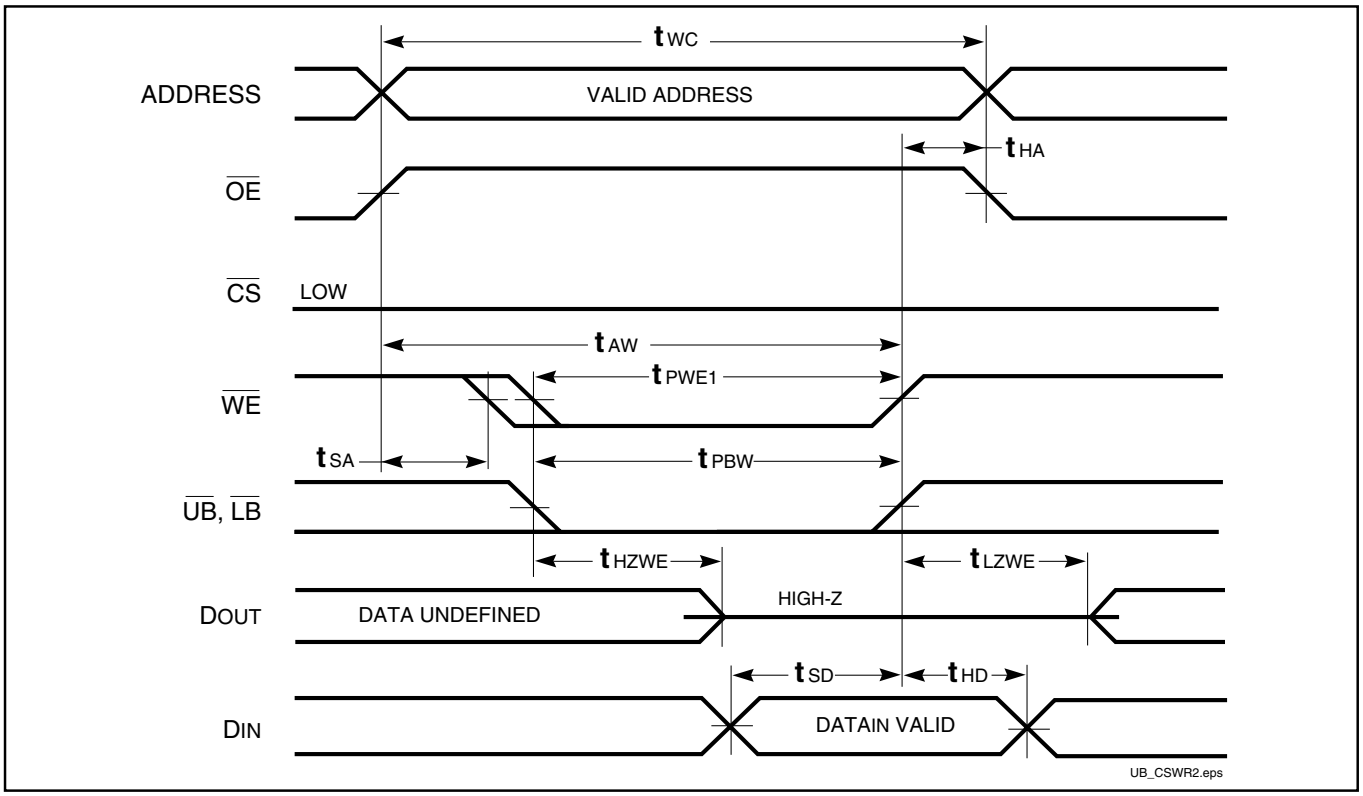
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

WRITE CYCLE NO. 1[1,2] ($\overline{CS}$ Controlled, $\overline{OE}$ = HIGH or LOW)

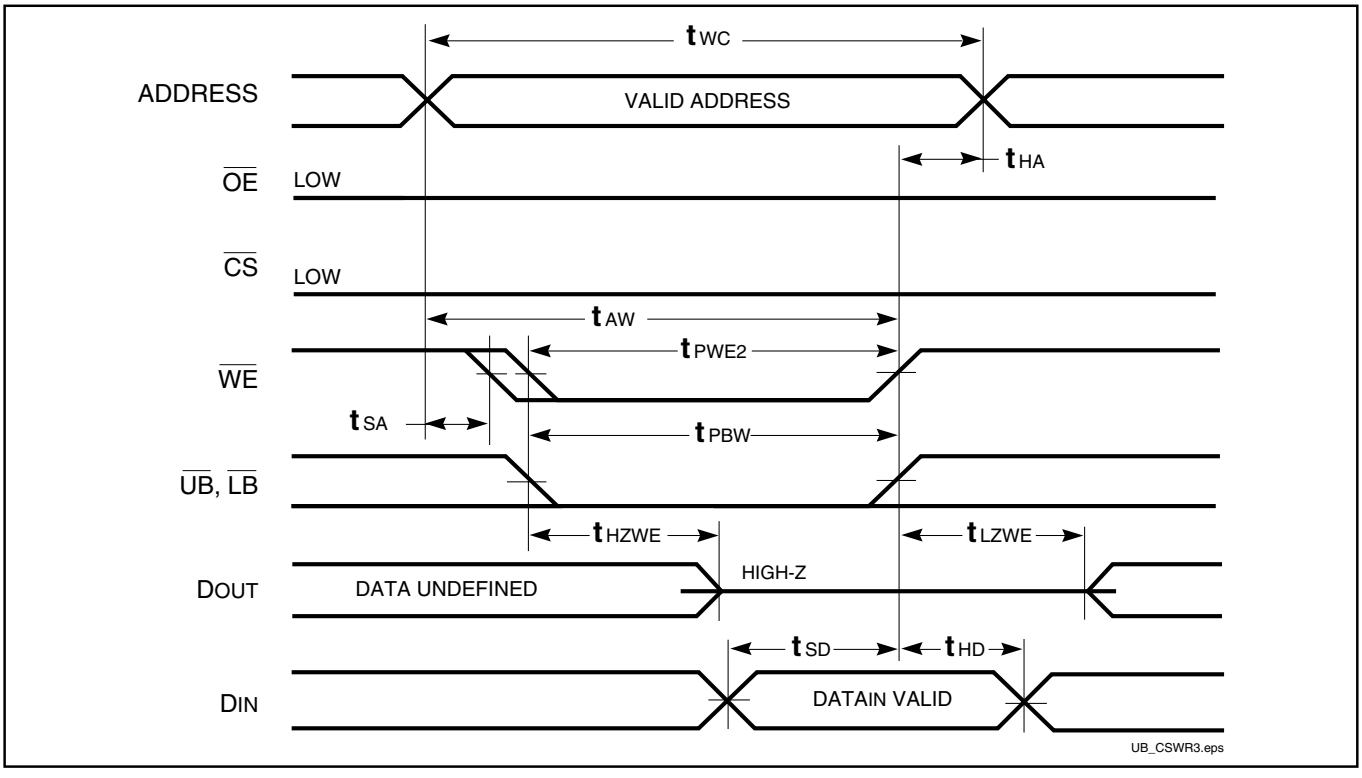


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

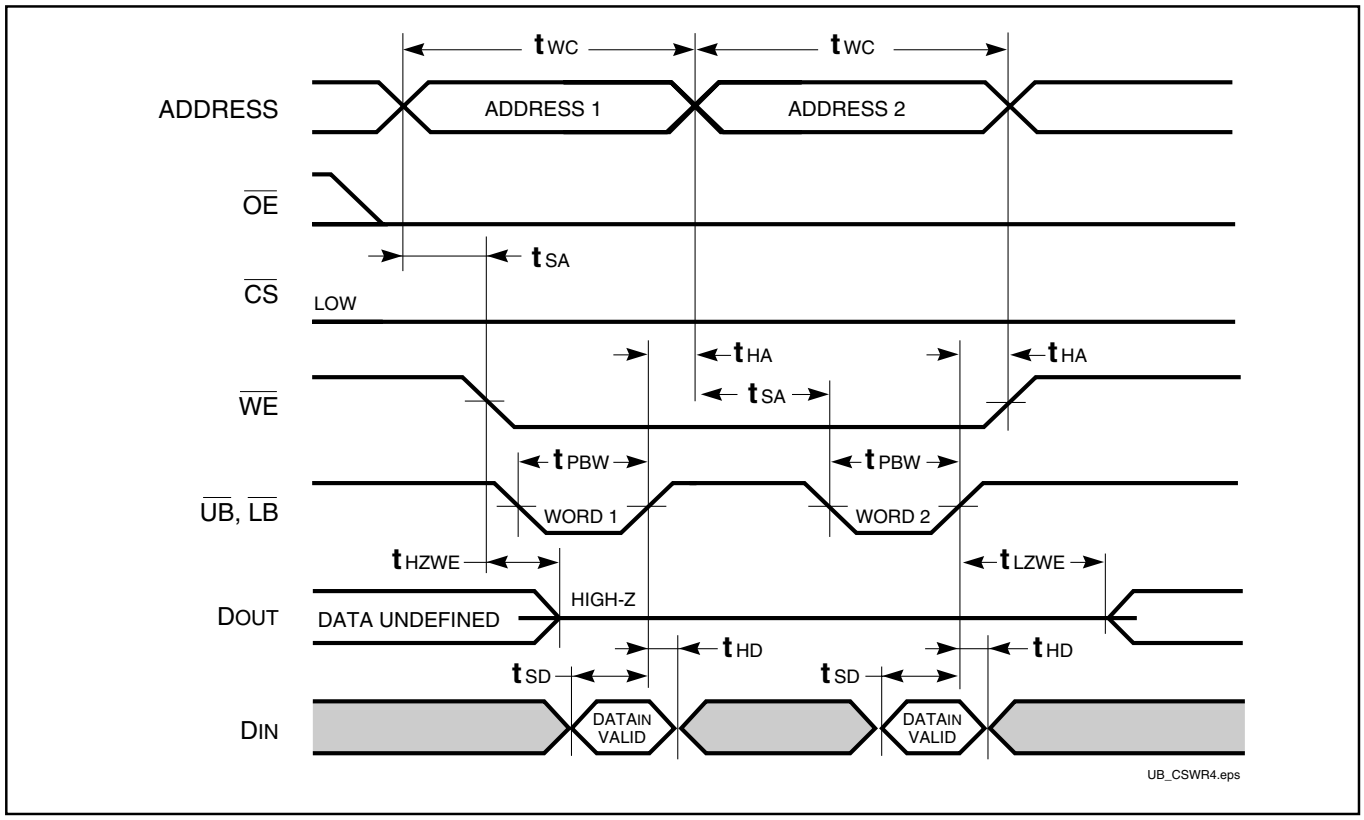
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



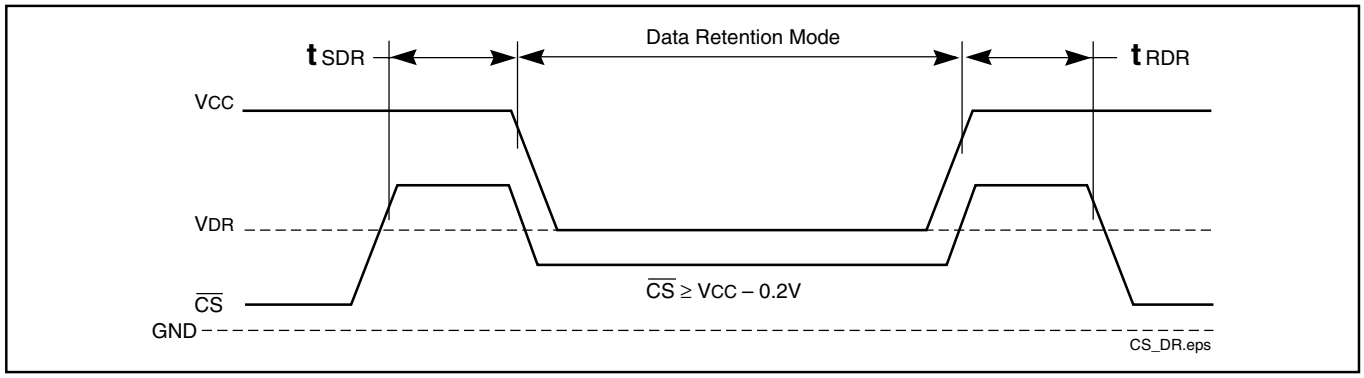
WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)



DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	V
I_{DR}	Data Retention Current	$V_{CC} = V_{DR}$ $\overline{CS} \geq V_{CC} - 0.2V$	—	5.0	µA
t_{SDR}	Data Retention Set up Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION TIMING DIAGRAM



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
100	IS62V6416BLL-10T	Plastic TSOP (Type II)
	IS62V6416BLL-10K	400-mil Plastic SOJ
	IS62V6416BLL-10B	Mini BGA (6mm x 8mm)
120	IS62V6416BLL-12T	Plastic TSOP (Type II)
	IS62V6416BLL-12K	400-mil Plastic SOJ
	IS62V6416BLL-12B	Mini BGA (6mm x 8mm)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
100	IS62V6416BLL-10TI	Plastic TSOP (Type II)
	IS62V6416BLL-10KI	400-mil Plastic SOJ
	IS62V6416BLL-10BI	Mini BGA (6mm x 8mm)
120	IS62V6416BLL-12TI	Plastic TSOP (Type II)
	IS62V6416BLL-12KI	400-mil Plastic SOJ
	IS62V6416BLL-12BI	Mini BGA (6mm x 8mm)

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Tel: 1-800-379-4774
Fax: (408) 588-0806
E-mail: sales@issi.com
www.issi.com