IS62U6416LL



ADVANCE INFORMATION DECEMBER 1998

64K x 16 LOW VOLTAGE, ULTRA-LOW POWER CMOS STATIC RAM

FEATURES

- Access time: 200 ns
- CMOS low power operation – 40 mW (typical) operating
 - 90 μW (typical) standby
- TTL compatible interface levels
- Single 1.8V-2.7V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in Jedec Std 44-pin SOJ package, 44-pin TSOP (Type II), and 48-pin mini BGA

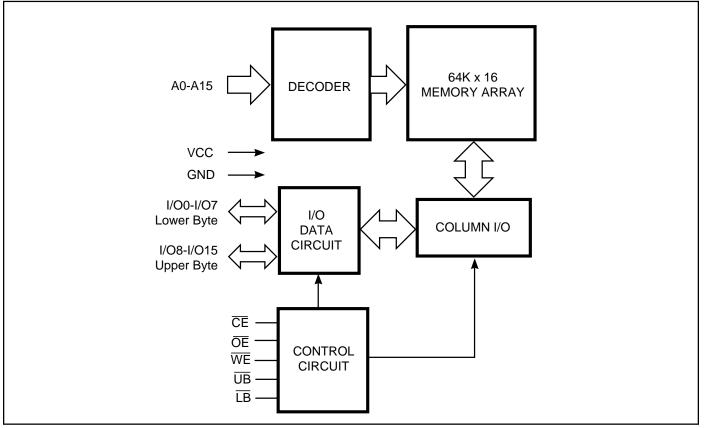
DESCRIPTION

The *ISSI* IS62U6416LL is an ultra-low power, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques yields access times as fast as 200 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

FUNCTIONAL BLOCK DIAGRAM



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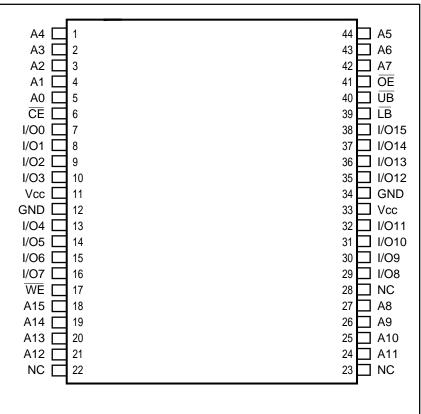
IS62U6416LL

PIN CONFIGURATIONS

44-Pin SOJ

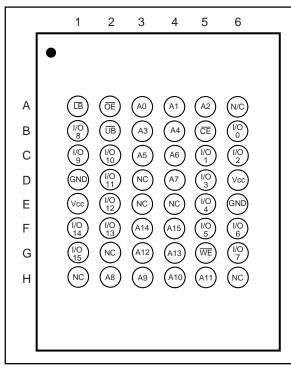
A4 🗖 1	44 🗌 A5
A3 🗌 2	43 🗋 A6
A2 🗖 3	42 🛛 A7
A1 🗖 4	41 🗍 OE
A0 🛛 5	40 🗍 ŪB
	39 🗋 LB
I/O0 🗖 7	38 🗍 I/O15
I/O1 🗖 8	37 🗍 I/O14
I/O2 🔲 9	36 🗍 I/O13
I/O3 🔲 10	35 🗍 I/O12
Vcc 🔲 11	34 🗍 GND
GND 🔲 12	33 🗍 Vcc
I/O4 🔲 13	32 🗍 I/O11
I/O5 🔲 14	31 🗍 I/O10
I/O6 🔲 15	30 🗍 1/O9
I/O7 🔲 16	29 🗍 I/O8
WE 🚺 17	28 🗍 NC
A15 🔲 18	27 🗋 A8
A14 🔲 19	26 🗋 A9
A13 🔲 20	25 🗋 A10
A12 🗖 21	24 🗋 A11
NC 🗖 22	23 🗌 NC

44-Pin TSOP



ISS

48-Pin mini BGA (Top View)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
ŪB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

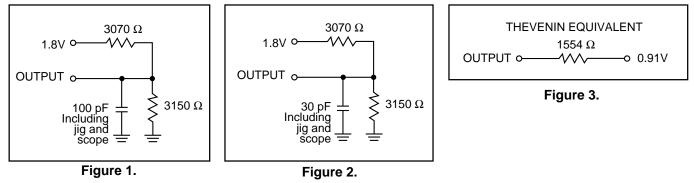
TRUTH TABLE

					I/O Pin				
Mode	WE	CE	ŌĒ	LB	UB	I/O0-I/O7	I/O8-I/O15	Vcc Current	
Not Selected	Х	Н	Х	Х	Х	High-Z	High-Z	ISB1, ISB2	
Output Disabled	Н	L	Н	Х	Х	High-Z	High-Z	lcc	
	Х	L	Х	Н	Н	High-Z	High-Z		
Read	Н	L	L	L	Н	Dout	High-Z	lcc	
	Н	L	L	Н	L	High-Z	Dout		
	Н	L	L	L	L	Dout	Dout		
Write	L	L	Х	L	Н	Din	High-Z	lcc	
	L	L	Х	Н	L	High-Z	DIN		
	L	L	Х	L	L	DIN	DIN		

AC TEST CONDITIONS

Parameter	Unit	
Input Pulse Level	0.4 to 1.8V ⁽¹⁾	
Input Rise and Fall Times	5 ns	
Input and Output Timing and Reference Level	0.9V ⁽¹⁾	
Output Load	See Figures 1 and 2	

AC TEST LOADS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	V
Tstg	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.5	W
Ιουτ	DC Output Current (LOW)	20	mA

Note:

 Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.8V (Min.) to 2.7V (Max.)
Industrial	–40°C to +85°C	1.8V (Min.) to 2.7V (Max.)

DC ELECTRICAL CHARACTERISTICS (Over Operating Range Unless Otherwise Specified)

Parameter	Test Conditions	Min.	Max.	Unit
Output HIGH Voltage	Vcc = Min., Iон = -0.44 mA	1.6	_	V
Output LOW Voltage	Vcc = Min., Io∟ = 0.33 mA		0.4	V
Input HIGH Voltage		1.6	Vcc + 0.2	V
Input LOW Voltage		-0.2	0.4	V
Input Leakage	$GND \le VIN \le Vcc$	-1	1	μA
Output Leakage	$GND \le VOUT \le Vcc$, Outputs Disabled	-1	1	μA
	Output HIGH Voltage Output LOW Voltage Input HIGH Voltage Input LOW Voltage Input Leakage	Output HIGH Voltage $Vcc = Min., IoH = -0.44 \text{ mA}$ Output LOW Voltage $Vcc = Min., IoL = 0.33 \text{ mA}$ Input HIGH VoltageInput LOW VoltageInput LOW Voltage $GND \le VIN \le Vcc$	Output HIGH VoltageVcc = Min., IoH = -0.44 mA1.6Output LOW VoltageVcc = Min., IoL = 0.33 mAInput HIGH Voltage1.6Input LOW Voltage-0.2Input LeakageGND \leq VIN \leq Vcc-1	Output HIGH VoltageVcc = Min., IoH = -0.44 mA1.6Output LOW VoltageVcc = Min., IoL = 0.33 mA 0.4 Input HIGH Voltage1.6Vcc + 0.2 Input LOW Voltage-0.2 0.4 Input Low VoltageGND \leq VIN \leq Vcc-1

Note:

1. VIL (min.) = -1.5V for pulse width less than 30 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range Unless Otherwise Specified)

				-20	00	
Symbol	Parameter	Test Conditions		Min.	Max.	Unit
lcc	Vcc Dynamic Operating Supply Current	Vcc = Max., lout = 0 mA, f = fmax \overline{CE} = VIH	Com. Ind.	_	25 40	mA
ISB1	TTL Standby Current (TTL Inputs)	$\label{eq:Vcc} \begin{array}{l} Vcc = Max., \\ V_{IN} = V_{IH} \text{ or } V_{IL} \\ \hline \overline{CE} \geq V_{IH} \text{ , } f = 0 \end{array}$	Com. Ind.	_	0.3 0.3	mA
ISB2	CMOS Standby Current (CMOS Inputs)	$\label{eq:constraint} \begin{array}{l} Vcc = Max.,\\ \overline{CE} \geq Vcc - 0.2V,\\ VIN \leq 0.2V, \ f = 0 \end{array}$	Com. Ind.	_	5 5	μA

Note:

1. At f = fMAX, address and data inputs are cycling at the maximum frequency; f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
Соит	Input/Output Capacitance	Vout = 0V	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾

(Over Operating Range)

		-20	00	
Symbol	Parameter	Min.	Max.	Unit
trc	Read Cycle Time	200	_	ns
t AA	Address Access Time		200	ns
tона	Output Hold Time	20	—	ns
t ACE	CE Access Time	—	200	ns
t doe	OE Access Time	_	100	ns
thzoe ⁽²⁾	OE to High-Z Output	0	50	ns
tlzoe ⁽²⁾	OE to Low-Z Output	20	_	ns
tHZCE ⁽²⁾	CE to High-Z Output	0	50	ns
tLZCE ⁽²⁾	CE to Low-Z Output	30	_	ns
tва	LB, UB Access Time	_	100	ns
tнzв	$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	0	50	ns
tlzв	\overline{LB} , \overline{UB} to Low-Z Output	20	_	ns

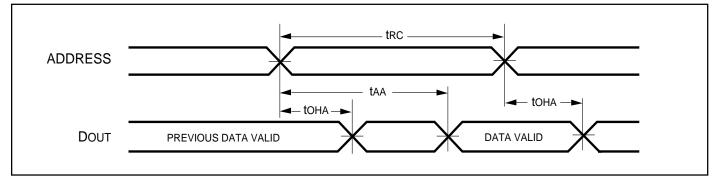
Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.8V and output loading specified in Figure 1.

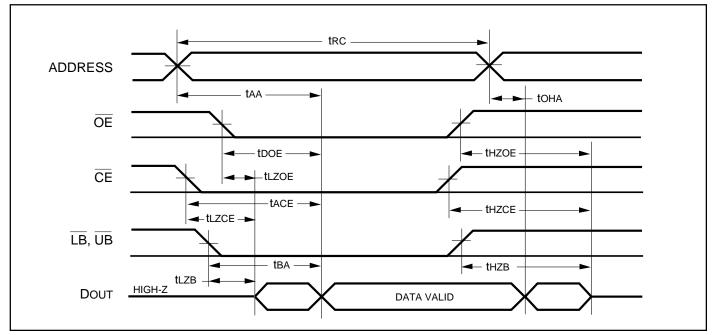
 Tested with the load in Figure 2. Transition is measured ±500mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}, \overline{UB} \text{ or } \overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



- **Notes:** 1. WE is HIGH for a Read Cycle. 2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
- 3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

		-200				
Symbol	Parameter	Min.	Max.	Unit		
twc	Write Cycle Time	200	—	ns		
t SCE	CE to Write End	160	_	ns		
taw	Address Setup Time to Write End	160		ns		
t ha	Address Hold from Write End	0		ns		
t sa	Address Setup Time	0		ns		
tрwв	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Valid to End of Write	160		ns		
t PWE	WE Pulse Width	160		ns		
tsp	Data Setup to Write End	160		ns		
t HD	Data Hold from Write End	0	_	ns		
tHZWE ⁽³⁾	WE LOW to High-Z Output	_	50	ns		
tLZWE ⁽³⁾	WE HIGH to Low-Z Output	20		ns		

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.8V and output loading specified in Figure 1.

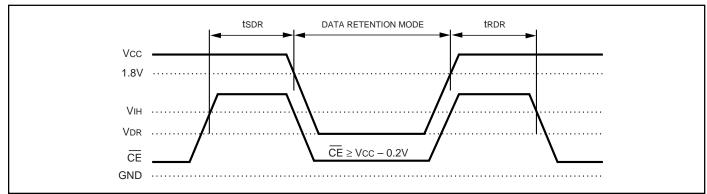
2. The internal write time is defined by the overlap of CE LOW and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

DATA RETENTION CHARACTERISTICS

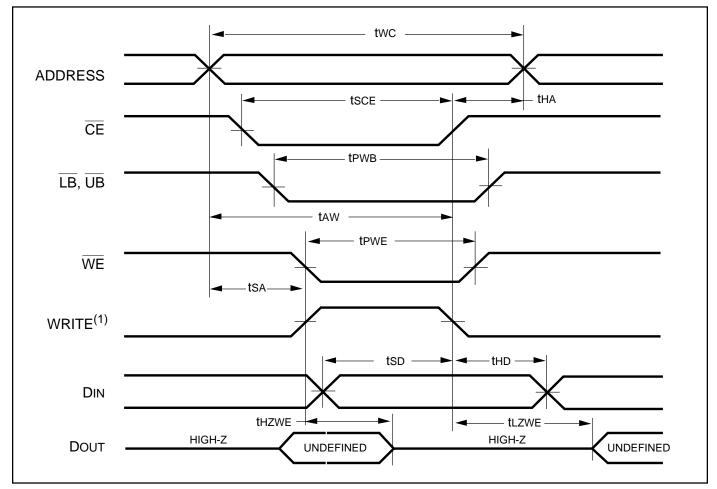
Symbol	Parameter	Test Condition	Min.	Max.	Unit
Vdr	Vcc for Data Retention	$\overline{CE} \ge Vcc - 0.2V$	1.5	_	V
Idr	Data Retention Current	$\frac{V_{CC} = V_{DR}}{CE} \ge V_{CC} - 0.2V$	—	5.0	μΑ
tsdr	Data Retention Set up Time	See Data Retention Waveform	0		ns
trdr	Recovery Time	See Data Retention Waveform	trc		ns

DATA RETENTION TIMING DIAGRAM



AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (WE Controlled)



Notes:

- WRITE is an internally generated signal asserted during an overlap of the LOW states on the CE and WE inputs and at least one of the LB and UB inputs being in the LOW state.
 WRITE = (CE) [(LB) = (UB)] (WE).

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
200	IS62U6416LL-20T IS62U6416LL-20K	Plastic TSOP (Type II) 400-mil Plastic SOJ
	IS62U6416LL-20B	Mini BGA (6mm x 8mm)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
200	IS62U6416LL-20TI IS62U6416LL-20KI	Plastic TSOP (Type II) 400-mil Plastic SOJ
	IS62U6416LL-20BI	Mini BGA (6mm x 8mm)

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