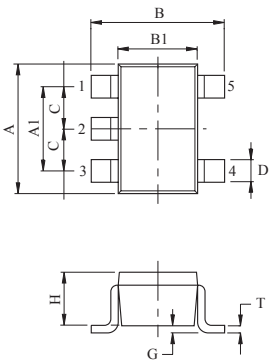
KIC7SZ38FU

SILICON MONOLITHIC CMOS DIGITAL INTEGRATED CIRCUIT

2 INPUT NAND GATE (Open Drain Output)

FEATURES

- Open Drain Output Stage for OR tied application.
- Super High Speed : 2.4ns(Typ.) 50pF at V_{CC}=5V.
- High Output Sink Drive : 24mA at V_{CC}=3V.
- Operating Voltage Range : $V_{CC(opr)}$=1.65~5.5V.
- Power Down High Impedance Inputs/Outputs.



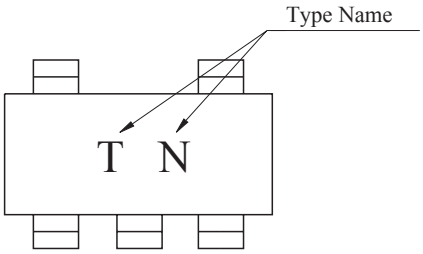
DIM	MILLIMETERS
A	2.00±0.20
A1	1.3±0.1
B	2.1±0.1
B1	1.25±0.1
C	0.65
D	0.2+0.10/-0.05
G	0-0.1
H	0.9±0.1
T	0.15+0.1/-0.05

USV

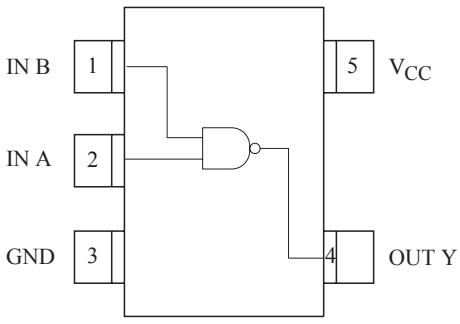
MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	-50~20	mA
Output Diode Current	I_{OK}	-50~20	mA
DC Output Current	I_{OUT}	50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING



PIN CONNECTION(TOP VIEW)



Logic Diagram

ELECTRICAL CHARACTERISTICS

DC Characteristics

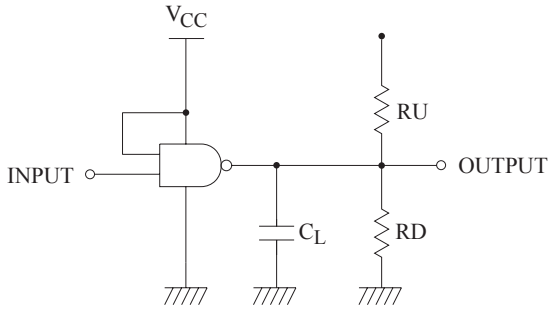
CHARACTERISTIC		SYMBOL	TEST CONDITION			Ta=25℃			Ta=-40~85℃		UNIT
					V_{CC}(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	High Level	V_{IH}	-		1.65~1.95	0.75×V_{CC}	-	-	0.75×V_{CC}	-	V
					2.3~5.5	0.7×V_{CC}	-	-	0.7×V_{CC}	-	
	Low Level	V_{IL}	-		1.65~1.95	-	-	0.25×V_{CC}	-	0.25×V_{CC}	
					2.3~5.5	-	-	0.3×V_{CC}	-	0.3×V_{CC}	
Output Leakage Voltage	High Level	I_{LKG}	V_{IN}=V_{IL} V_{OUT} = V_{CC} or GND		5.5	-	-	±5	-	±10	μA
	Low Level	V_{OL}	V_{IN}=V_{IH}	I_{OL}=100μA	1.65	-	0	0.1	-	0.1	V
					1.8	-	0	0.1	-	0.1	
					2.3	-	0	0.1	-	0.1	
					3.0	-	0	0.1	-	0.1	
					4.5	-	0	0.1	-	0.1	
				I_{OL}=4mA	1.65	-	0.08	0.24	-	0.24	
				I_{OL}=8mA	2.3	-	0.10	0.3	-	0.3	
				I_{OL}=16mA	3.0	-	0.15	0.4	-	0.4	
				I_{OL}=24mA	3.0	-	0.22	0.55	-	0.55	
				I_{OL}=32mA	4.5	-	0.22	0.55	-	0.55	
Input Leakage Current		I_{IN}	V_{IN}=5.5V or GND		0~5.5	-	-	±1	-	±10	μA
Power Off Leakage Current		I_{OFF}	V_{IN} or V_{OUT}=5.5V		0.0	-	-	1	-	10	μA
Quiescent Supply Current		I_{CC}	V_{IN}=5.5V or GND		5.5	-	-	2.0	-	20	μA

AC Characteristics (unless otherwise specified, Input : $t_r=t_f=3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta=25℃			Ta=-40~85℃		UNIT
			V_{CC}(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation delay time	t_{PZL}	C_L=50pF, R_U=500Ω R_D=500Ω V_I=2×V_{CC} (Figures 1,3)	1.65	1.5	6.5	12.7	1.5	13.2	ns
			1.8	1.5	5.4	10.5	1.5	11.0	
			2.5±0.2	0.8	3.5	7.0	0.8	7.5	
			3.3±0.3	0.8	2.8	5.0	0.8	5.2	
			5.0±0.5	0.5	2.2	4.3	0.5	4.5	
	t_{PLZ}	C_L=50pF, R_U=500Ω R_D=500Ω V_I=2×V_{CC} (Figures 1,3)	1.65	1.5	5.5	12.7	1.5	13.2	ns
			1.8	1.5	4.6	10.5	1.5	11.0	
			2.5±0.2	0.8	3.0	7.0	0.8	7.5	
			3.3±0.3	0.8	2.1	5.0	0.8	5.2	
			5.0±0.5	0.5	1.3	4.3	0.5	4.5	
Input Capacitance	C_{IN}	-	0	-	4	-	-	-	pF
Output Capacitance	C_{OUT}	-	0	-	5	-	-	-	pF
Power Dissipation Capacitance	C_{PD}	(Note) (Figures 2)	3.3	-	5.1	-	-	-	pF
			5.0	-	7.3	-	-	-	

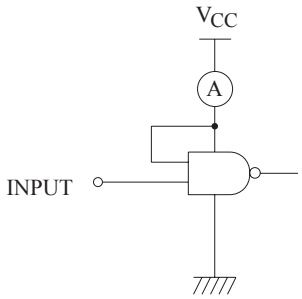
Note : C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression : $I_{CCD}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$ Static

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR=1.0MHz ; t_W=500ns

FIGURE 1. AC Test Circuit



Input=AC Waveform ; $t_r=t_f$=1.8ns
PRR=10MHz ; Duty Cycle=50%

FIGURE 2. I_{CCD} Test Circuit

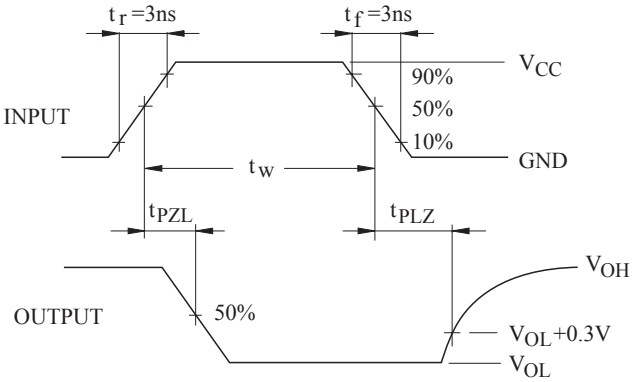


FIGURE 3. AC Waveforms