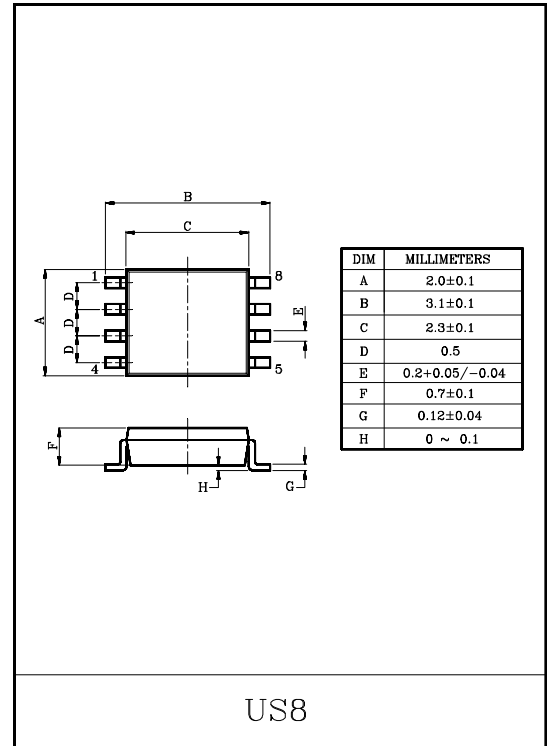


NON-INVERTED, 3-STATE OUTPUTS

The KIC7W241FK is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation. It is a non-inverting 3-state buffer that has one active-high and one active-low output enable. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

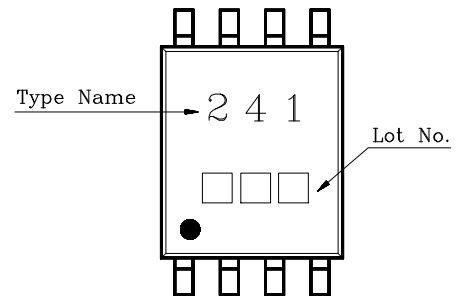
- High Speed : $t_{pd}=10\text{ns}$ (Typ.) at $V_{CC}=5\text{V}$.
- Low Power Dissipation : $I_{CC}=2\mu\text{A}$ (Max.) at $T_a=25^\circ\text{C}$.
- High Noise Immunity : $V_{NIH}=V_{NIL}=28\% V_{CC}$ (Min.).
- Output Drive Capability : 15 LSTTL Loads.
- Symmetrical Output Impedance : $|I_{OH}|=I_{OL}=6\text{mA}$ (Min.)
- Balanced Propagation Delays : $t_{pLH}\doteq t_{pHL}$
- Wide Operating Voltage Range : $V_{CC(\text{opr})}=2\sim 6\text{V}$.



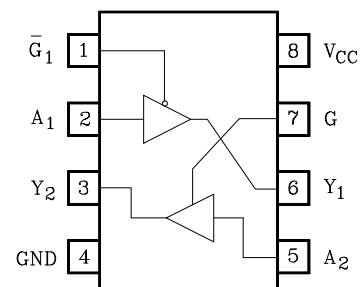
MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC} /Ground Current	I_{CC}	±37.5	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10s)	T_L	260	°C

MARKING

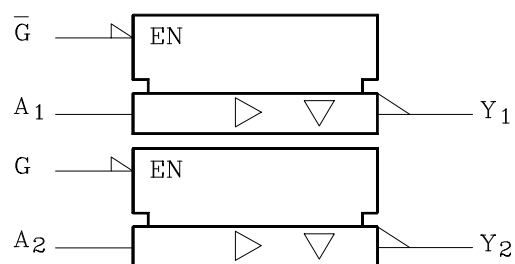


PIN CONNECTION(TOP VIEW)



KIC7W241FK

LOGIC DIAGRAM



TRUTH TABLE

INPUT			OUTPUT
\bar{G}	G	A	Y
L	H	L	L
L	H	H	H
H	L	X	Z

X : Don't Care
Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC}=2.0V$) 0~500 ($V_{CC}=4.5V$) 0~400 ($V_{CC}=6.0V$)	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	V_{CC}	$T_a=25^\circ C$			$T_a=-40\sim 85^\circ C$		UNIT										
					MIN.	TYP.	MAX.	MIN.	MAX.											
High-Level Input Voltage	V_{IH}	-	-	2.0	1.5	-	-	1.5	-	V										
				4.5	3.15	-	-	3.15	-											
				6.0	4.2	-	-	4.2	-											
Low-Level Input Voltage	V_{IL}	-	-	2.0	-	-	0.5	-	0.5	V										
				4.5	-	-	1.35	-	1.35											
				6.0	-	-	1.8	-	1.8											
High-Level Output Voltage	V_{OH}	-	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V									
					4.5	4.4	4.5	-	4.4	-										
					6.0	5.9	6.0	-	5.9	-										
Low-Level Output Voltage	V_{OL}	-	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V									
					4.5	-	0.0	0.1	-	0.1										
					6.0	-	0.0	0.1	-	0.1										
3-State Output Off-State Current	I_{OZ}	-	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	6.0	-	-	± 0.5	-	± 5.0	μA										
											Input Leakage Current	I_{IN}	-	$V_{IN}=V_{CC}$ or GND	6.0	-	-	± 0.1	-	± 1.0

KIC7W241FK

AC ELECTRICAL CHARACTERISTICS (Input $t_r=t_f=6\text{ns}$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				C _L	V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}	-	-	50	2.0	-	25	60	-	75	ns
					4.5	-	7	12	-	15	
					6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}	-	-	50	2.0	-	36	90	-	115	
					4.5	-	12	18	-	23	
					6.0	-	10	15	-	20	
				150	2.0	-	51	130	-	165	
					4.5	-	17	26	-	33	
					6.0	-	14	22	-	28	
Output Enable Time	t_{pZL} t_{pZH}	-	R _L =1kΩ	50	2.0	-	48	125	-	155	
					4.5	-	16	25	-	31	
					6.0	-	14	21	-	26	
				150	2.0	-	63	165	-	205	
					4.5	-	21	33	-	41	
					6.0	-	18	28	-	35	
Output Disable Time	t_{pLZ} t_{pHZ}	-	R _L =1kΩ	50	2.0	-	32	125	-	155	
					4.5	-	15	25	-	31	
					6.0	-	14	21	-	26	
Input Capacitance	C _{IN}	-	-	-	-	-	5	10	-	10	pF
Output Capacitance	C _{OUT}	-	-	-	-	10	-	-	-		
Power Dissipation Capacitance	C _{PD}	-	(Note 1)	-	-	-	33	-	-	-	

Note 1 : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation

$$: I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per gate)}$$