GigabitCAM

KE5BGCA256

Preliminary

KAWASAKI
LSI

Ver. 1.1.1

Contents

1. Features

The KE5BGCA256 provides best solution to the fast "Address Filtering" requirements of today's internetworking switching equipment with the following outstanding functions.

• 256k-bit capacity of table

- 64-bit x 4096 entries
- CAM/RAM substitution

• Dual Port Architecture

- 32-bit I/O Port
- 16-bit Output Port

• 12 Search Conditions

-12 Mask registers selected by the external pins (MS<3:0>) and the CNTL1 register

- Access bit can be set for data aging
- Permanent bit can be set for permanent entry
- Automatic output of the contents of the Hit entry and the Empty entry address from the 16-bit Output Port

• Cascading

- Table size is expandable.
- A cascaded table acts as one integral search data table by internal device priority control.

• Commands

- Useful commands for table management such as aging and purging.
- Useful command for Source Address Learning

• Synchronous Operation

- 30ns cycle time
- 64-bit input/30ns
- Search, data read/write, and command operations are executed at high speed.

• 128-pin SQFP Package

• 3.3 v CMOS technology

2. Block Diagram

This device consists of the following blocks as shown.

CPU Bus Control Block

An access to the search key data, commands, or internal registers are executed through the CPU Bus.

Pipeline Execution Control

This block controls the pipeline operation of this device.

CNTL1/2 Registers

These registers define the mask registers and the input modes , etc.

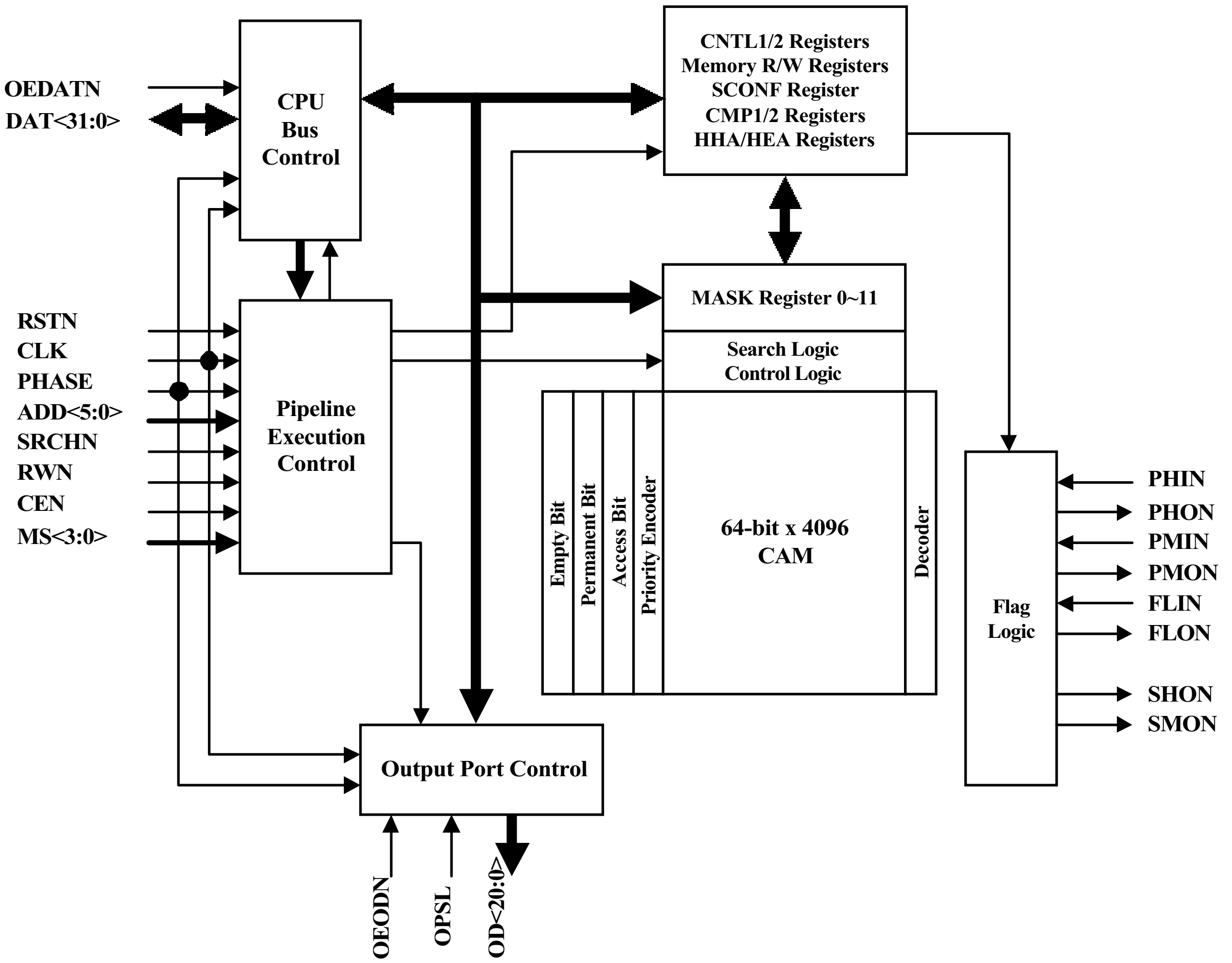


Fig. 2 Block Diagram

Memory R/W Registers

These registers are used to access the CAM table.

SCONF Register

This register defines the configuration of the search operation.

CMP1/2 Registers

These two registers store the search key data and both are 64 bits in width.

HHA/HEA Registers

These two registers respectively store the hit address and the empty address of the CAM table.

MASK Registers

These 12 registers are used to mask the data bit by bit in the search operation or the write operation to the CAM table.

CAM

The capacity of the CAM table is 64 bits x 4096 entries.

Flag Logic

This block outputs the search result and the status of the CAM table and has the interface function for a cascade connection.

Output Port Control

This block controls the Output Port which outputs the search result.

3. Pin Assignment and Pin Descriptions

3.1 Pin Assignment

KE5BGCA256
(128pinSQFPtype)

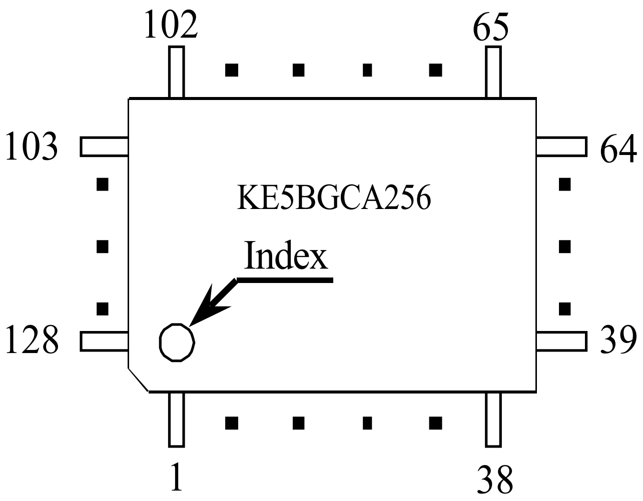


Fig. 3.1.1 Pin Assignment

Pin No.	Signal Name	I/O type
1	GND	-
2	OD<0>	OUT
3	OD<1>	OUT
4	VDD	-
5	VDD	-
6	OD<2>	OUT
7	OD<3>	OUT
8	OD<4>	OUT
9	GND	-
10	OD<5>	OUT
11	OD<6>	OUT
12	OD<7>	OUT
13	GND	-
14	OD<8>	OUT
15	VDD	-
16	OD<9>	OUT
17	OD<10>	OUT
18	GND	-
19	GND	-
20	GND	-
21	OD<11>	OUT
22	VDD	-
23	OD<12>	OUT
24	VDD	-
25	OD<13>	OUT
26	OD<14>	OUT
27	GND	-
28	OD<15>	OUT
29	OD<16>	OUT
30	OD<17>	OUT
31	OD<18>	OUT
32	GND	-
33	OD<19>	OUT
34	VDD	-
35	VDD	-
36	OD<20>	OUT
37	GND	-
38	FLON	OUT
39	SMON	OUT
40	SHON	OUT
41	GND	-
42	PMON	OUT
43	PHON	OUT
44	FLIN	IN
45	PMIN	IN
46	PHIN	IN
47	VDD	-
48	OPSL	IN
49	OEODN	IN
50	GND	-
51	GND	-
52	GND	-
53	MS<0>	IN
54	MS<1>	IN
55	MS<2>	IN
56	MS<3>	IN
57	DAT<0>	I/O
58	DAT<1>	I/O
59	VDD	-
60	DAT<2>	I/O
61	DAT<3>	I/O
62	GND	-
63	DAT<4>	I/O
64	DAT<5>	I/O
65	GND	-
66	DAT<6>	I/O
67	DAT<7>	I/O
68	VDD	-
69	VDD	-
70	DAT<8>	I/O
71	DAT<9>	I/O
72	GND	-
73	DAT<10>	I/O
74	DAT<11>	I/O
75	DAT<12>	I/O
76	GND	-
77	DAT<13>	I/O
78	VDD	-
79	DAT<14>	I/O
80	VDD	-

Table.3.1 Pin Assignment

Pin No.	Signal Name	I/O type
81	PHASE	IN
82	CLK	IN
83	GND	-
84	GND	-
85	GND	-
86	DAT<15>	I/O
87	DAT<16>	I/O
88	VDD	-
89	DAT<17>	I/O
90	DAT<18>	I/O
91	DAT<19>	I/O
92	GND	-
93	DAT<20>	I/O
94	DAT<21>	I/O
95	DAT<22>	I/O
96	GND	-
97	DAT<23>	I/O
98	VDD	-
99	VDD	-
100	DAT<24>	I/O
101	DAT<25>	I/O
102	GND	-
103	DAT<26>	I/O
104	DAT<27>	I/O
105	GND	-
106	DAT<28>	I/O
107	DAT<29>	I/O
108	DAT<30>	I/O
109	DAT<31>	I/O
110	VDD	-
111	ADD<0>	IN
112	ADD<1>	IN
113	ADD<2>	IN
114	ADD<3>	IN
115	GND	-
116	GND	-
117	GND	-
118	ADD<4>	IN
119	ADD<5>	IN
120	RSTN	IN
121	CEN	IN
122	RWN	IN
123	SRCHN	IN
124	OEDATN	IN
125	NC	OPEN*1
126	GND	-
127	GND	-
128	GND	-

*1 NC pins must be open. (Do not connect.)

Table 3.1 Pin Assignment (cont'd)

3.2 Pin Descriptions

Pin name	Attribute	Function
CLK	**CLOCK** Input LVTTL	CLK is the master clock input. Other input signals are referred to the rising edge of CLK.
PHASE	**PHASE** Input LVTTL	PHASE determines the action timing of the device. The latency of the output is also determined by the relationship between PHASE and CLK. Regardless of whether the input mode is 32 bits (Normal Access Mode) or 64 bits (First Access Mode), two cycles of the CLK signals are necessary. PHASE regulates the input timing of the data input from 32-bit DAT<31:0> when the input mode is 64 bits. When PHASE is high, the data on DAT<31:0> is input in the 32 bits on the MSB side of 64 bits. When PHASE is low, the data is input in the 32 bits on the LSB side. When the input mode is 32 bits, the 32-bit data is written in the register designated by ADD<5:0> on the rising edge of CLK while PHASE is low.
DAT<31:0>	**CPU Bus** Input/Output Tristate LVTTL	DATA<31:0> is a 32-bit, bidirectional data bus used to convey data, to execute commands, and to write/read to and from the registers. The direction is controlled by RWN and there is latency when the bus is switched.
ADD<5:0>	**CPU Bus Address Bus** Input LVTTL	ADD<5:0> is a 6-bit address bus used to select registers.
CEN	**Device Enable** Input LVTTL	CEN is used to access the CPU port. The active CEN enables the input operation of data and command.
RWN	**Read/Write** Input LVTTL	RWN is used to determine the direction of the CPU bus. RWN low selects a write cycle, and RWN high selects a read cycle. There is latency between the RWN change and the output as the result of the data bus change.
OEDATN	**CPU Bus Output Enable** Input LVTTL	OEDATN controls the CPU bus output. OEDATN low enables the output of the CPU bus by the read operation, and OEDATN high makes the CPU bus have high impedance despite the output indication by the read operation. There is latency between the OEDATN change and its result.
SRCHN	**Search Enable** Input LVTTL	SRCHN enables the search operation together with the write operation to the comparand register.

Pin name	Attribute	Function
MS<3:0>	**Mask Select** Input LVTTL	MS<3:0> is a mask select signal. One of 12 Mask registers is selected by the MS<3:0>.
RSTN	**Hardware Reset** Input LVTTL	RSTN is used to reset the hardware.
OD<20:0>	**Output Port** Output Tristate LVTTL	OD<20:0> is a 21-bit output port. The device ID is output in the 5 bits, OD<20:16> from the MSB, and HHA, HEA, or MEMHHA is output in the 16 bits from the LSB.
OEODN	**Output Port Output Enable** Input LVTTL	OEODN controls the Output Port. OEODN low enables the output, and OEODN high disables the output (i.e. the Output Port is made high impedance). There is latency between the OEODN change and its result.
OPSL	**Output Port Select** Input LVTTL	OPSL low enables the output of MEMHHA from the Output Port. There is latency between the OPSL change and its result.
SHON	**Synchronous Hit Output** Output LVTTL	SHON outputs the search results in the device synchronous with the master clock. This pin is low when even one hit occurs in the search operation. This pin is high when no entry is hit.
SMON	**Synchronous Multi-hit Output** Output LVTTL	SMON outputs the search results in the device synchronous with the master clock. This pin is low when multi-hit occurs in the search operation. This pin is high when no multi-hit occurs.
PHON	**Priority Hit Output** Output LVTTL	PHON outputs the search results. This pin is not synchronous with the master clock. This pin is low when even one hit occurs in the search operation. This pin is high when no entry is hit. In a cascaded system, the hit signal of the cascade configuration appears in the PHON pin of the lowest priority device (Last Device).
PMON	**Priority Multi-hit Output** Output LVTTL	PMON outputs the search results. This pin is not synchronous with the master clock. This pin is low when multi-hit occurs in the search operation. This pin is high when no multi-hit occurs. In a cascaded system, the multi-hit signal of the cascade configuration appears in the PMON pin of the lowest priority device (Last Device).

Pin name	Attribute	Function
PHIN	**Priority Hit Input** Input LVTTL	PHIN is used to connect plural devices in a cascaded system.
PMIN	**Priority Multi-hit Input** Input LVTTL	PMIN is used to connect plural devices in a cascaded system.
FLON	**Full Flag Output** Output LVTTL	FLON outputs the search results. This pin is low when all entries in the CAM are filled with valid entries (full status) and there is no more entry for a new registration. In a cascaded system, the full signal of the cascade configuration appears in the FLON pin of the lowest priority device (Last Device).
FLIN	**Full Flag Input** Input LVTTL	FLIN is used in a cascaded system.
VDD	**Supply**	Power supply : 3.3V±0.3V
GND (Supply)	**Ground**	Ground

4. Functional Descriptions

4.1 Access from CPU Port

This device has a 32-bit data bus as a CPU port. Data read/write is performed by the registers that are mapped with 32-bit width (Refer to Chapter 7.2). To access registers wider than 32 bits or to access the CAM memory, two data read/write accesses are required. A special high speed write mode (Fast Write Mode) is provided for the data write.

• Normal Access Mode

In this mode, one 32-bit data read/write is done with one PHASE signal cycle. Data, address and control signals must be input synchronously with the rising edge of CLK when the PHASE signal, which is a double cycle signal of the CLK, is low. (See Fig. 4.1.1 (a))
All the bits of each register address are valid in this mode. Each 32-bit register is defined by the address pins ADD<5:0>. Two accesses cycles are required for the read/write of 64-bit registers and the CAM memory.

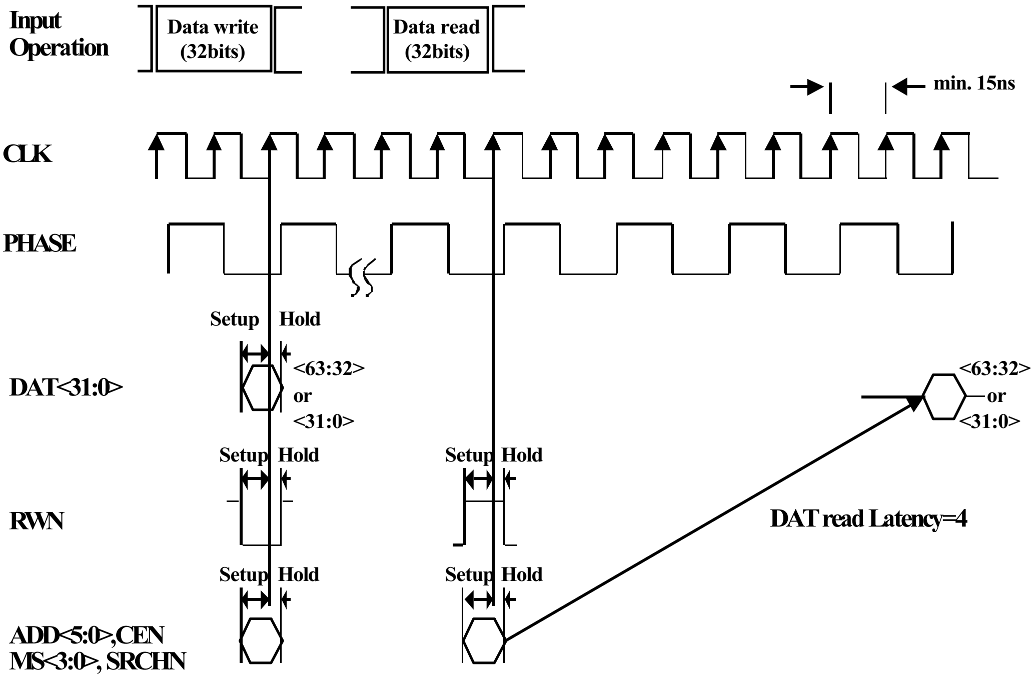


Fig. 4.1.1 (a) CPU Access Mode (Normal Access Mode)

• Fast Write Mode

In this mode, one 64-bit data read/write is done within one PHASE signal cycle. The upper 32-bit data of the 64-bit register is input synchronously with the rising edge of CLK when the PHASE signal, which is a double cycle signal of the CLK, is high. The lower 32-bit data of the 64-bit register, address, and control signals are input synchronously with the rising edge of the CLK signal when the PHASE signal is low. (See Fig. 4.1.1 (b)) The LSB of the address is ignored in this case. If a 32-bit register is accessed in this mode, only the data, the address, and the control signals that are input with the rising edge of CLK while the PHASE signal is low, are valid. (See Fig. 4.1.1 (b)) The LSB of the address is also ignored in this case.

Normal Access or Fast Write Mode is selected by the definition of the CNTL1 register. The initial definition after the device reset is Normal Access Mode.

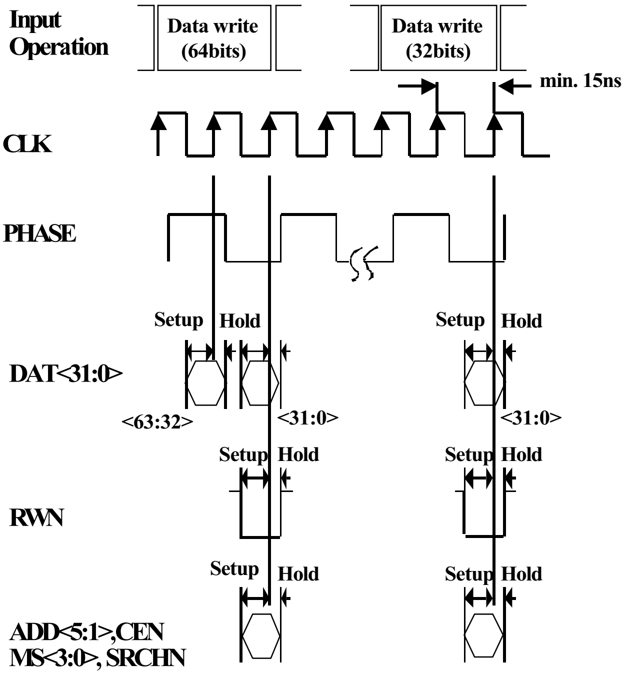


Fig. 4.1.1 (b) CPU Access Mode (Fast Write Mode)

4.2 Read/Write Registers

The register address is designated by the address pins of the CPU port, and the data is inputted on the DAT bus. (See Fig. 4.2.1) The function of each register is described in Chapter 7. This figure shows the example of the Fast Write Mode.

In case of the Normal Access Mode, data write is the same as the Fast Write Mode shown in Fig. 4.2.1 if you exclude the write of the upper 32 bits of the 64-bit word.

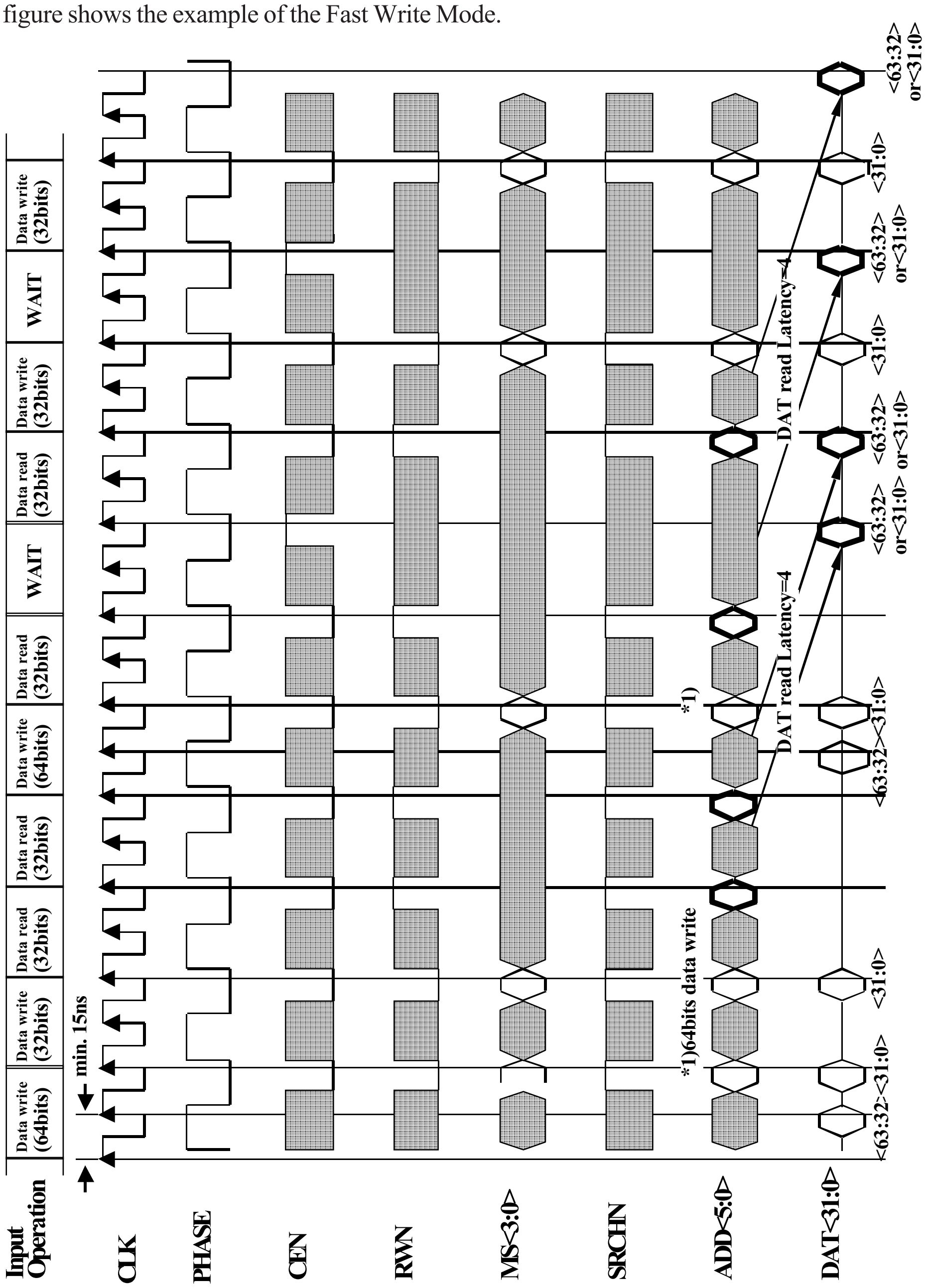


Fig. 4.2.1 Data read/write Timing Chart (Fast Write Mode)

4.3 Access to the CAM Memory

• Word Structure of CAM

One word of the CAM is made up of 64-bit CAM memory and 3 attribute bits (1 bit each). The 64-bit CAM memory stores the users data to be searched. The attribute bits are the Empty Bit, the Permanent Bit, and the Access Bit. (See Fig. 4.3.1):

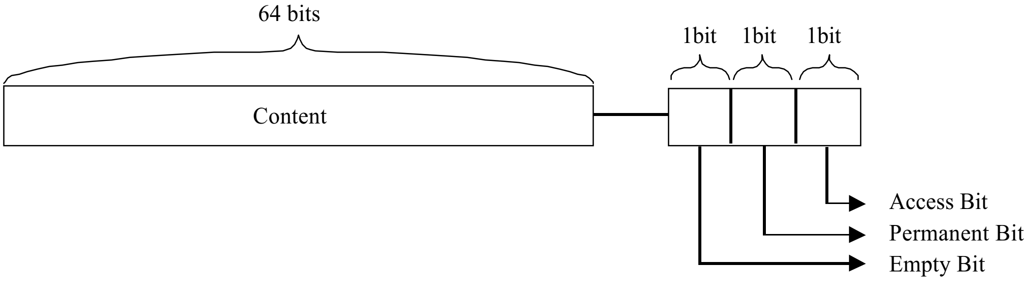


Fig.4.3.1 Word Structure of CAM

The Empty Bit: The Empty Bit is a flag that indicates the validity of the CAM word. An invalid word is excluded from the search target and is recognized as a candidate for memory for a new registration of valid data.
The flag logic is:

0 : valid (Valid data is written);
1 : invalid (Memory is a space).

The Permanent Bit: The entry whose Permanent Bit is set to "1" will not become invalid (Empty Bit = 1) by any purge commands. In order to clear this bit, users can use the reset command.

The Access Bit: The Access Bit is provided for the management of the hit career of each entry. Users can specify whether the hit career is held in the Access Bit or not for each search cycle. Once the Access Bit is set to "1," however, it holds "1" until an Access Bit reset command is executed.
These attribute bits can be directly modified by accessing the MEMAR_AT, MEMHHA_AT, and MEMHEA_AT registers.
These bits are reset by the reset signal from the RSTN pin as follows:

- The Empty Bit : 1 (Invalid)
- The Permanent Bit : 0 (Impermanent)
- The Access Bit : 0 (No hit career)

• Read/Write CAM Memory

Read/write of the entry data is executed not by direct address indication, but by indirect address indication through specific registers (MEMAR, MEMARAI, MEMAR_AT, MEMHHA, MEMHHA_AT, MEMHEA, MEMHEAAI, and MEMHEA_AT). When writing through MEMAR, MEMARAI, MEMHHA, MEMHEA, and MEMHEAAI, 12 kinds of mask conditions can be selected. Mask in the data write operation means that the data of masked bit is not changed by the write operation. There are two ways to select the mask condition from the 12 mask registers (MASK0 - MASK11). One way is to select it with 4 single pins, MS<3:0> applied dynamically in data write. The other way is to select by the definition in the CNTL1 register statically .

The read/write of the CAM memory is basically the same as the read/write of the registers. As shown in Fig. 4.2.1, the mask condition in the write operation is selected by MS<3:0>, the status of these select control signals is latched by the rising edge of CLK while the PHASE signal is low, and the data is written to the memory with Latency 2. The read data is output from the CPU port with Latency 4. (See Section 4.7 about Latency.)

• Read/Write CAM Data through the MEMAR register

Read/write operation of the CAM word, whose address is designated by the AR register, is executed by the MEMAR register. Write through the MEMAR register changes the attribute bits in the CAM word as follows:

- Empty Bit : 0 (Entry is valid.)
- Permanent Bit : Return to the default value defined in the CNTL1 register
- Access Bit : Return to the default value defined in the CNTL1 register.

•Read/Write CAM Data through the MEMARAI register

Read/write operation of the CAM word, whose address is designated by the AR register, is executed by the MEMARAI register. One read/write to the MEMARAI register increments the value of the AR register automatically. Write through the MEMARAI register changes the attribute bits in the CAM word as follows:

- Empty Bit : 0 (Entry is valid.)
- Permanent Bit : Return to the default value defined in the CNTL1 register.
- Access Bit : Return to the default value defined in the CNTL1 register.

•Read/Write CAM Data through the MEMHHA register

Read/write operation of the CAM word, whose address is designated by the HHA register, is executed by the MEMHHA register. Read/write through the MEMHHA register is prohibited when the address stored in the HHA register is invalid, because this may cause an access to the undesired CAM word and the data in it might be destroyed. Read/write through the MEMHHA register does not change the attribute bits in the CAM word.

•Read/Write CAM Data through the MEMHEA register

Read/write operation of the CAM word, whose address is designated by the HEA register, is executed by the MEMHEA register. Read/write through the MEMHEA register is prohibited when the address stored in the HEA register is invalid, because this may cause an access to the undesired CAM word and the data in it might be destroyed. Write through the MEMHEA register changes the attribute bits in the CAM word as follows:

- Empty Bit : 0 (Entry is valid.)
- Permanent Bit : Return to the default value defined in the CNTL1 register.
- Access Bit : Return to the default value defined in the CNTL1 register.

•Read/Write CAM Data through the MEMHEAAI register

Read/write operation of the CAM word, whose address is designated by the HEA register, is executed by the MEMHEAAI register. One read/write to the MEMHEAAI register shifts the value of the HEA register to the value of the next HEA automatically. Write through the MEMHEAAI register changes the attribute bits in the CAM word as follows:

- Empty Bit : 0 (Entry is valid.)
- Permanent Bit : Return to the default value defined in the CNTL1 register.
- Access Bit : Return to the default value defined in the CNTL1 register.

•Read/Write CAM Data through the MEMAR_AT, MEMHHA_AT, and MEMHEA_AT registers

Read/Write operation to the attribute bits of the CAM word, whose address is designated by the AR, the HHA, and the HEA registers respectively, is executed by these registers. Examples of this operation would be to make the designated CAM word Invalid, to make the designated CAM word Permanent, and/or to change the Access bit of the designated CAM word. Users can mask each attribute bit. (Refer to Chapter 7 for more details.)
This capability also enables the attribute of the CAM word to be read.

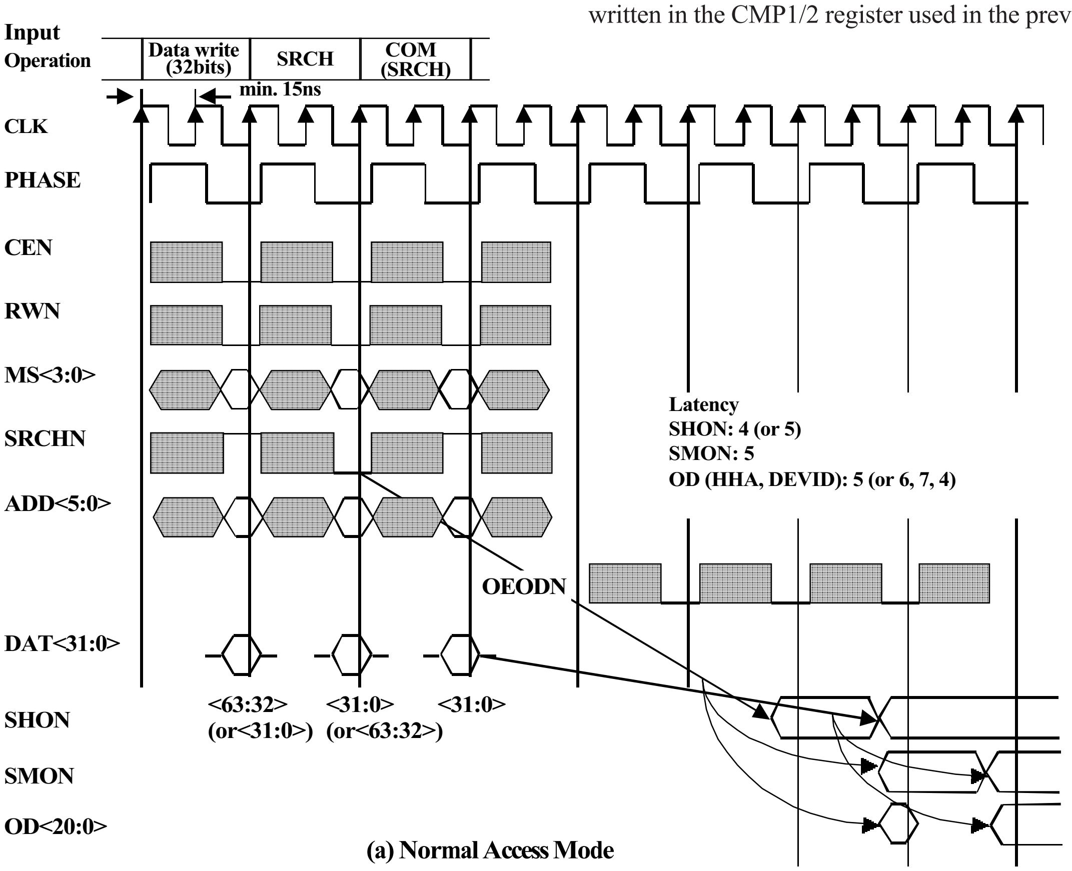
4.4 Search

• Search Operation through the CMP 1/2 register

The key data should be written to the CMP1/2 register from the CPU bus. The low pulse of the SRCHN pin synchronized with the rising edge of CLK while the PHASE signal is low activates the search operation when the key data is written. The mask condition for the search is also chosen from 12 kinds of mask conditions defined by the MASK registers (MASK0 - MASK11), dynamically by the status of the MS<3:0> pins or statically by the CNTL1 register.

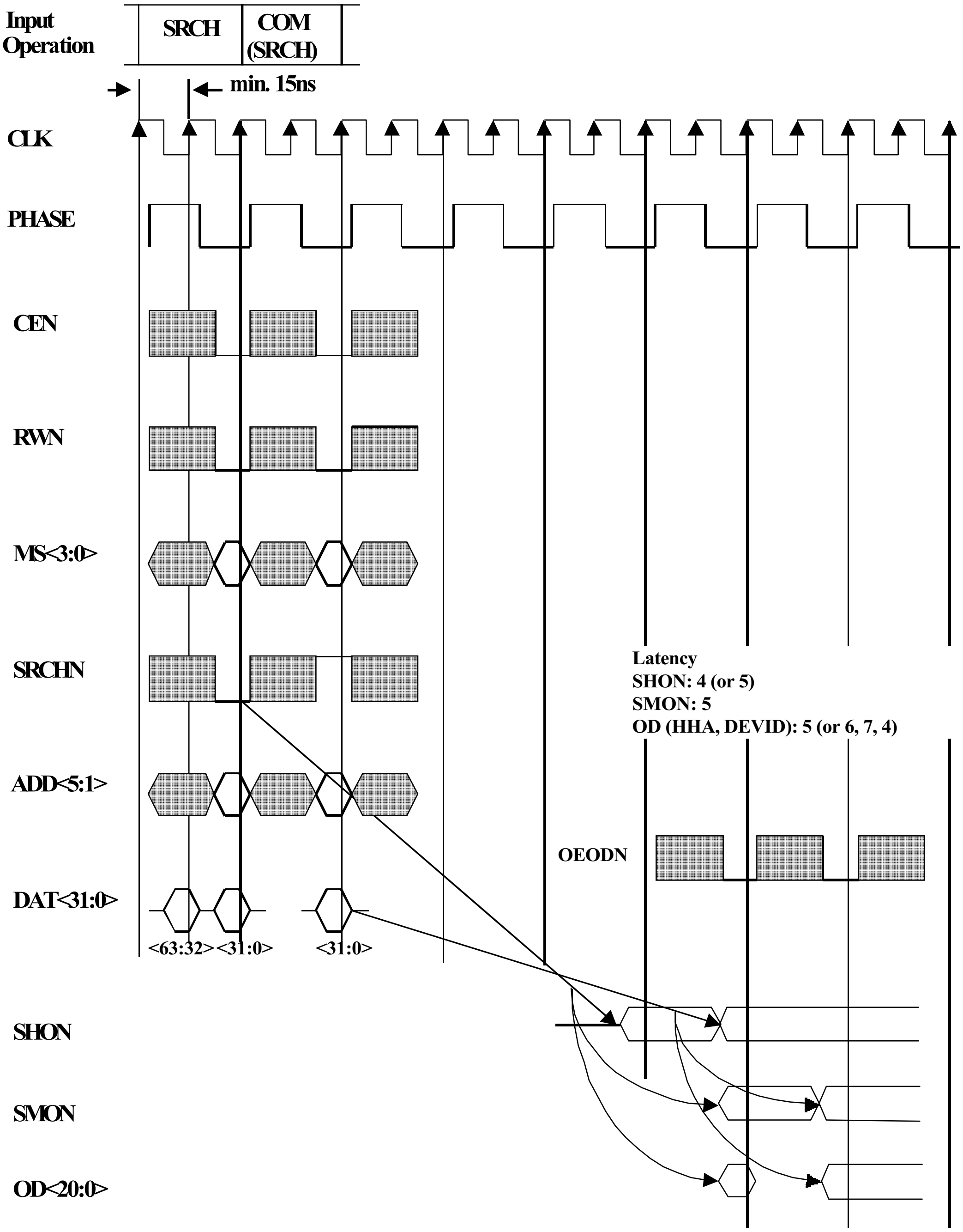
The CMP1/2 register stores the key data until the next write operation is done. Users can choose to perform a Search Operation in the Normal Access mode or the Fast Write mode. The example is shown in Fig. 4.4.1 (a/b).

In Fig. 4.4.1, the search operation is started by the data write to the CMP1/2 register and the synchronous low pulse to the SRCHN pin. As a result, the Hit flag is output on the SHON pin with Latency 4, the Multi-Hit flag is output on the SMON pin with Latency 5, and the HHA and the DEVID of the device which has a hit are output on the OD<20:0> with Latency 5. Fig. 4.4.1 shows two methods for searching the CAM. In this example, the first search is executed by a pulse from the SRCHN pin using the data previously written to the CMP1/2 register. The second search operation is executed by the command, SRCH 1/2. This time, the search operation by command is executed with the data already written in the CMP1/2 register used in the previous search.



(a) Normal Access Mode

Fig. 4.4.1 SRCH Operation through CMP Register Write



(b) Fast Write Mode

Fig. 4.4.1 SRCH Operation through CMP Register Write

• Search Operation by commands

The search command, SRCH 1/2, written to the command register (COM register) activates the search operation using the key data stored in the CMP1/2 register.
The mask condition for the search is chosen at the time of command write from 12 kinds of mask conditions defined by the MASK registers (MASK0 - MASK11). The mask register is chosen dynamically by the status of the MS<3:0> pins on the rising edge of the CLK signal while the PHASE signal is low or statically by the CNTL1 register. Like the search operation above, users can choose the write mode from the Normal Access mode or the Fast Write mode. In both modes, the search operation is started by the command (SRCH). The example is shown in Fig. 4.4.2 (a/b).

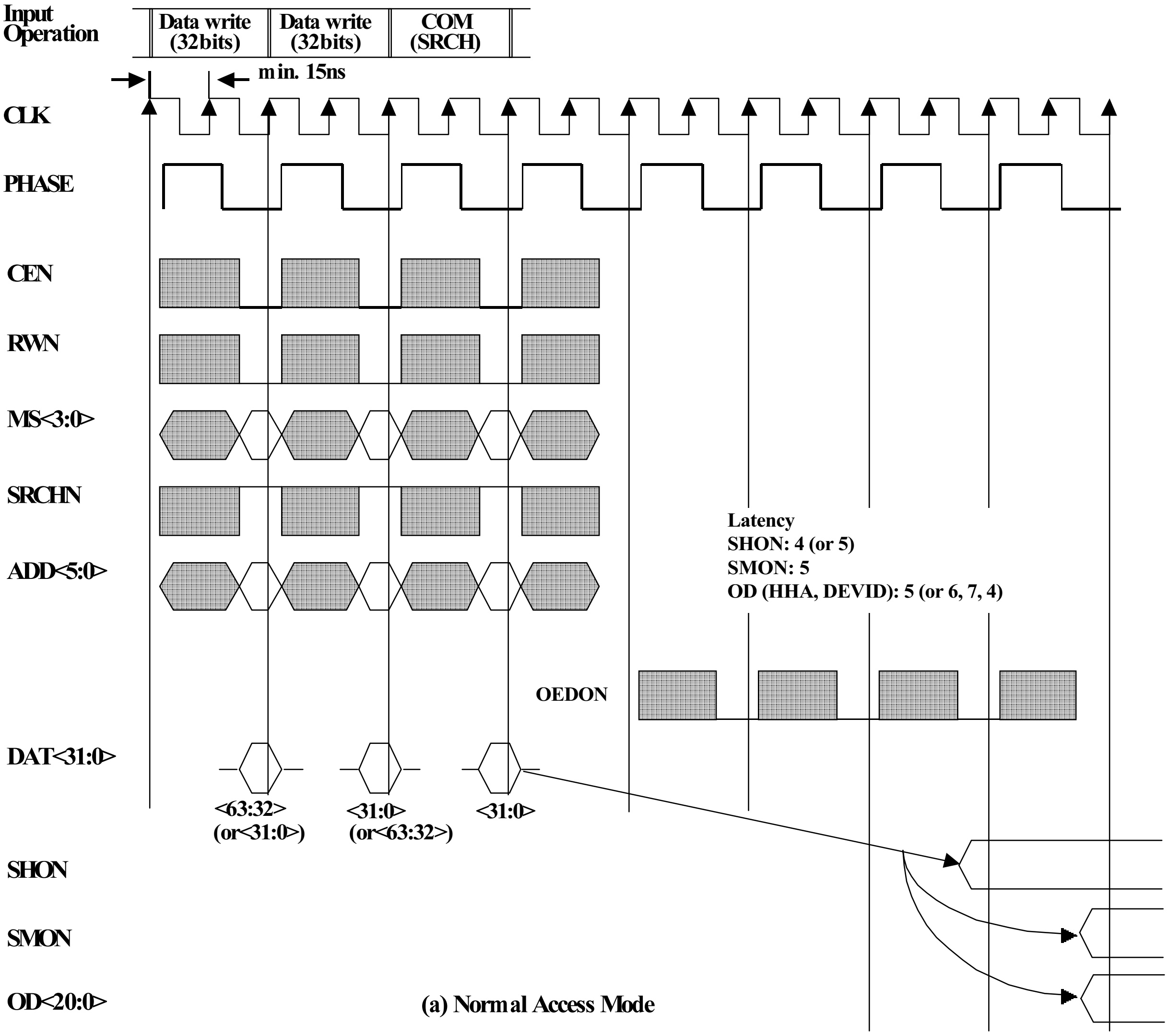
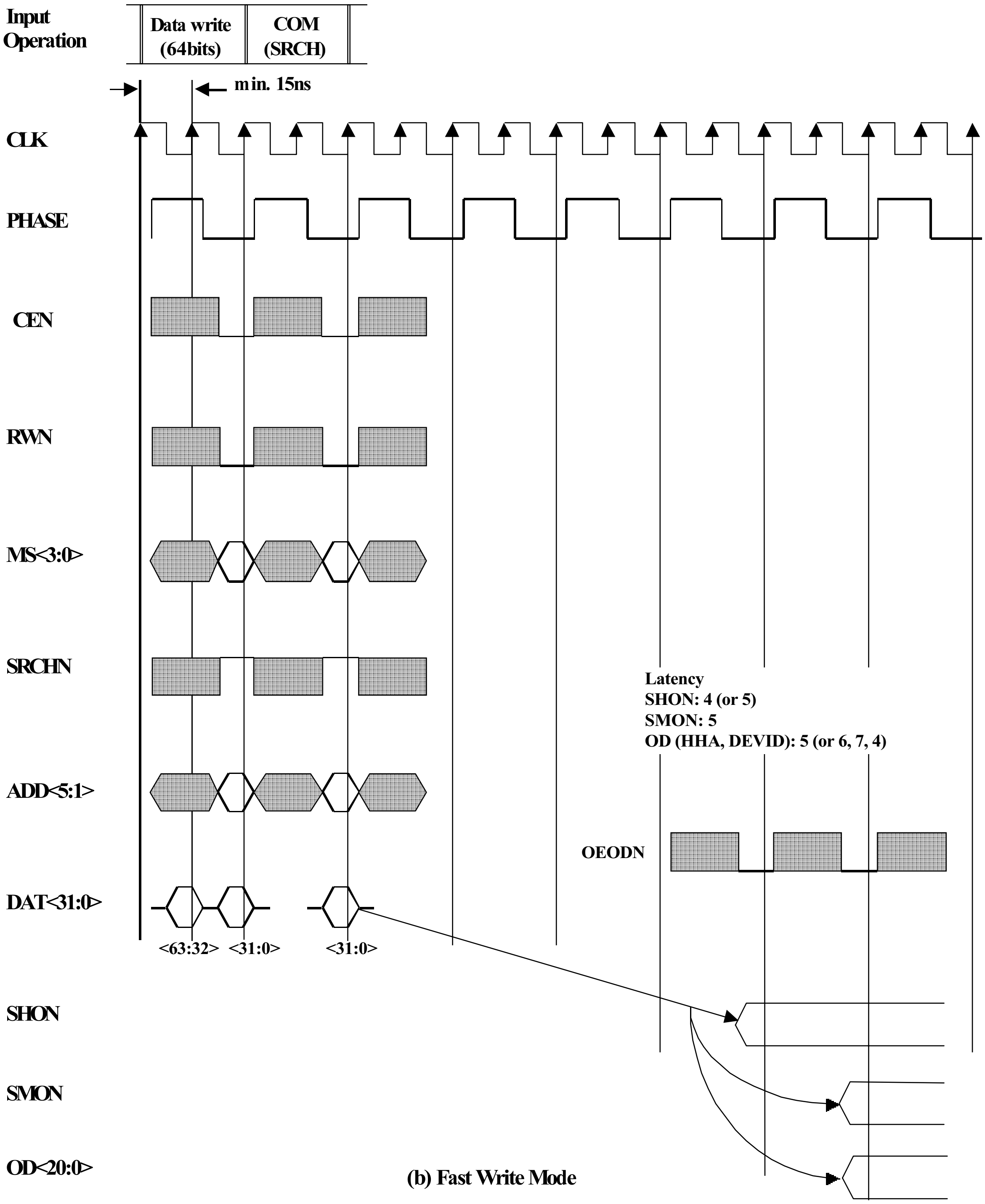


Fig. 4.4.2 SRCH Operation with COMMAND



(b) Fast Write Mode

Fig. 4.4.2 SRCH Operation with COMMAND

• Access Bit set while searching

When a hit occurs in the CAM word while searching, the hit result of the entry can be stored as the Access Bit data. This means the past career of the hit results can be managed. For every 12 MASK registers, the determination of whether the search result is stored in the Access Bits or not (whether the Access Bits must be set according to the hit result) can be done using the SCONF register. (Refer to Chapter 7 for more details.)

• Search Result Flag pins (PHON, PMON, SHON, SMON)

The PHON and SHON pins indicate if the Hit word (the CAM word which is hit) exists. A high level on the PHON pin indicates that a single hit does not exist and a low level on this pin indicates that a single hit exists and multi-hit does not exist. A high level on the SHON pin indicates that no hit exist and a low level on this pin indicates that a single hit or Multi-Hit exist. The PHON pin goes to an unknown status when the search operation starts, and it outputs high or low level according to the search result. The PHON pin outputs the search results asynchronously with the CLK. The SHON outputs the corresponding search result synchronously with CLK. (See Fig. 4.4.2. Refer to Chapter 5 for more details)

The PMON and SMON pins indicate if Multi-Hit entries exist. A high level of these pins indicates that a multi-hit does not exist and the low level of this pin indicates that a multi-hit exists. The PMON and SMON pin goes to an unknown status when the search operation starts, and it outputs high or low level according to the search result The PMON pin outputs the search results asynchronously with the CLK. The SHON outputs the corresponding search result synchronously with CLK. (See Fig. 4.4.2.)

HHA register

The HHA register stores the address of the CAM word that is hit by the search operation. The HHA register has the valid bit that indicates the validity of the data stored in the HHA register. This valid bit becomes “0” if single hit (no multi-hit word exist) exists. If a multi-hit or no hit exists, the valid bit becomes “1” , invalid. The HHA register also stores the data output to the PHON and PMON pins according to the search result, namely Hit and Multi-Hit flag data (Labeled SYH and SYM in section 7.3 Register Bit Maps). In a cascaded system in which multiple devices are interconnected, the Last Device in the chain holds the Hit and Multi-Hit flags of the total system.

Careful consideration is required for the HHA register, because the HHA (Highest Hit Address) becomes invalid data when a multi-hit exists. The search configuration register, SCONF, allows the user to set the Access Bit according to the search operation results. Even though a multi-hit is set as invalid, all the Access Bits of Hit words are still set.

Hit and Multi-Hit status of the total system is valid only when the HHA register in the Last Device is accessed with the timing which considers the propagation delay between the devices.

MEMHHA register

The MEMHHA register is used to read and write the hit CAM. The mask condition in the 12 MASK registers is also used for a partial write to modify part of the hit CAM word. The write through the MEMHHA register is prohibited when the address stored in the HHA register is invalid, because this may cause access to the undesired CAM word and the data in it might be destroyed.

Output from Output Port

The Output port is a 21-bit output bus used for the search result. The main purpose of this port is to output the HHA. Usually, 5 bits out of the 21 indicate the Device ID (the ID data provided to recognize the device in the system with multiple devices), and the other 16 bits output the HHA that indicates the hit address in the device. The Output port is controlled by the OEODN pin.

The HHA, the HEA, and part of the MEMHHA (16 bits) can be output from the Output port. The SCONF register defines which data set listed above will be output.

The SCONF register holds the following 5-bit information for each of the 12 mask conditions. These bits determine what kind of search result is output from the Output port, caused by the corresponding mask condition:

AS* (1bit): Whether the Access Bits are set or not
HE* (1bit): Whether the HEA is output or not when no hit
MH* (1bit): Whether part of the MEMHHA is output or not
S*<1:0> (2bits): Which part of the MEMHHA is output
00:MEMHHA<15:0>, 01:MEMHHA<31:16>,
10:MEMHHA<47:32>,11:MEMHHA<63:48>
(* : 00 - 11)

The output data selection with the OPSL pin is necessary to output the MEMHHA. (See Fig. 4.4.3)

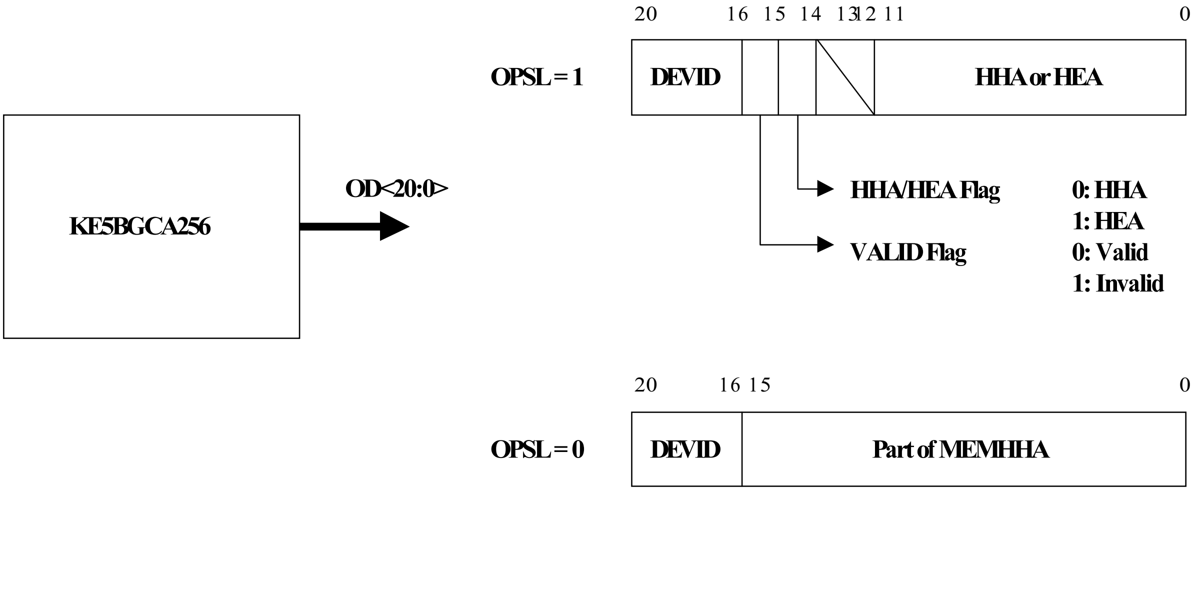


Fig.4.4.3 Output Port Format

The latency (how many clock cycles of delay from the data input) can be defined by the CNTL2 register. The latency of the HHA output (or the HEA output) can be selected from 4, 5, 6 and 7. The latency of the MEMHHA output can be selected from 6 and 7. (See Fig. 4.4.4)

If the Output port is connected to the same bus in a cascaded system, the output control with the OEODN pin or with the latency selection is required so that the bus conflict does not occur. (Refer to Chapter 5 for more details.)

• Definition of the Mask Register for Search and Write

KE5BGCA256 has 12 Mask registers. There are two methods of Mask selection for each of the four register groups. One way is to select it dynamically with MS<3:0> pins. The other way is to select it statically by the definition in the CNTL1 register.

The registers are broken up into four groups as follows:

A Group: The search (or write) with the CMP1 or CMP2 register

B Group: The search with the SRCH1 command or the SRCH2 command

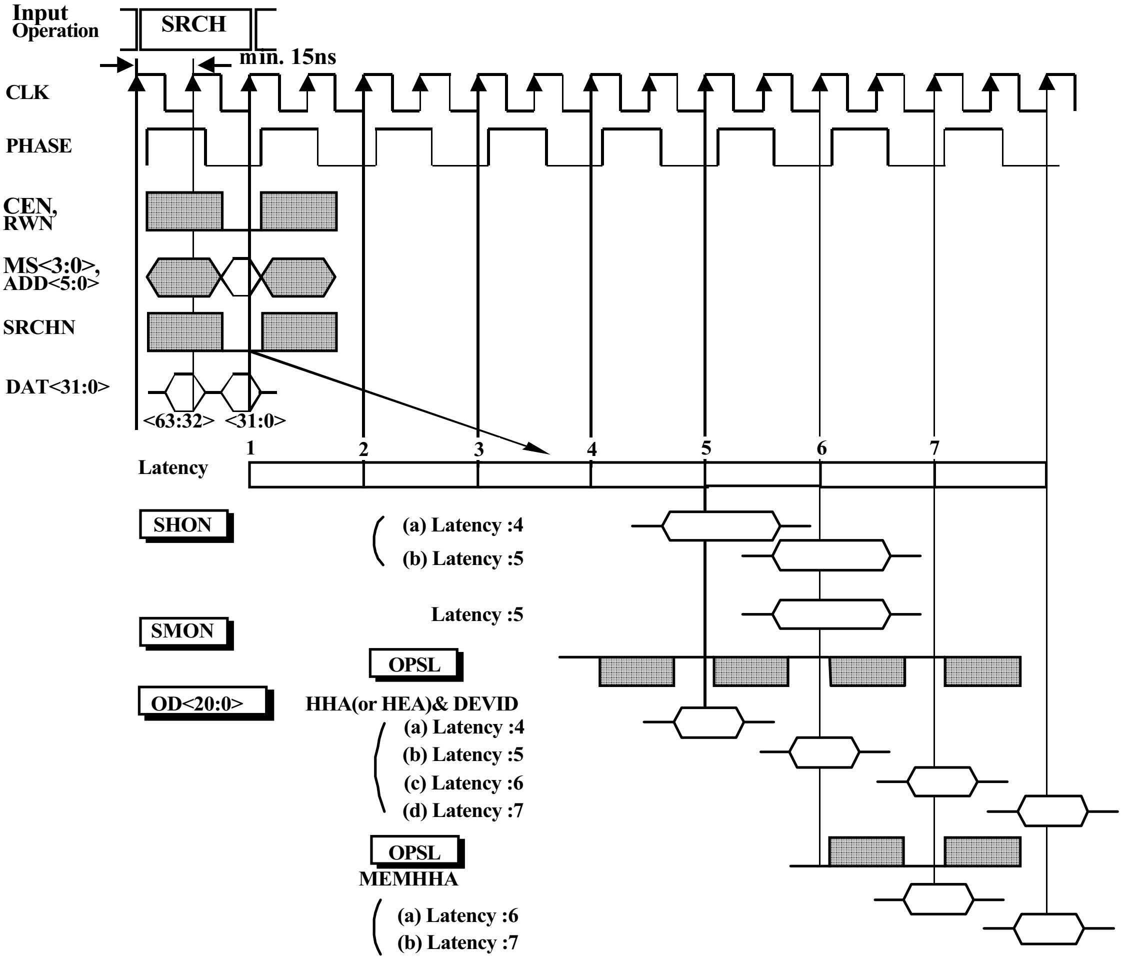


Fig.4.4.4 Output Latency of SRCH Operation

C Group: The write with the STR commands
D Group: The write with the MEM registers

Each of these groups has one bit in the CNTL1 register that is used to define the method of selection, either from the pin MS<3:0>, or from the register. If the mask condition is selected from the register, there are four bits for each group in the CNTL1 register that selects one of the 12 Mask registers. (Refer to Chapter 7 for more details.)

If the mask condition is defined to be selected by the pins, following bits corresponds to each Mask register.
The data of MS<3:0> pins should be input synchronously with the rising edge of CLK when the PHASE signal is low level as described above.

MS<3:0> pins	MASK register
0000	MASK 0 register defines the mask condition.
0001	MASK1 register defines the mask condition.
0010	MASK2 register defines the mask condition.
0011	MASK3 register defines the mask condition.
0100	MASK4 register defines the mask condition.
0101	MASK5 register defines the mask condition.
0110	MASK6 register defines the mask condition.
0111	MASK7 register defines the mask condition.
1000	MASK8 register defines the mask condition.
1001	MASK9 register defines the mask condition.
1010	MASK10 register defines the mask condition.
1011	MASK11 register defines the mask condition.

If the bit of the MASK register is “1,” the bit is “don’t care” and not searched. If the bit of the MASK register is “0,” the bit is "care" and searched. One of the 12 MASK registers must always be defined in the search operation.

MASK registers are also used for the mask condition of the write operation to the CAM memory. If the mask is set (The bit is “1.”), the corresponding bit of the CAM memory is not changed by the write operation. One of the 12 MASK registers must always be defined in the write operation.

4.5 Data Management by Commands

KE5BGCA256 has several commands for data management. This chapter describes the important points. (Refer to Chapter 6 for more details.)

• Data management using Access Bits

The following three commands are provided regarding the Access Bits:
PRG_AC: Erases all the CAM words whose Access Bits are “1.”
PRG_NAC: Erases all the CAM words whose Access Bits are “0.”
RST_AC: Clears all the Access Bits (Access Bit: 0).

An example of using these commands would be to perform a search with the definition that the hit career is being held in the Access Bit, then delete unnecessary CAM words whose Access Bits are “1” (or “0”). Another example is to delete all the CAM words which hit (or did not hit) after the search with certain data.

• Data management using Store Commands

STR1/2_HHAcommand

This command overwrites the data of the CMP1/2 register to the hit CAM word using the mask condition of the defined Mask register. In other words, this command is a partial (maskable) write to the hit address, and it is useful for time stamping to the CAM word. The time stamping data can be used, for example, to find the oldest CAM words by searching this, and delete them.

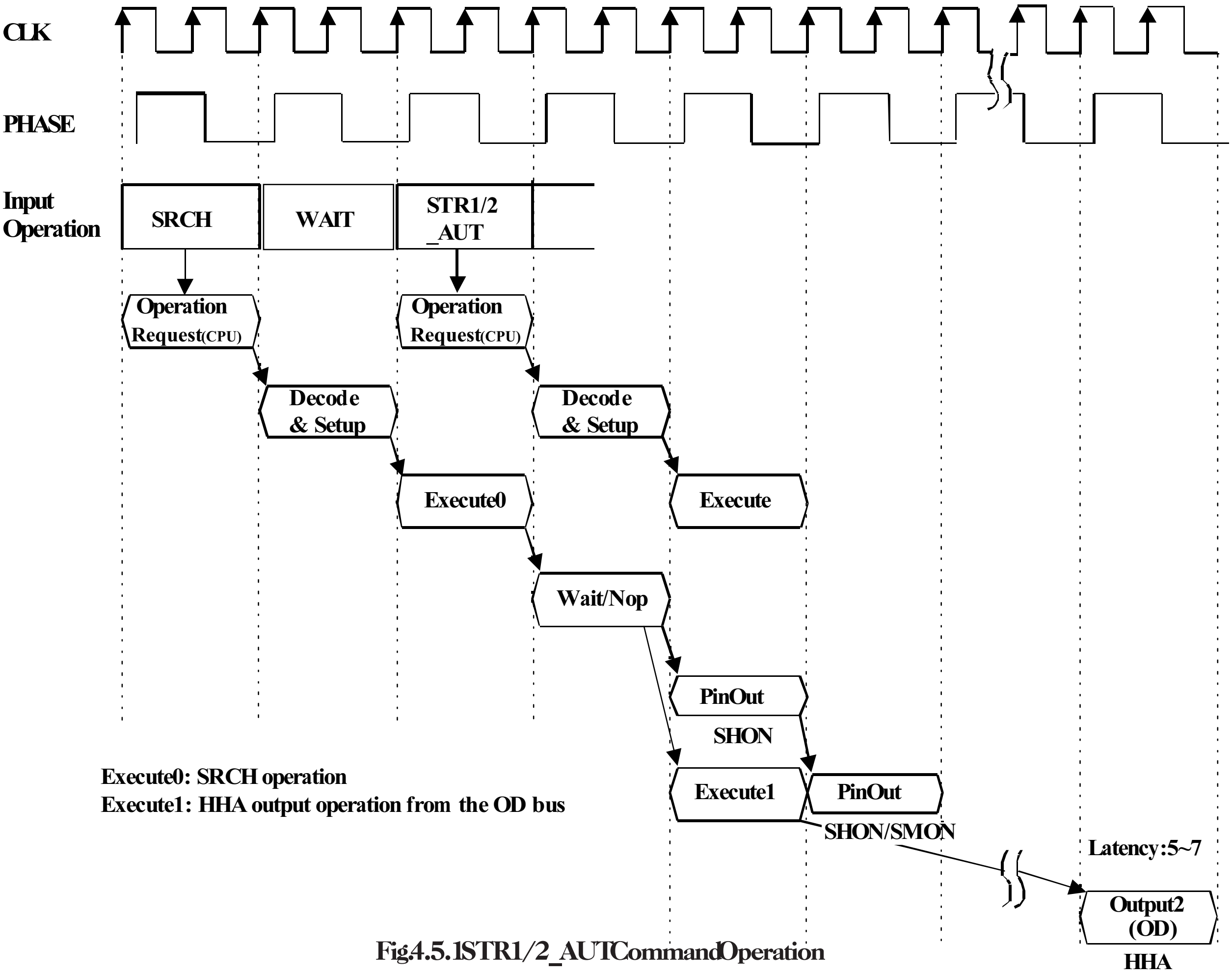
STR1/2_HEAcommand

This command overwrites the data of the CMP1/2 register to the empty CAM word using the mask condition of the defined Mask register. In other words, this command is a partial (maskable) write to the empty address, and it is useful to register new CAM word data when there is no hit CAM word in the search.

The commands STR1/2_HHA and STR1/2_HEA should be executed according to the search result. KE5BGCA256 operates with the Pipeline method synchronously with the external system clock causing multiple steps of latency before receiving the results of each operation. If the command is executed after receiving the result of each operation, it will affect the performance.

STR1/2_AUTcommand

To avoid the performance problem described above, the STR1/2_AUT command is provided in this device.
This command executes the same operation as the STR1/2_HHA command if the device has a hit, and executes the



Execute0: SRCH operation
Execute1: HHA output operation from the OD bus

Fig.4.5.1STR1/2_AUTCommandOperation

same operation as the STR1/2_HEA command if the device does not have a hit. Users can execute this command regardless of whether the device has a hit or not, so that the overhead caused by the unnecessary judging cycles can be reduced.
The example is shown in Fig. 4.5.1. The status of the internal pipeline is also shown in the example. (Refer to Chapter 4.6 for more details.) The STR1/2_AUT command is executed one wait after the external request for the search. The one wait in this example is inserted because the idle time of one PHASE signal is necessary to utilize the search result information such as a Hit. However, the STR_AUT command should only be used when the cascade connection uses external logic. (Refer to Chapter 5 for more details.)

For these STR commands, users can use the mask condition defined by MS<3:0> pins or the CNTL1 register. When using the CNTL1 register, this would be group C.

4.6 Restriction in Pipeline Operation

KE5BGCA256 is designed to use a maximum main clock of 66 MHz. This clock is synchronized with external requests, resulting in operations which are processed by the internal Pipeline. Internal Pipeline processing has several stages corresponding to various requests for operation. When users request multiple operations continuously from the outside, these operations must be requested so that a conflict between the Pipeline stages does not occur.
This Chapter describes the ways the internal pipeline stages work to process the external request, and the rules for continuous input of the various operations.

• Stages of pipeline

The following are five groups of stages of the Pipeline for the operation request:

(1) Operation Request Stage
In this stage, the operation is requested through the CPU bus, with the data and the address input being latched. There are two kinds of stages, Read request stage and Write request stage. The difference between these two stages depends upon whether the DAT bus is occupied. The Read request stage does not occupy the DAT bus, but the Write request stage occupies the DAT bus.

(2) Decode & Setup Stage
This stage follows the Operation Request Stage. The data or the address that is latched in the Operation Request Stage is decoded to recognize the request, and then the necessary data is set up in this stage.

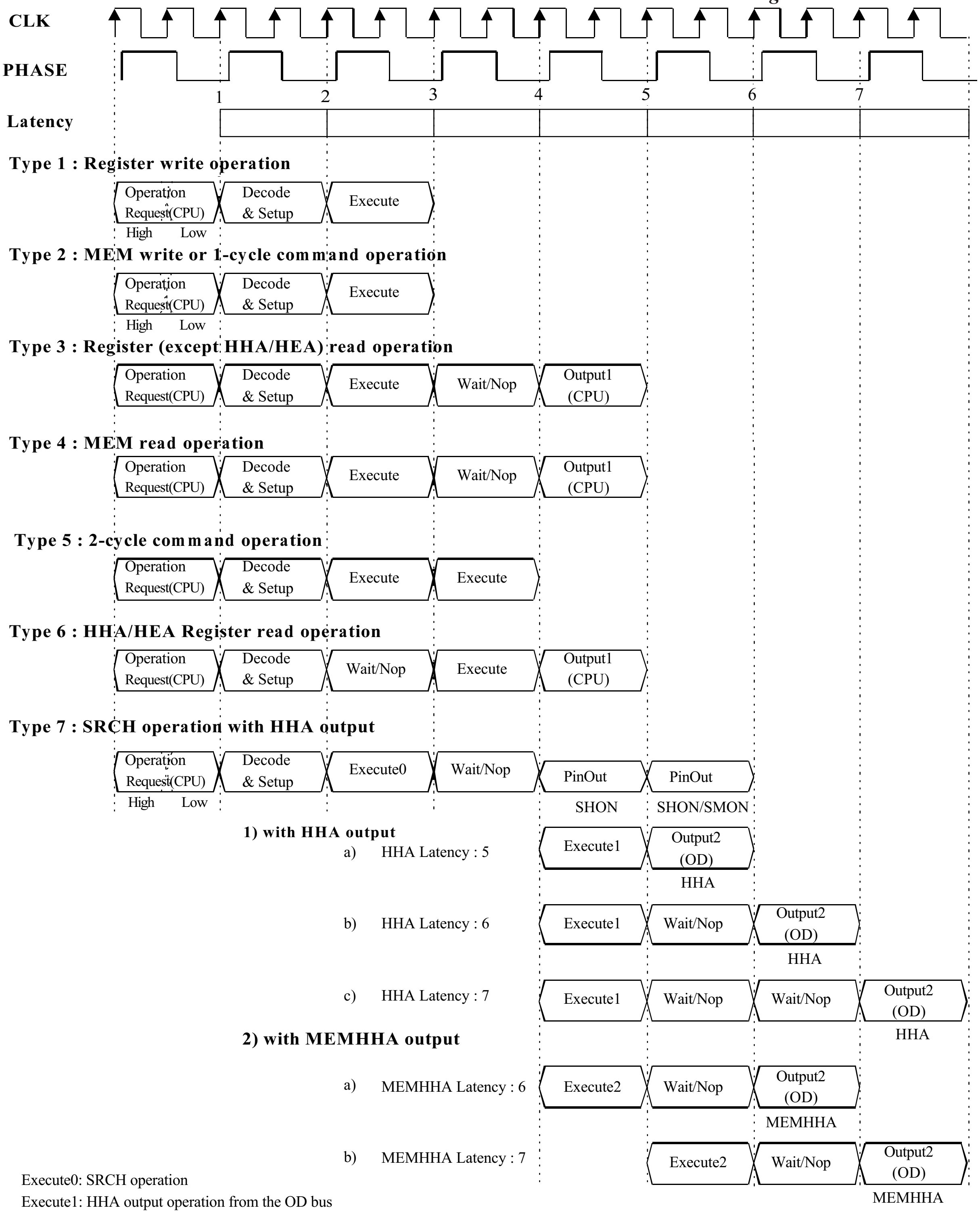
(3) Execute Stage
In this stage, the external request for operation is executed. There are two kinds of operations, the operations that can be executed with the other pipeline stage, See Fig. 4.5.1, and the operations that cannot be executed with the other pipeline stage, according to which block in the device is executed.

(4) Wait/Nop Stage
This stage is for the timing adjustment of the internal bus driving.

(5) Output Stage
Two stages, Output1 and Output2, are included. Output1 is the stage for the output of the DAT bus, and Output2 is the stage for the output of the OD bus. Output1 and Output2 can be executed simultaneously because these ports, DAT bus and OD bus, are different ports.

• Processing and Pipeline Stages

The following seven Types are the categories of operation according to the Pipeline Stages:



Execute0: SRCH operation
Execute1: HHA output operation from the OD bus
Execute2: MEMHHA output operation from the OD bus

Fig. 4.6.1(a) Pipeline Operation Stage Chart

Type1: Registers write operation
Type2: MEM* write operation *1 or 1 cycle command operation
Type3: Registers (except HHA and HEA) read operation
Type4: MEM* read operation *1
Type5: 2 -cycle command operation *2
Type6: HHA/HEA register read operation
Type7: SRCH operation with HHA read (with HEA read)

*1): The read/write of the MEMHEAAI register is in Type5.
*2): SRST, GEN_FL, NXT_HE, STR1_HEAAI, STR1_AUTAI, STR2_HEAAI, STR2_AUTAI commands

The Pipeline Stage timing of each Type is shown in Fig. 4.6.1. As shown in Fig. 4.6.1(a), the Operation Request Stage in Type 1, 2, 7 is divided into two stages (High and Low) because the 64-bit data could possibly be written to the register or to the CAM word using the Fast Write Mode (64-bit access per one PHASE signal cycle).

• Restriction of simultaneous execution of Pipeline Stages

There are some restrictions of simultaneous executions of the internal Pipeline Stages. Basically, the simultaneous execution of the different Pipeline Stages is possible if they are in different Pipelines, but the simultaneous execution must meet the following restrictions:

1) The Write Request of the Operation Request Stage and the Output1 Stage must not be executed simultaneously because they use the same bus (DAT bus).

2) Any operation can execute simultaneously during Wait/Nop Stages.

3) The possible simultaneous operations of the Execute Stages between the multiple Pipelines are restricted to the following 3 cases:

a) The Execute of Type5 and the Execute of Types 1- 7
b) The Execute of Type6 and the Execute of Types 1- 7
c) The Execute1 and the Execute2 of Type7 and the Execute of Types 1- 6

These executions must follow the restriction shown in Table 4.6.1. The column of the Table 4.6.1 means Execute stage which is possible to simultaneously execute. As shown in Fig. 4.6.1 (b), the the column of the table means 1st Input Operation, and the row of the table means 2nd Input Operation.

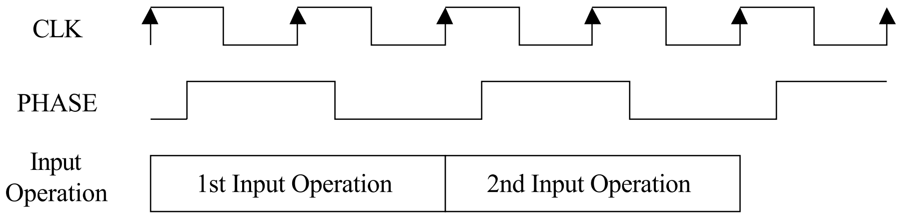


Fig. 4.6.1(b) Restriction of pipeline

2nd Input Operation \ 1st Input Operation	Type 5 : 2-cycle command operation *4)	Type 6 : HHA/HEA Register read operation	Type 7 : SRCH operation with HHA output	
				with MEMHHA output
Type 1 : Register write operation	○	○	○ *3)	○ *3)
Type 2 : MEM_HHA, _HEA, _AR, _ARAI write or 1-cycle command operation	△ *1)	○	○	X
Type 3 : Register (except HHA/HEA) read operation	○	○	○	○
Type 4 : MEM_HHA, _HEA, _AR, _ARAI read operation	○	○	○	○
Type 5: 2-cycle command operation, MEMHEAAI	X	△ *5)	○	○
Type 6 : HHA/HEA Register read operation	○	X	○	○
Type 7 : SRCH operation with HHA output	X *2)	△ *6)	X	X
with MEMHHA output	X	△ *6)	X	X

*1) Only the NXT_HE command and MEM write can be simultaneously executed.
*2) Impossible to simultaneously execute with the Execute 0 of the SRCH operation.
*3) Impossible to simultaneously execute with the write to the CNTL2 register.
*4) In case of the SRST command, reset operation has priority.
*5) Execute of the HEA read operation cannot be simultaneously executed Execute of the GEN_FL, NXT_HE, STR1/2_HEAAI, STR1/2_AUTAI (mis-hit case), and MEMHEAAI access.
*6) Execute of the HHA read operation cannot be simultaneously executed Execute of search operation.

○	: allowed
△	: allowed partially
X	: not allowed

Table 4.6.1 Restriction of pipeline

• Restriction in usage of the result of data operation in each Pipeline

Data Write and Read

The write and read operations of the data are classified into Type1/2 and Type3/4. As shown in Fig. 4.6.2, DATA WRITE (2), (3) Input Operation can be put on after DATA READ Input Operation to use pipeline of the device effectually. However, (4) ~ (5) Input Operation stage cannot be used because data output of DATA READ (1) starts on the WAIT stage (5).

Definition of Search Condition and Search Operation

The search operation can executed immediately after the search condition has been changed with the write to the CNTL1 register , the MASK register, or to the SCONF register. It is not possible to change the output latency during the search operation. The search condition (latency) must be kept unchanged until the Output operation of the search result has been completed (See Fig. 4.6.4).
The output latency is defined in the CNTL2 register.

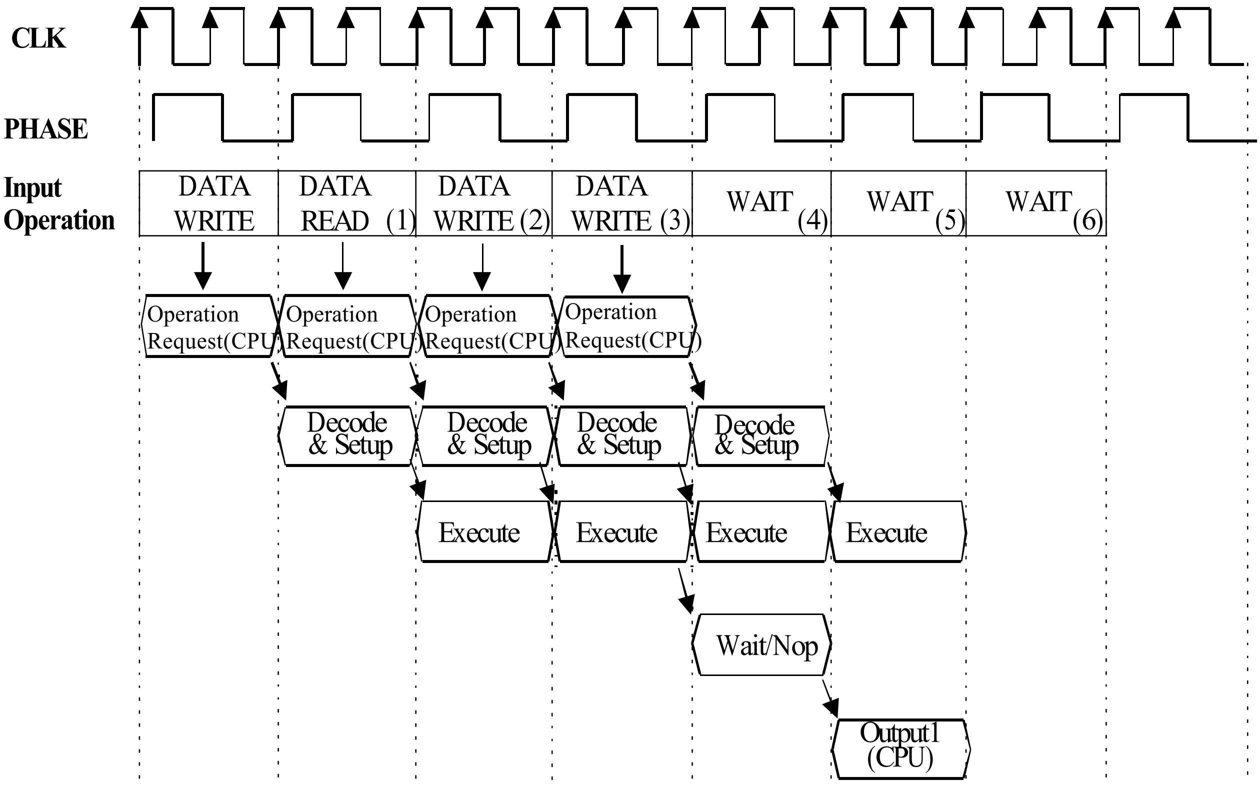


Fig.4.6.2 Restrictions between Data Read/Write Operations

Search and Use of the Search Result

For continuous operations executed through the CPU, some operations are restricted. These types of operations must be executed according to the result of the previous operation. An example would be when reading the HHA through the CPU port using the MEMHHA register after the search operation. Using this example, the restriction of the usage of the result of data processing is described. As shown in Fig. 4.6.1, the HHA is determined in the Wait/Nop Stage, one cycle after the Execute0 stage for a search operation which is Type7. If the reading of the MEMHHA is requested right after the request of the search operation, as shown in Fig. 4.6.3 (a), the Execute of the read operation of the MEMHHA is executed at the same time as the Wait/Nop stage of the SRCH. The value in the HHA has not been decided yet, so this Execute is not executed correctly. This is because the reading operation of the MEMHHA uses the HHA. In the cases as above, one wait is necessary before an operation which uses the HHA, such as the request for reading the MEMHHA register (See Fig. 4.6.3 (b).). If the search is performed after an operation which uses the HHA, such as reading the MEMHHA register, one wait is not necessary.

Change the HEA and Use of the HEA

In the same way as the HHA, two waits are necessary before an operation which uses the HEA, such as the request for reading the MEMHEA register (See Fig. 4.6.3 (c).).
If an operation which changes the HEA is performed after an operation which uses the HEA, two waits are not necessary.

Operations which change the HHA or the HEA and Operations which use the HHA or the HEA

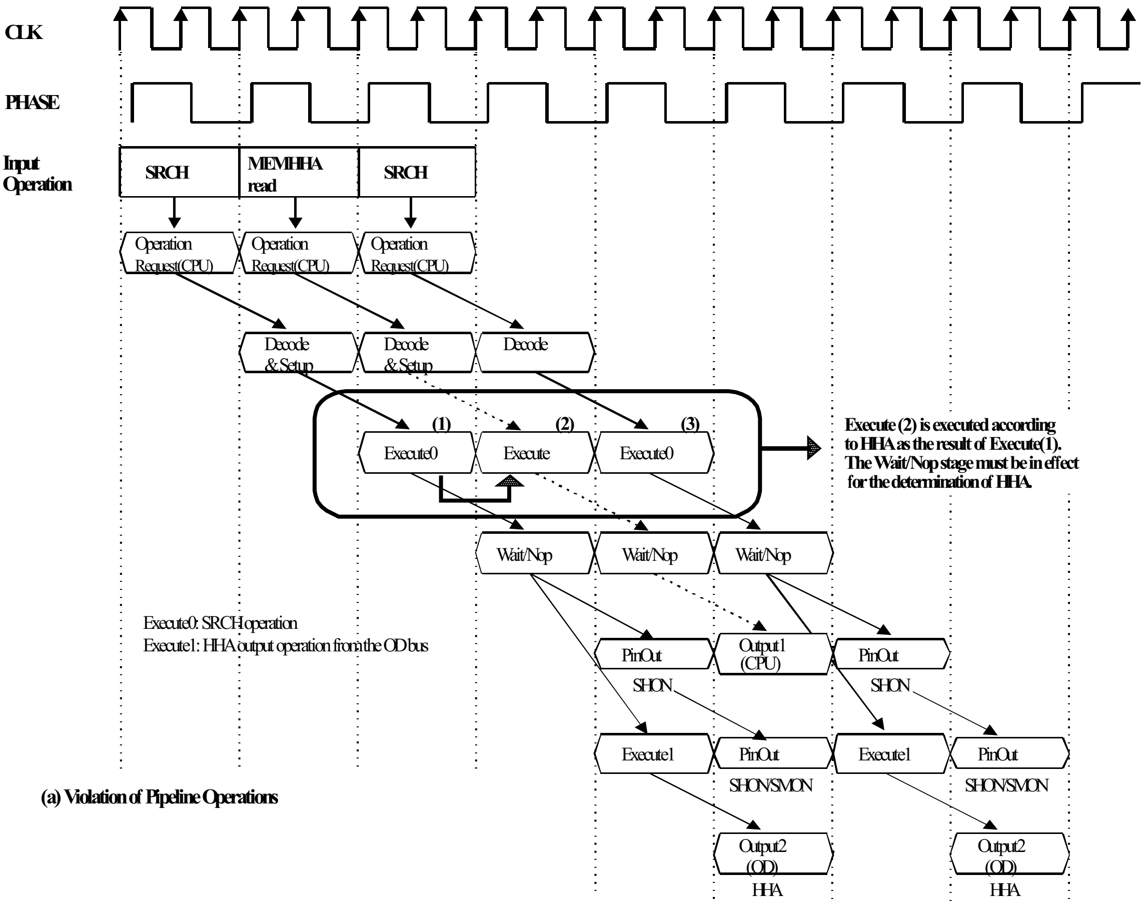
The operations which change the HHA or change the HEA and the operation which use the HHA or use the HEA, are listed as follows.

Operations which change the HHA
Search operation with the SRCHN pin
SRCH1/2command

Operations which change the HEA
MEMHEAAI register access
GEN_FL,NXT_HE,STR1/2_HEAAI,STR1/2_AUTAI commands

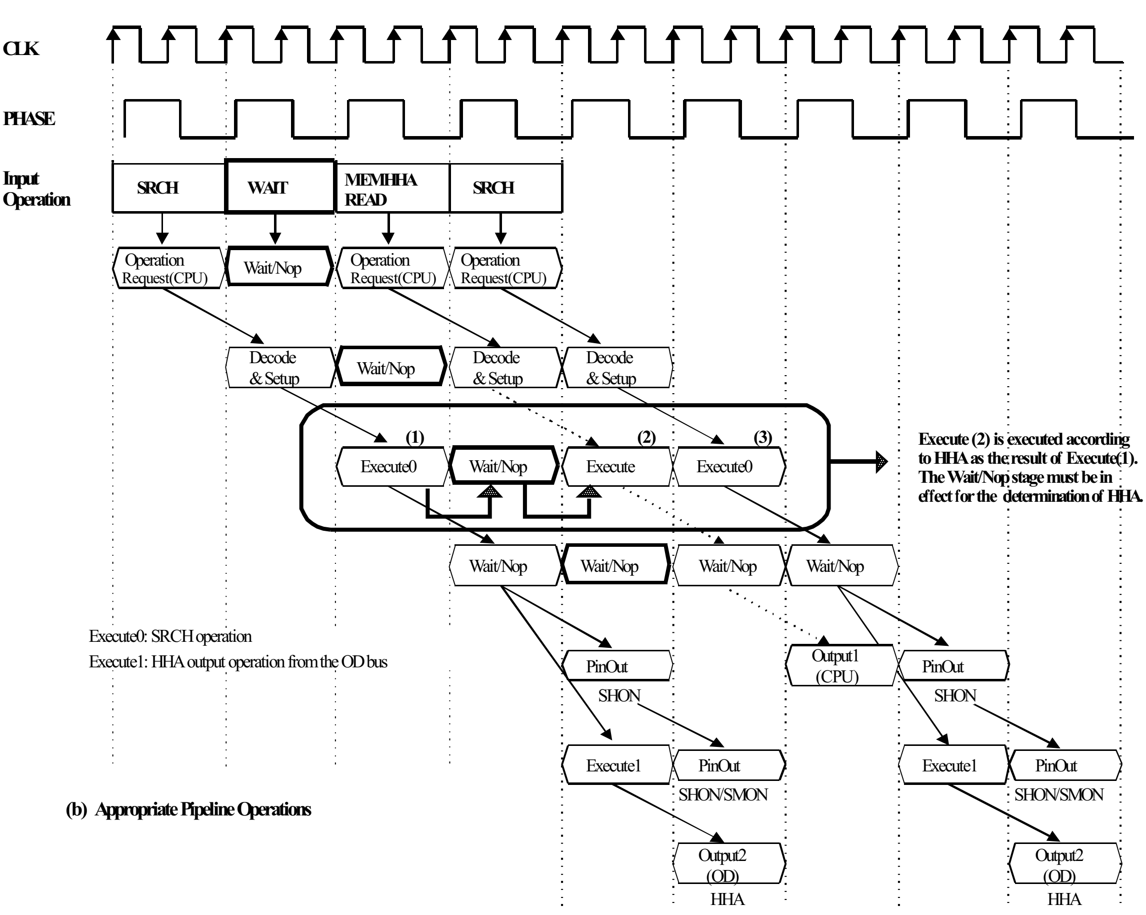
Operations which use the HHA
MEMHHA register access
STR1/2_HHA, STR1/2_AUT (hit case),
STR1/2_AUTAI (hit case) commands

Operations which use the HEA
MEMHEA register access
MEMHEAAI register access
STR1/2_HEA, STR1/2_AUT (mis-hit case),
STR1/2_AUTAI (mis-hit case) commands



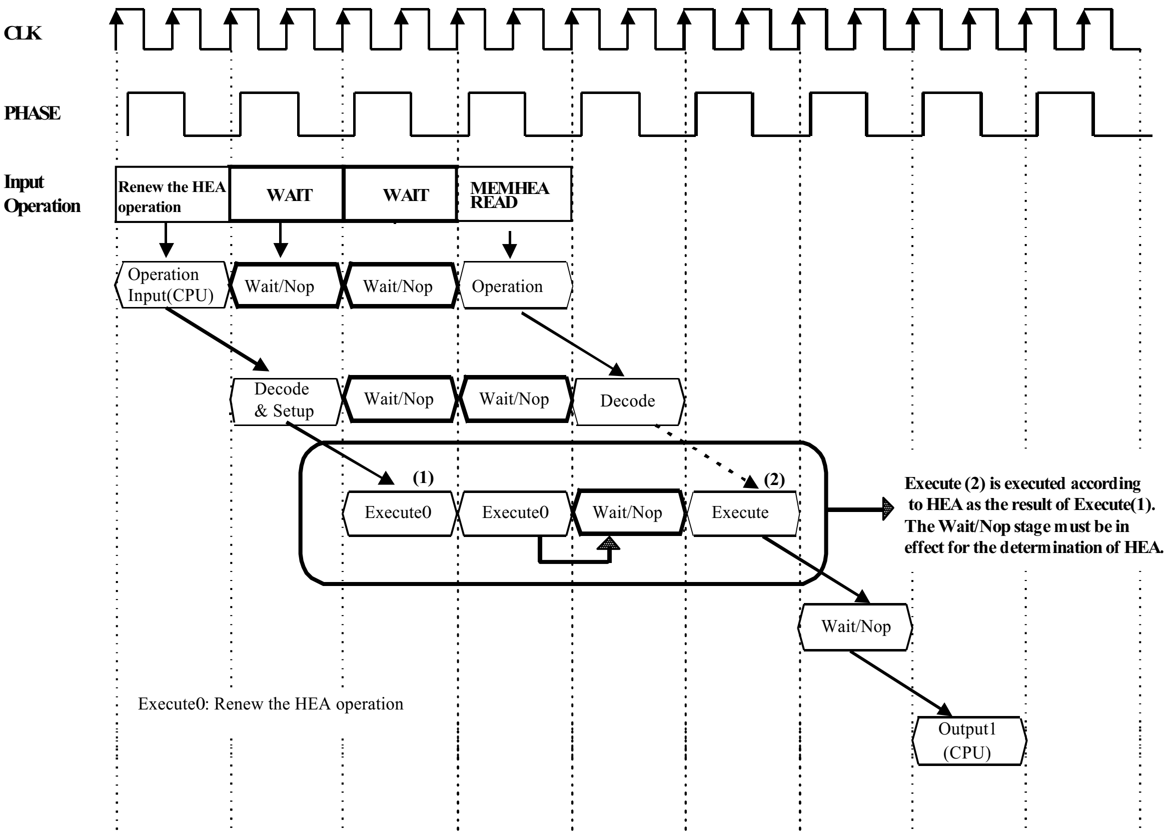
(a) Violation of Pipeline Operations

Fig. 4.6.3(a) Restriction Example between Pipeline Operations



Execute (2) is executed according to HHA as the result of Execute(1). The Wait/Nop stage must be in effect for the determination of HHA.

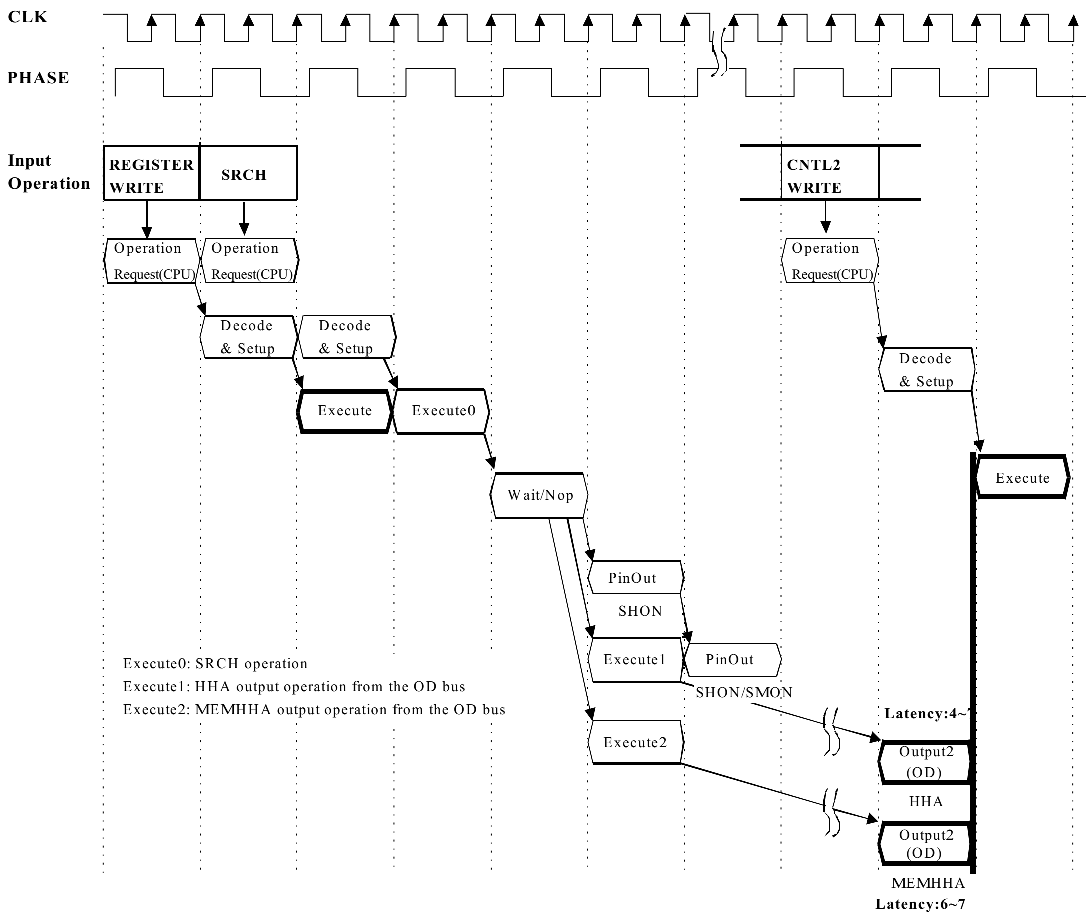
Fig. 4.6.3 (b) Restriction Example between Pipeline Operations (cont'd)



Execute (2) is executed according to HEA as the result of Execute(1). The Wait/Nop stage must be in effect for the determination of HEA.

(c) Appropriate Pipeline Operations

Fig. 4.6.3 (c) Restriction Example between Pipeline Operations (cont'd)



Execute0: SRCH operation
Execute1: HHA output operation from the OD bus
Execute2: MEMHHA output operation from the OD bus

Fig.4.6.4RestrictionsbetweenSRCHOperationandSearchConditionDefinitionOperation

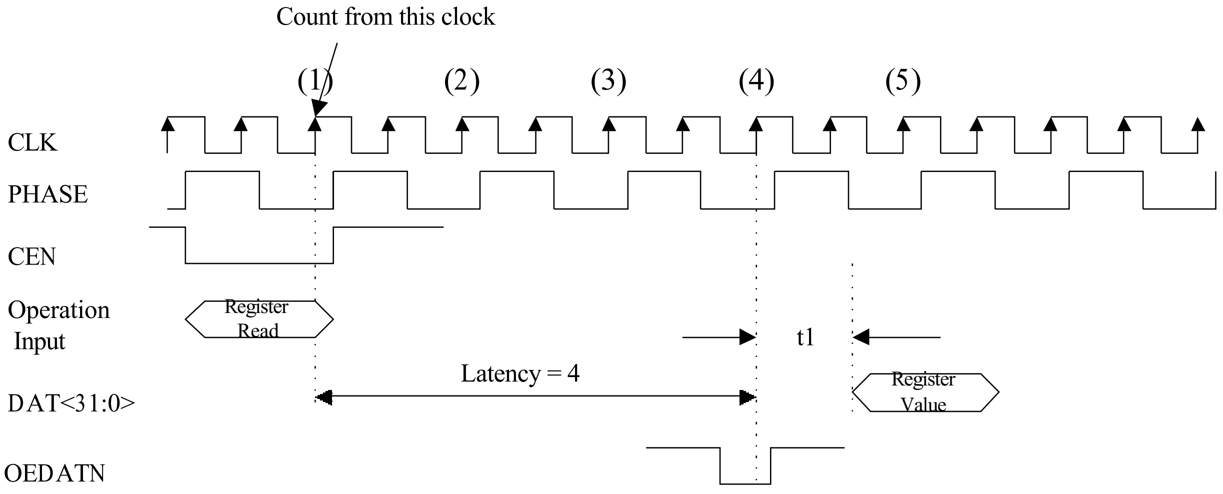
4.7 Latency

This device operates with the CLK signals as the master clock. Therefore, there is latency which is characteristic for a synchronous circuit between some action and the following action. Latency is counted by the number of rising edge of the CLK signals when the PHASE signal is low from the input operation, as shown in Fig. 4.7.1, 4.7.2 For example, Fig. 4.7.1 shows that the output latency of the CPU port is 4. Fig. 4.7.2 shows that the output latency of the Output port is 5.

Table 4.7.1 shows the output latency.

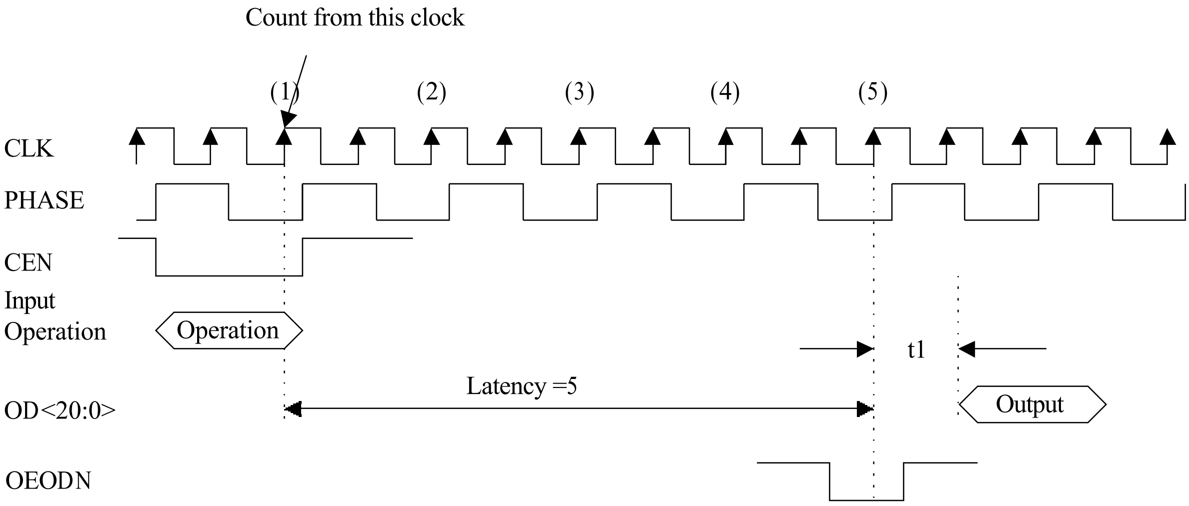
There is also execution latency in read/write operation by commands or registers. (See Fig. 4.6.1)

The user that the values for latency can be modified by writing to the CNTL2 register.



t1: output delay time from CLK which is provided in Chapter 9

Fig. 4.7.1 Output Latency on the CPU Port



t1: output delay time from CLK
which is provided in Chapter 9

Fig. 4.7.2 Output Latency on the Output Port

Pins	Latency
DAT<31:0>	· Latency is fixed to be 4. · Latency (OEDATN => DAT<31:0>) is 1.
OD<20:0>	· Latency can be selected from 4, 5, 6, and 7 in HHA/HEA output. · Latency from the operation to renew the HEA is equal to the HEA/HHA latency. · Latency can be selected from 6 and 7 in MEMHHA output. · Latency (OEODN => OD<20:0>) is 1.
SHON	· Latency can be selected from 4 and 5. · Latency is 2.5 when the SRST command is executed. (See Fig. 9.4.3) · Latency is 0.5 from the RSTN low pulse. (See Fig. 9.4.3)
SMON	· Latency is fixed to be 5. · Latency is 2.5 when the SRST command is executed. (See Fig. 9.4.3) · Latency is 0.5 from the RSTN low pulse. (See Fig. 9.4.3)
FLON	· When MEM_HEAAI is accessed or the GEN_FL, NXT_HE, STR1_HEAAI, STR2_HEAAI, STR1_AUTAI, or STR2_AUTAI command is executed, latency is 2.5. · Latency is 2 when the SRST command is executed. · Latency is 0 from the RSTN low pulse.
PHON	· When the search operation by the SRCHN pin or the SRCH command is executed, latency is 2.5. · Latency is 0 from the RSTN low pulse.
PMON	· When the search operation by the SRCHN pin or the SRCH command is executed, latency is 2.5. · Latency is 0 from the RSTN low pulse. · When the SRST, STR_DEVID, END_DEVID, and NXT_PR command is executed, latency is 2.

Table 4.7.1 Output Latency

5. Connection

5.1 Initialization

There are two types of initialization for this device: Hardware reset by setting the RSTN pin to a low level, and Software reset by executing the SRST command.
Hardware reset must be done after the power is on.
Hardware reset or Software reset executes the following initialization:

1) Initializes Device ID *1
2) Initializes registers
3) Sets Empty Bits of all entries (all entries are empty)
4) Clears Permanent Bits of all entries
5) Clears Access Bits of all entries
6) PHON = 1, SHON = 1
7) PMON = 1, SMON = 1
8) FLON = 1

*1 Device ID must be registered after reset when devices are cascaded.

The GEN_FL command must be executed after registration to the CAM table.

5.2 Single Device Operation

A device reset either by a Hardware reset using the RSTN low pulse or software reset using the SRST command automatically sets the Device ID to “00000” and the LD bit to “1”. The LD bit means the Last Device in a cascaded system. Therefore, it is not necessary to set the Device ID by using the DEVID mode in the single device operation. The PHIN and PMIN pins must be pulled up and the FLIN pin must be pulled down with a single device.

When used in a single device operation, the device acts as one with hit/empty priority if there is any hit/empty entry in the device. On the other hand, it acts as the Last Device if there is no hit/empty entry in the device. Therefore, the behavior is the same in the broadcast method as in the device select method, but some commands must be executed in the device select method according to the condition of Table 6.2 , and some registers must be accessed in the device select method according to the condition of Table 7.4.1, even in this case.

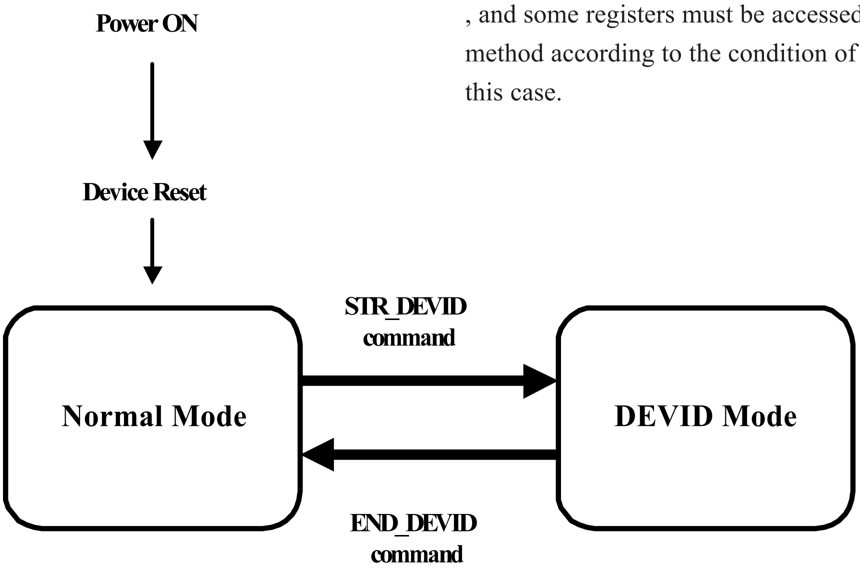


Fig 5.3.1.1 Device ID registration

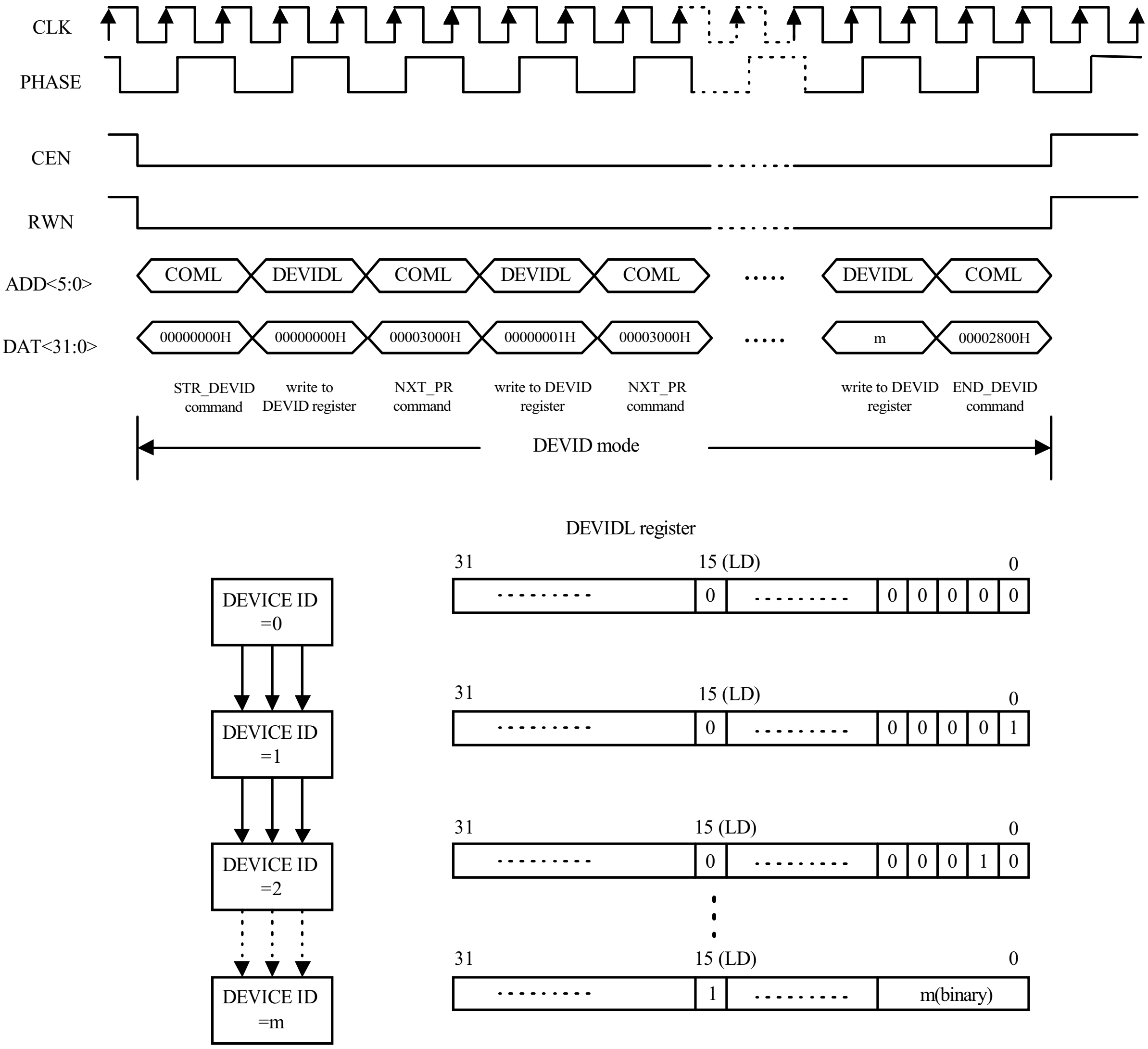


Fig.5.3.1.2 Device ID registration procedure

5.3 Cascade Connection

5.3.1 Device ID Registration

The device can be cascaded to use a maximum of 32 devices. A cascaded system can be treated as one device which has a larger table size. It is necessary to define the Device ID in the DEVID register in order to identify each device in the operation of a cascaded system. The procedure for registration of the Device ID is shown in Fig. 5.3.1.2.

In order to set the Device ID, the devices in a cascaded system must be moved into the DEVID mode by the STR_DEVID command as shown in Fig. 5.3.1.1. The STR_DEVID command enables the user to apply read/write operations to the DEVID register of the highest (top) device in the cascaded system. The Device ID is set in the DI<4:0> of the register. After that, the Device ID of the next device can be set by the NXT_PR command. The registration should be repeated down the chain until each device is given a unique Device ID by repeating these operations. If the STR_DEVID command is executed among these operations, it returns to the status where the DEVID register of the highest (top) device can be read/written.
The Device ID must be a continuous number starting from the top device. The LD in the Last Device DEVID register must be set to “1.” This bit indicates that the device has the lowest priority, and it is used to control the data outputs. The LD bits of all devices except the Last Device must be set to “0.”

After the DEVID registers of all devices are set, the devices should be moved out of the DEVID mode and into the normal operation mode by executing the END_DEVID command. The devices must leave the DEVID mode after all Device IDs are set, because operations like Table Configuration or search cannot be executed correctly in the DEVID mode. Waiting time is recommended to ensure that the PMIN and PMON pins become stable.

The Device IDs of all devices are initialized to the same value of “00000” after device reset. The operations described above, from the STR_DEVID command, must be executed after device reset. If only one device is used, the Device ID registration is not necessary.
Do not register the Device ID in normal operation mode once the Device ID is set after device reset.

5.3.2 Priority

In a cascaded system, the data buses of the CPU Port and the Output Port must be connected to all devices. As for the CPU Port, the same data is written to all devices through DAT<31:0> and the same Pipeline is executed in all devices. The output device is automatically determined in the broadcast method and the device in which the MEMHHA or the MEMHEA register is written, or the device in which the STR_HHA, the STR_HEA, or the STR_AUT command is executed, is also determined automatically. As for the Output Port, all devices output the search results respectively. The Output Port must therefore be controlled by the users’ logic using the SHON when there is a multi-hit in the system, when there are many devices with a single hit, or when HEA is set to be output in a no hit case.

The empty priority is controlled in this device, but the hit priority is not controlled in order to realize a higher speed. The HHA as a result of the multi-hit in the device therefore becomes invalid, and the write operation to the entry designated by the HHA is not executed. The above-mentioned priority control is, however, executed in the cascaded system including the device in which the multi-hit occurs. It is also possible not to write, regarding the multi-hit in the system as illegal status by the cascade connection method described later.

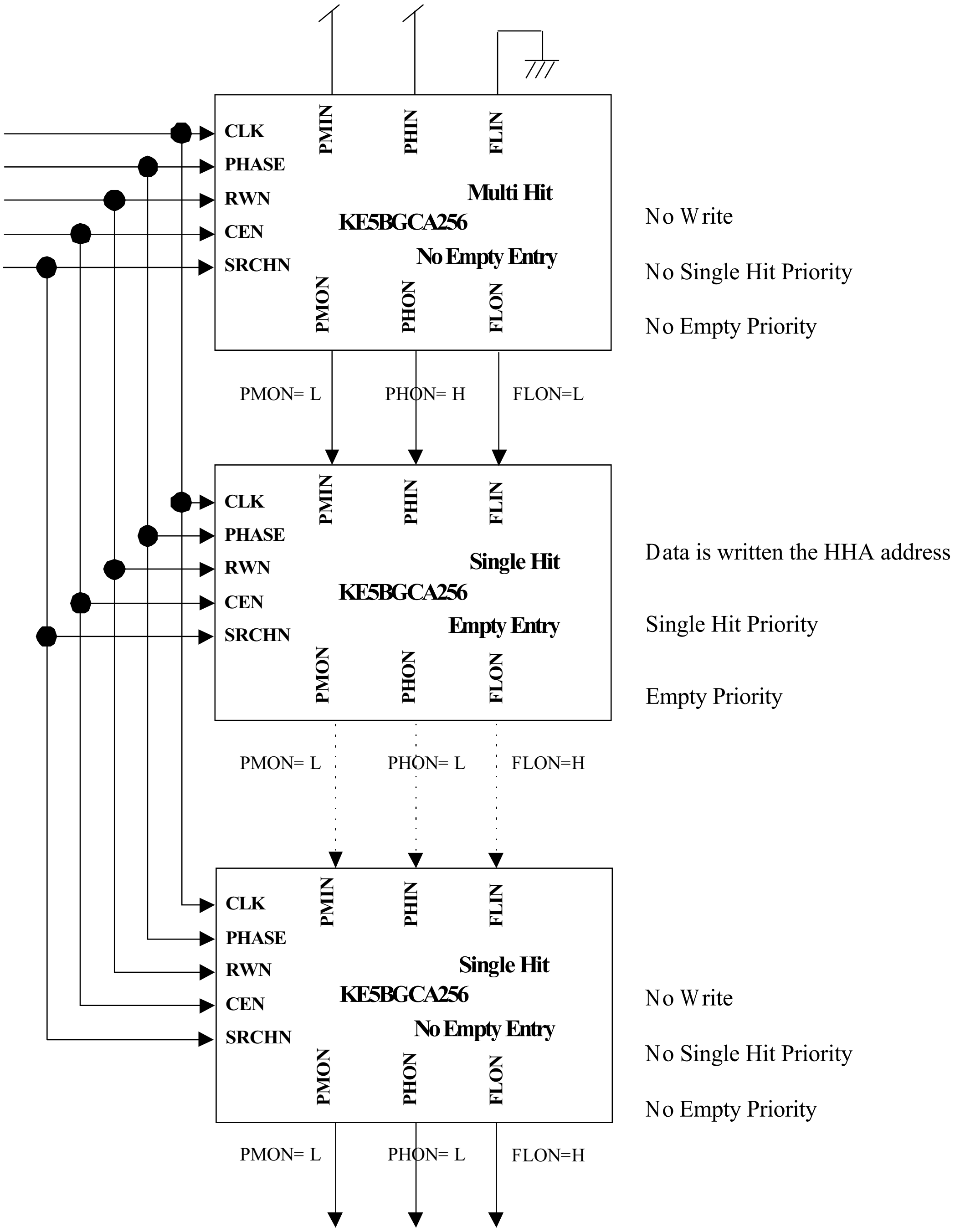


Fig.5.3.2.1 Cascade Connection

Three priorities are used for these controls: the single-hit priority, the empty priority, and the DEVID priority. THE PHIN, PMIN, FLIN, PHON, PMON, and FLON pins are used to propagate the priorities.

(1) Single Hit Priority

In a cascaded system, the uppermost located device among all devices that have hit entries, except the devices in which the multi-hit occurs, is defined as having hit priority. (See Fig. 5.3.2.1) This priority is propagated through the PHON and the PHIN. When a multi-hit does not occur in a device and the upper devices have single hit priority, the PHON of the device outputs "0." When neither single hit nor multi-hit occurs in the device and the upper devices do not have single hit priority, the PHON of the device outputs "1."
In order to have a device having single hit priority, the PHIN of the device must be set to "1."

(2) Empty Priority

In a cascaded system, the uppermost located device among all devices that have empty entries is defined as having empty priority (See Fig.5.3.2.1). This priority is propagated through the FLON and the FLIN. When a device is full status and the upper devices are full, the FLON of the device outputs "0." When the device is not full or the upper devices are not full, the FLON of the device outputs "1." In order to have a device having empty priority, the FLIN of the device must be set to "0."

(3) DEVID Priority

DEVID priority specifies which device accepts the Device ID data in the DEVID mode. DEVID priority is propagated through the PMIN and PMON pins in the DEVID mode. However, the PMIN and PMON pins propagate multi-hit information in something other than the DEVID mode.

(4) Last Device

The device located at the bottom of the cascaded chain must be known in order to perform internal control of the device. The LD bit in the DEVID register of the bottom device must be set to "1" to indicate that it is the "Last Device."
For example, the Last Device stores the total hit and empty information of the cascaded system in the HHA and HEA registers. The Last Device outputs the bits: HV, EV, SYH, SYM, SYE, HT, MH, the address with hit priority or empty priority when the HHA or HEA register is read in the broadcast method. If there is no device having single hit priority, the Last Device outputs the data of the HHA register in the broadcast method. The HV flag of the output data is "1" and that indicates that the HHA is invalid. In the same manner, if there is no device having empty priority, the Last Device outputs the data of the HEA register in the broadcast method. The EV flag of the output data is "1" and that indicates that the HEA is invalid. In a cascade system, for registers that have the same data in each device, such as the CNTL1/2 and the SCONF register, when these registers are read in the broadcast method, the Last Device outputs the register's data.

5.3.3 CPU Port in a Cascaded System

Read/Write Registers

Read/write operations (including command execution) can be performed by both the broadcast and the device select method.
This selection is defined in the DEVSEL register. The BR bit in the DEVSEL register must be set to "0" in the device select method The selected device can be specified by the DS<4:0> in the DEVSEL register. The BR must be set to "1"

in the broadcast method. When data is written to a register, one of the following operations is executed according to the attribute of the register:

(1) Write to all devices simultaneously
(2) Write to the device which has single hit priority
(3) Write to the device which has empty priority

When data is read from a register, one of the following operations is executed according to the attribute of the register:

(1) Read from the Last Device
(2) Read from the device which has single hit priority
(3) Read from the device which has empty priority

For registers which must have common data for all devices, the device select method is invalid and data is written to appropriate register of all the devices. Some registers must be accessed by the device select method. See Table 7.4.1 in Chapter 7 for Read/Write availability of each register in the broadcast method/device select method and the output device that is accessed in the broadcast method.

Command Execution

The command of the device should be executed by the broadcast method in a cascaded system. The device to which the command execution applies is automatically decided internally in this case.

Cascade Connection of the CPU Port

Cascade connection methods of multiple devices are shown below:

(1) Priority control without the external logic
(2) Priority control with the external logic

A cascade connection can be realized by either of the two methods. Table 5.3.3.1 shows the relationship between cascade input pins and their actions. When the priority is controlled by the external logic, the external circuit must be designed referring to Table 5.3.3.1 and Fig. 5.3.3.3.

(1) Connection without the External Logic

In this method, the external logic is not necessary to control the priority (See Fig. 5.3.3.1). However, additional propagation time is needed according to the number of cascaded devices. This is because the priority signal is cascaded through each of the devices. We define two types of multi-hit's: When there are multiple hits within a single device, or when there are two devices in a cascaded system that have a single hit. When two devices have a single multi-hit, the data is written in the HHA address of the uppermost single hit priority device in the cascaded system. For devices that have multiple hits within a single device, data will not be written to the HHA address. Data will be written to the HHA address in the next device in the cascade chain that has a single hit priority. (See Fig. 5.3.2.1) The commands STR1_AUT, STR2_AUT, STR1_AUTAI, and STR2_AUTAI cannot be executed in this connection method.

AC Characteristics in this method

This device can automatically perform its internal control function by using respective priority signals. After the priority is changed by some action, the next operation which needs priority determination must wait a certain time according to the number of cascaded devices. As shown in Fig. 5.3.3.2, the total time between some action and the next operation which needs priority determination is required for priority determination.
t1: latency of the action in the top device
t2: delay time after latency of the action in the top device

t3: propagation delay of priority signal from the top device to the Last Device
t4: setup time for the action which needs priority determination in the Last Device

(2) Connection with the External Logic

In this method, external priority control logic is used to minimize the cascade delay of the system (See Fig. 5.3.3.3). The external control logic must generate the priority signal of each device, PHIN. This is determined from the SHON pin, which is output by each device in hit priority control. In the case of writing to the MEM_HHA register or writing by the STR1_HHA or the STR2_HHA command, the PHIN signal is made with consideration of the writing timing in the device as shown in Fig. 5.3.3.4. When the STR1_AUT or the STR2_AUT command is used in a cascaded system, the PHIN of each device must be controlled with consideration of the action timing in each device as shown in Fig. 5.3.3.4.

AC Characteristics in this method

This device can automatically perform its internal control function by using respective priority signals. After the priority is changed by some action, the next operation which needs priority determination must wait a certain time according to the number of cascaded devices. As shown in Fig. 5.3.3.4, the total time between some action and the next operation which needs priority determination is required for priority determination.
t1: latency of the action in each device
t2: delay time after latency of the action in each device
t3: propagation delay of priority signal from the external priority control circuit to each device
t4: setup time for the action which needs priority determination in each device

Operation by hit priority (in the broadcast method)

Device external pin*1			Operation that needs priority determination	Status in device	Operation
PMIN	PHIN	FLIN			
X	0	X	MEMHHA, MEMHHA_AT(WRITE)	Single hit	No operation
X	0	X		No hit	No operation
X	0	X		No hit	No operation
X	0	X	MEMHHA, MEMHHA_AT(READ)	Single hit	Hi-Z output
X	0	X		Multi-hit	Hi-Z output
X	0	X		No hit	Hi-Z output
X	0	X	HHA(READ) DAT<30,27,26,24>,<23:0> *2	Single hit	Hi-Z output
X	0	X		Multi-hit	Hi-Z output
X	0	X		No hit	Hi-Z output
V *3	0	X	HHA(READ) DAT<31,29,28,25> *3	Single hit	Hi-Z output or if the Last Device, output
V *3	0	X		Multi-hit	Hi-Z output or if the Last Device, output
V *3	0	X		No hit	Hi-Z output or if the Last Device, output
X	0	X	STR1_HHA, STR2_HHA	Single hit	No operation
X	0	X		Multi-hit	No operation
X	0	X		No hit	No operation
X	0	X	STR1_AUT, STR2_AUT	Single hit	No operation
X	0	X		Multi-hit	No operation
X	0	X		No hit	No operation

*1 "X" means "don't care."

*2 Each device drives DAT<30,27,26,24>,<23:0> in the 32-bit CPU Bus since this is respective information of each device.

*3 The Last Device drives DAT<31,29,28,25> in the 32-bit CPU Bus since this is information of the cascaded system. FLIN of the Last Device must be determined for the SYE flag to be output exactly in DAT<25>. PMIN of the Last Device must be determined for the SYM flag to be output exactly in DAT<28>.

Table 5.3.3.1 Operation by hit priority(in the broadcast method)

Device external pin*1			Operation	Status in device	Operation
PMIN	PHIN	FLIN			
X	1	X	MEMHHA, MEMHHA_AT(WRITE)	Single hit	Write
X	1	X		Multi-hit	No operation
X	1	X		No hit	No operation
X	1	X	MEMHHA, MEMHHA_AT(READ)	Single hit	Output
X	1	X		Multi-hit	Hi-Z output or if the Last Device, output invalid data
X	1	X		No hit	Hi-Z output or if the Last Device, output invalid data
X	1	X	HHA(READ) Bit<30,27,26,24>,<23:0> *4	Single hit	Output
X	1	X		Multi-hit	Hi-Z output or if the Last Device, output invalid address
X	1	X		No hit	Hi-Z output or if the Last Device, output invalid address
V *5	1	X	HHA(READ) Bit<31,29,28,25> *5	Single hit	Hi-Z output or if the Last Device, output valid address
V *5	1	X		Multi-hit	Hi-Z output or if the Last Device, output valid address
V *5	1	X		No hit	Hi-Z output or if the Last Device, output valid address
X	1	X	STR1_HHA, STR2_HHA,	Single hit*6	Write to HHA*6
X	1	X		Multi-hit*6	No operation
X	1	X		No hit*6	No operation
X	1	X	STR1_AUT, STR2_AUT, STR1_AUTAI, or ,STR2_AUTAI	Single hit*7	Write to HHA
X	1	X		Multi-hit*7	No operation
X	1	0		No hit with empty entry*7	Write to HEA*8
X	1	0		No hit without empty entry*7	No operation
X	1	1		No hit with empty entry*7	No operation
X	1	1		No hit without empty entry*7	No operation

*4 Each device drives DAT<30,27,26,24>,<23:0> in the 32-bit CPU Bus since this is respective information of each device.

*5 The Last Device drives DAT<31,29,28,25> in the 32-bit CPU Bus since this is information of the cascaded system.
FLIN of the Last Device must be determined for the SYE flag to be output exactly in DAT<25>.
PMIN of the Last Device must be determined for the SYM flag to be output exactly in DAT<28>.

*6 STR*_HHA is STR1_HHA or STR2_HHA . If the search result by the CMP1 register is a single hit, the STR1_HHA command executes the write operation that the data in the CMP1 register is written in the entry indicated by HHA1. If the search result by the CMP2 register is a single hit, the STR2_HHA command executes the write operation that the data in the CMP2 register is written in the entry indicated by HHA2.

*7 STR*_AUT is STR1_AUT or STR2_AUT. If the search result by the CMP1 register is a single hit, the STR1_AUT command executes the write operation that the data in the CMP1 register is written in the entry indicated by HHA1. If there is no hit, write in the entry indicated by HEA1. If the search result by the CMP2 register is a single hit, the STR2_AUT command executes the write operation that the data in the CMP2 register is written in the entry indicated by HHA2. If there is no hit, write in the entry indicated by HEA2.

*8 If STR*_AUTAI is executed, renewal of the HEA address is performed simultaneously.

Table5.3.3.1(cont'd)

Operation by empty priority (in the broadcast method)

Device external pin*1			Operation	Status in device	Operation
PMIN	PHIN	FLIN			
X	X	0	MEMHEA, MEMHEA_AT(WRITE)	With empty entry	Write*11
X	X	0	or MEMHEAAI	Without empty entry	No operation
X	X	0	MEMHEA, MEMHEA_AT(READ)	With empty entry	Output*11
X	X	0	or MEMHEAAI	Without empty entry	Hi-Z output or if the Last Device, output invalid data
X	X	0	HEA(READ)	With empty entry	Output
X	X	0	Bit<30,27,26,24>,<23:0>*9	Without empty entry	Hi-Z output or if the Last Device, output invalid address
V *10	V *10	0	HEA(READ)	With empty entry	Hi-Z output or if the Last Device, output valid address
V *10	V *10	0	Bit<31,29,28,25>*10	Without empty entry	Hi-Z output or if the Last Device, output valid address
X	X	0	STR1_HEA, STR2_HEA,	With empty entry	Write*12
X	X	0	STR1_HEAAI, or STR2_HEAAI	Without empty entry	No operation
X	X	1	MEMHEA, MEMHEA_AT(WRITE)	With empty entry	No operation
X	X	1	or MEMHEAAI	Without empty entry	No operation
X	X	1	MEMHEA, MEMHEA_AT(READ)	With empty entry	Hi-Z
X	X	1	or MEMHEAAI	Without empty entry	Hi-Z
X	X	1	HEA(READ)	With empty entry	Hi-Z
X	X	1	Bit<30,27,26,24>,<23:0>	Without empty entry	Hi-Z
X	X	1	HEA(READ)	With empty entry	Hi-Z output or if the Last Device, output valid address
X	X	1	Bit<31,29,28,25>	Without empty entry	Hi-Z output or if the Last Device, output valid address
X	X	1	STR1_HEA, STR2_HEA,	With empty entry	No operation
X	X	1	STR1_HEAAI, or STR2_HEAAI	Without empty entry	No operation

*9 Each device drives DAT<30,27,26,24>,<23:0> in the 32-bit CPU Bus since this is respective information of each device.

*10 The Last Device drives DAT<31,29,28,25> in the 32-bit CPU Bus since this is information of the cascaded system.
PMIN of the Last Device must be determined for the SYM flag to be output exactly in DAT<28>.
PHIN of the Last Device must be determined for the SYH flag to be output exactly in DAT<29>.

*11 If the MEMHEAAI register is accessed, renewal of the HEA address is performed simultaneously.

*12 If the STR1_HEAAI or the STR2_HEAAI command is executed, renewal of the HEA address is performed simultaneously.

Table5.3.3.1(cont'd)

Operation by hit priority (in the device select method).
In devices that are not selected, no operation is performed for write group operation, and Hi-Z output is performed for read group operation.

Device external pin*1			Operation	Status in device	Operation
PMIN	PHIN	FLIN			
X	X	X	MEMHHA, MEMHHA_AT(WRITE)	Single hit	Write
X	X	X		Multi-hit	No operation
X	X	X		No hit	No operation
X	X	X	MEMHHA, MEMHHA_AT(READ)	Single hit	Output
X	X	X		Multi-hit	Output invalid data
X	X	X		No hit	Output invalid data
X	X	X	HHA(READ) Bit<30,27,26,24>,<23:0>*13	Single hit	Output
X	X	X		Multi-hit	Output invalid address
X	X	X		No hit	Output invalid address
X	X	X	HHA(READ) Bit<31,29,28,25>*14	Single hit	Output
X	X	X		Multi-hit	Output
X	X	X		No hit	Output
X	X	X	STR1_HHA or STR2_HHA	Single hit*15	Write
X	X	X		Multi-hit*15	No operation
X	X	X		No hit*15	No operation
X	X	X	STR1_AUT, STR2_AUT, STR1_AUTAI, or ,STR2_AUTAI	Single hit*16	Write to HHA*16
X	X	X		Multi-hit*16	No operation
X	X	X		No hit*16	Write to HEA*16,17

*13 Each device drives DAT<30,27,26,24>,<23:0> in the 32-bit CPU Bus since this is respective information of each device.

*14 The Last Device drives DAT<31,29,28,25> in the 32-bit CPU Bus since this is information of the cascaded system.

*15 STR*_HHA is STR1_HHA or STR2_HHA. If the search result by CMP1 is a single hit, the STR1_HHA command executes the write operation that the data in the CMP1 register is written in the entry indicated by HHA1. If the search result by CMP2 is a single hit, the STR2_HHA command executes the write operation that the data in the CMP2 register is written in the entry indicated by HHA2.

*16 STR*_AUT is STR1_AUT or STR2_AUT. If the search result by CMP1 is a single hit, the STR1_AUT command executes the write operation that the data in the CMP1 register is written in the entry indicated by HHA1. If there is no hit, write in the entry indicated by HEA1. If the search result by CMP2 is a single hit, the STR2_AUT command executes the write operation that the data in the CMP2 register is written in the entry indicated by HHA2. If there is no hit, write in the entry indicated by HEA2.

*17 If the STR1_AUTAI or the STR2_AUTAI command is executed, renewal of the HEA address is performed simultaneously.

Table5.3.3.1(cont'd)

Operation by empty priority (in the device select method)
In devices that are not selected, no operation is performed for write group operation, and Hi-Z output is performed for read group operation.

Device external pin*1			Operation	Status in device	Operation
PMIN	PHIN	FLIN			
X	X	X	MEMHEA(WRITE) or MEMHEA_AT	With empty entry	Write*20
X	X	X		Without empty entry	No operation
X	X	X	MEMHEA, or MEMHEAAI_AT(READ)	With empty entry	Output*20
X	X	X		Without empty entry	Output invalid data
X	X	X	HEA(READ) Bit<30,27,26,24>,<23:0>*18	With empty entry	Output
X	X	X		Without empty entry	Output invalid address
X	X	X	HEA(READ) Bit<31,29,28,25>*19	With empty entry	Output
X	X	X		Without empty entry	Output
X	X	X	STR1_HEA, STR2_HEA or STR1_HEAAI, STR2_HEAAI	With empty entry	Write*21
X	X	X		Without empty entry	No operation

*18 Each device drives DAT<30,27,26,24>,<23:0> in the 32-bit CPU Bus since this is respective information of each device.
*19 The Last Device drives DAT<31,29,28,25> in the 32-bit CPU Bus since this is information of the cascaded system.
*20 If the MEMHEAAI register is accessed, renewal of the HEA address is performed simultaneously.
*21 If the STR1_HEAAI or the STR2_HEAAI command is executed, renewal of the HEA address is performed simultaneously.

Table5.3.3.1(cont'd)

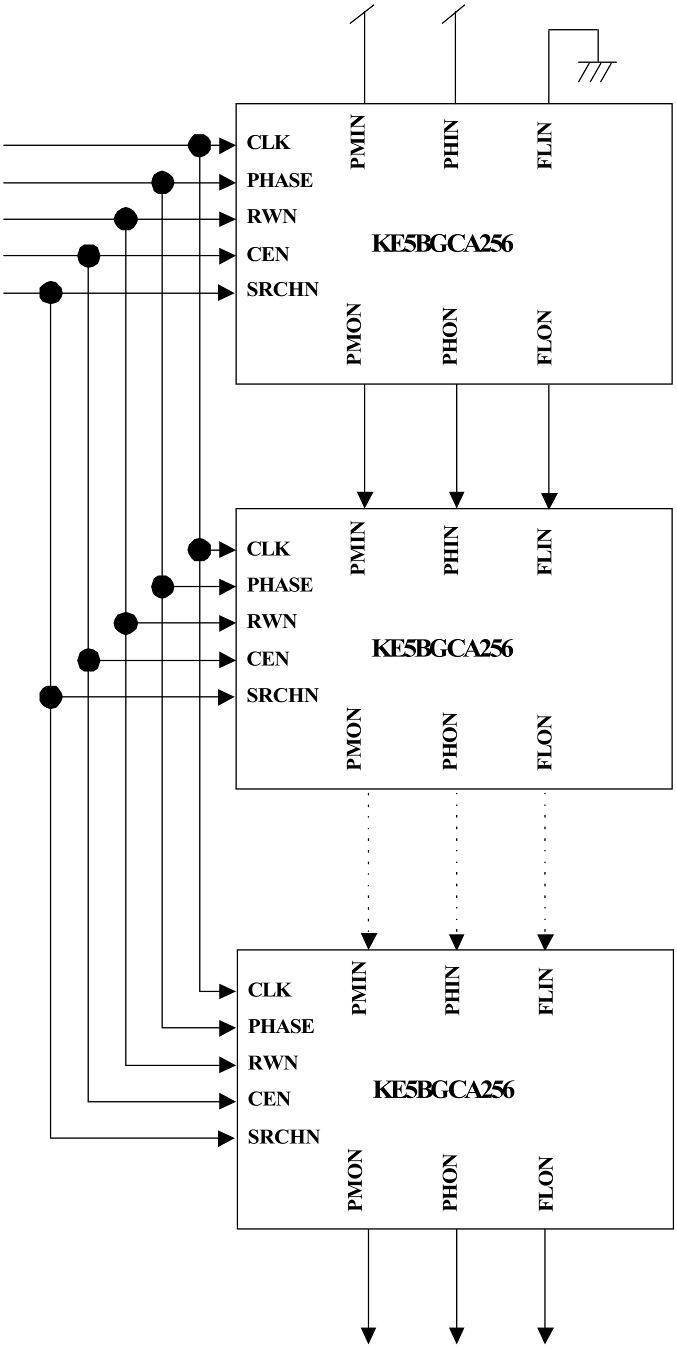


Fig. 5.3.3.1 Simple cascade connection

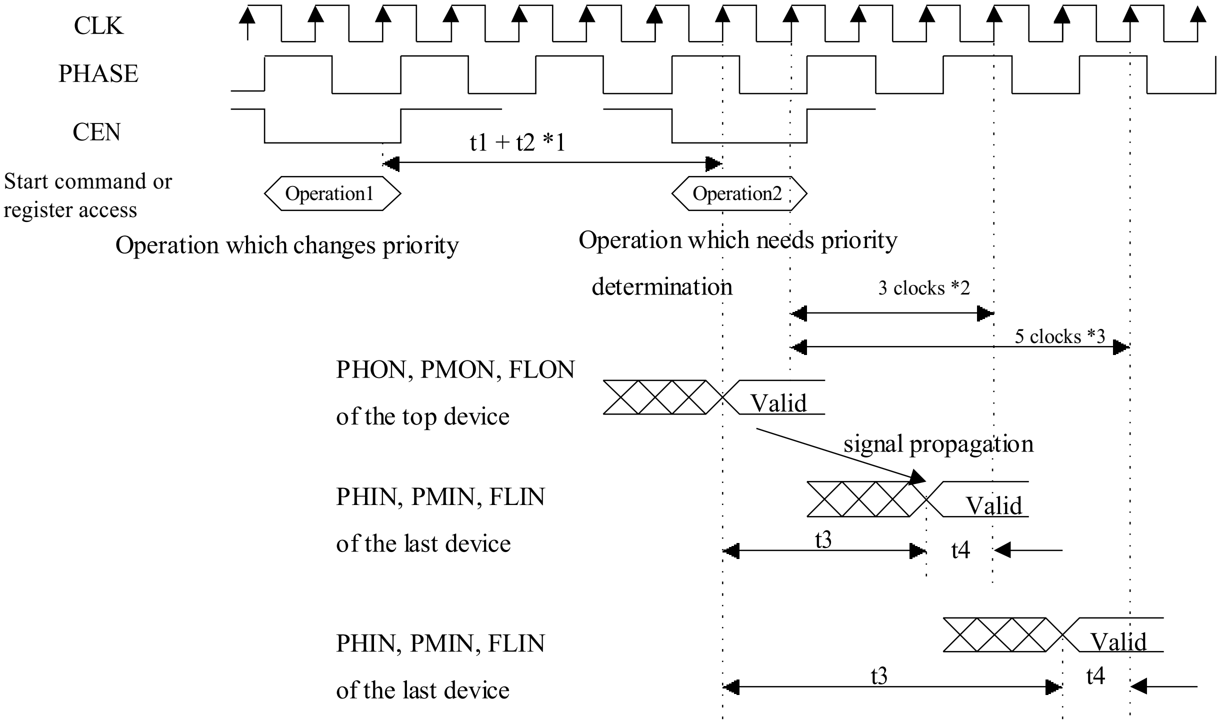

CLK
PHASE
CEN
t1 + t2 *1
Start command or register access
Operation1
Operation2
Operation which changes priority
Operation which needs priority determination
3 clocks *2
5 clocks *3
PHON, PMON, FLON of the top device
Valid
signal propagation
PHIN, PMIN, FLIN of the last device
Valid
t3
t4
PHIN, PMIN, FLIN of the last device
Valid
t3
t4

Fig. 5.3.3.2 Priority decision timing in a cascaded system (Simple cascade connection)

*1 • When the operation which changes the priority falls under one of the cases shown below, t1 is Latency 1.5 (= 3 clock).

1) Search by the SRCHN pin
2) Search by the SRCH command
3) Execution of the MEMHEAAI(Read/Write), NXT_HEA, GEN_FL, or STR1_HEAAI/STR2_HEAAI command

• When the operation which changes the priority falls under reset by the SRST command, t1 is Latency 1 (= 2 clock).

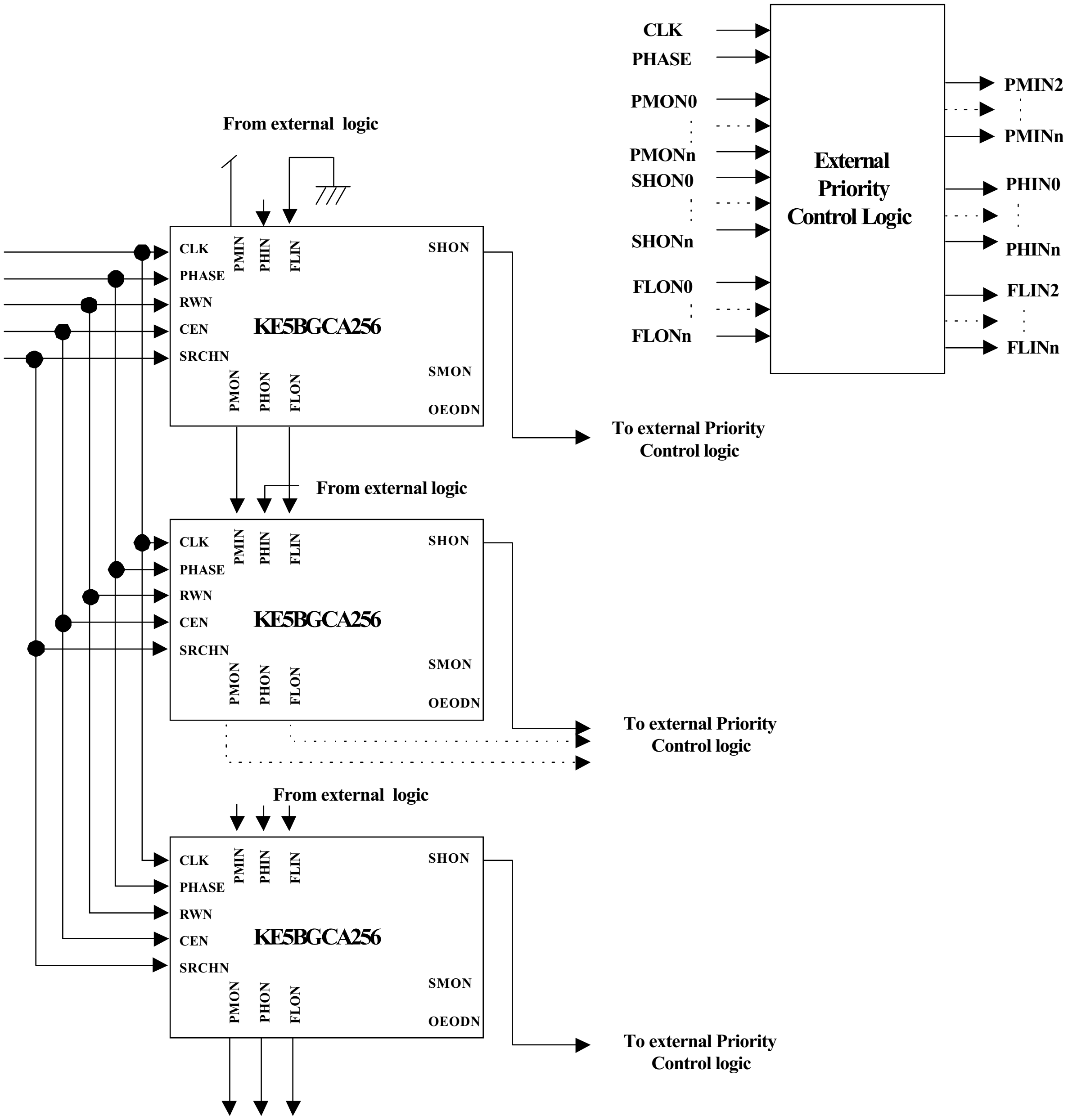
• When the operation which changes the priority falls under reset by the RSTN pulse, t1 is Latency 0 (= 0 clock).

t2 is the same in any case shown above.

*2 If the operation which needs priority determination falls under one of the cases shown below, the setup time is counted from 3 clock after input of the operation.

1) Execution of the MEMHHA(Read/Write), MEMHEA(Read/Write), MEMHEAAI(Read/Write), STR1_HHA/STR2_HHA, STR1_HEA/STR2_HEA, or STR1_HEAAI/STR2_HEAAI command

*3 If the operation which needs priority determination is HHA(Read) or HEA(Read), the setup time is counted from 5 clock after input of the operation.



*1 PHIN and PMON are used to propagate device priority and multi-hit flag.

Fig.5.3.3.3 Cascaded system with external priority control logic example

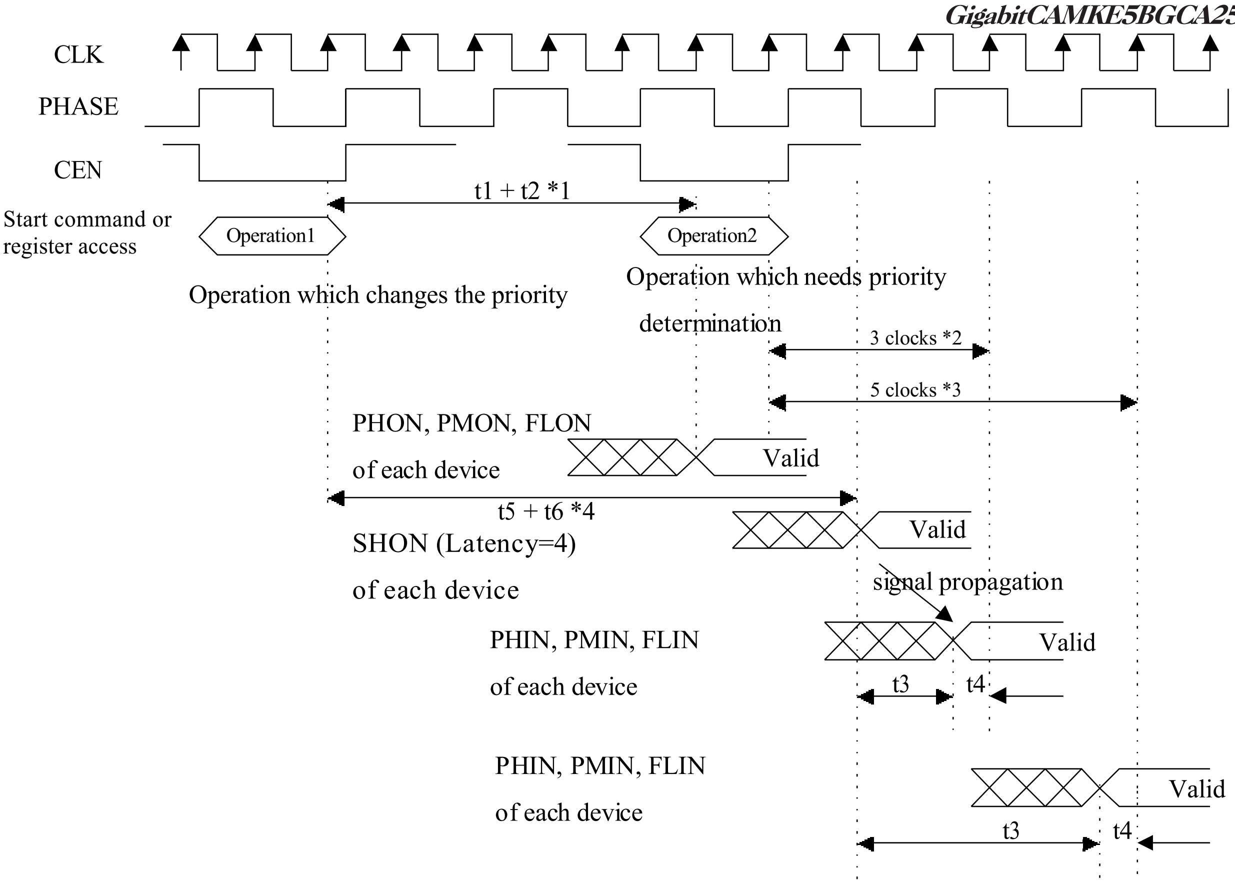

CLK
PHASE
CEN
Start command or register access
Operation1
Operation2
t1 + t2 *1
Operation which changes the priority
Operation which needs priority determination
3 clocks *2
5 clocks *3
PHON, PMON, FLON of each device
Valid
t5 + t6 *4
SHON (Latency=4) of each device
Valid
signal propagation
PHIN, PMIN, FLIN of each device
Valid
t3
t4
PHIN, PMIN, FLIN of each device
Valid
t3
t4

Fig.5.3.3.4 Priority decision timing in a cascaded system with external priority control logic

*1 • When the operation which changes the priority falls under one of the cases shown below, t1 is Latency 1.5 (= 3 clock).

1) Search by the SRCHN pin
2) Search by the SRCH command
3) Execution of the MEMHEAAI(Read/Write), NXT_HEA, GEN_FL, STR1_HEAAI/STR2_HEAAI, or STR1_AUTAI / STR2_AUTAIcommand

• When the operation which changes the priority falls under reset by the SRST command, t1 is Latency 1 (= 2 clock).

• When the operation which changes the priority falls under reset by the RSTN pulse, t1 is Latency 0 (= 0 clock).

t2 is the same in any case shown above.

*2 If the operation which needs priority determination falls under one of the cases shown below, the setup time is counted from 3 clock after input of the operation.

1) Execution of the MEMHHA(Read/Write), MEMHEA(Read/Write), MEMHEAAI(Read/Write), STR1_HHA/STR2_HHA, STR1_HEA/STR2_HEA, STR1_HEAAI/STR2_HEAAI, STR1_AUT/STR2_AUT, or STR1_AUTAI/STR2_AUTAI

*3 If the operation which needs priority determination is HHA(Read) or HEA(Read), the setup time is counted from 5 clock after input of the operation.

*4 In Fig. 5.3.3.4, the latency of the SHON of each device is 4. Therefore, t5 is latency 4 (= 8 clock) and t6 is delay time.

Operation1 Operation which changes the priority		Operation2 Operation which needs priority determination	
Single hit the priority propagation	Pins whose status changes	Command	Pins to consider
Search by the SRCHN pin command	PHON, PMON, SHON, SMON *1	MEMHHA(Read/Write)	PHIN
		MEMHHA_AT(Read/Write)	PHIN
Search by the SRCH command command	PHON, PMON, SHON, SMON *1	HHA(Read)	PHIN
		STR1_HHA command	PHIN
Reset by the SRST command command	PHON, PMON, SHON, SMON *1	STR2_HHA command	PHIN
		STR1_AUT command STR2_AUT command	PHIN, PFIN
Reset by the RSTN pulse	PHON, PMON, SHON, SMON *1	STR1_AUTAI command STR2_AUTAI command	PHIN, PFIN
Empty priority propagation	Pins whose status changes	Command	Pins to consider
MEMHEAAI(Read/Write) command	PFON command	MEMHEA(Read/Write)	FLIN
		MEMHEA_AT(Read/Write)	FLIN
NXT_HEA command GEN_FL command	FLON *2	MEMHAEAAI(Read/Write)	FLIN
		HEA(Read)	FLIN
STR1_HEAAI command STR2_HEAAI command	FLON *2	STR1_HEA command STR2_HEA command	FLIN
STR1_AUTAI command (in no hit) STR2_AUTAI command (in no hit)	FLON *2	STR1_HEAAI command STR2_HEAAI command	FLIN
Reset by the SRST command	FLON *2	STR1_AUT command STR2_AUT command	PHIN, FLIN
Reset by the RSTN pulse	FLON *2	STR1_AUTAI command STR2_AUTAI command	PHIN, FLIN

*1 Output variations of PHON, PMON, SHON, and SMON are shown below.

PHON Output	PHIN	PMIN	Status in the device
Low	0	Don't care	Single hit only
Low	0	Don't care	Multi-hit
Low	0	Don't care	Others
Low	1	Don't care	Single hit only
High	1	Don't care	Multi-hit
High	1	Don't care	Others

Table 5.3.3.2 Relations between the operation which changes the priority and the operation which needs priority determination

*1 Output Variations of PHON, PMON, SHON, and SMON (cont'd)

PMON Output	PHIN	PMIN	Status in the device
Low	0	0	Single hit only
Low	0	0	Multi-hit
Low	0	0	Others
Low	0	1	Single hit only
Low	0	1	Multi-hit
High	0	1	Others
Low	1	0	Single hit only
Low	1	0	Multi-hit
Low	1	0	Others
High	1	1	Single hit only
Low	1	1	Multi-hit
High	1	1	Others

SHON Output	PHIN	Status in the device
Low	Don't care	Single hit only
High	Don't care	Others

SMON Output	PHIN	Status in the device
Low	Don't care	Multi-hit
High	Don't care	Others

*2 Output Variations of FLON

FLON Output	FLIN	Status in the device
High	0	Empty entry in the device
Low	0	No empty entry in the device
High	1	Empty entry in the device
High	1	No empty entry in the device

Table 5.3.3.2 Relations between the operation which changes the priority and the operation which needs priority determination (cont'd)

STR_AUT Command in a Cascaded System

The STR_AUT command executes the STR_HHA action when there is a hit in the device and the STR_HEA action when there is no hit in the device as mentioned before. After the search operation, each device is going to execute either the STR_HHA or the STR_HEA action referring to its own search result. Therefore, in a cascaded system, the PHIN must be controlled by determining the priority with hit information in the system before the STR_AUT command is executed in devices. (See Fig. 5.3.3.4) The PHIN of each device should be created from the SHON signal of the each device by the external logic.

Operation in Hit (same as STR_HHA)
When there is a hit in the device, the data in the CMP register is going to be written in the entry indicated by the HHA register. Unless there is a multi-hit in the device, the STR1_AUT uses the HHA1 which is a search result of the CMP1, and the STR2_AUT uses the HHA2 which is a search result of the CMP2. This operation is not performed when there is not single hit priority (PHIN = "0").

Operation in No Hit
This operation is a little bit different from the normal operation of the STR_HEA command. The STR_HEA command takes only the empty priority into account in a cascaded system. The STR_HEA command is going to be executed in the device where there are no hits even though there is a hit in other devices, because the hit information in the device alone is taken into account in the STR_HEA operation by the STR_AUT command. Therefore, when there is a hit in some other devices, the STR_HEA operation must be restrained in the device where there are no hits according to the timing shown in Fig. 5.3.3.4. The PHIN signal is as the control signal to perform this function in the device. Only when the PHIN is “1,” is the STR_HEA operation performed in the no hit case of the STR_AUT command. Therefore, when the STR_AUT command is used in a cascaded system, the PHIN signal must be controlled by external logic, while taking this into account. When there are no hits in all devices in the system, the STR_HEA operation is performed in the device that has the highest empty priority. Table 5.3.3.2 shows the operation that changes the priority and the operation that needs priority determination.

5.3.4 Output Port in a Cascaded System

Table 5.3.4.1 shows the output conditions of the Output Port and Fig. 5.3.4.1 (a/b) shows the timing. If there is no multi-hit in the system, if there are many devices with a single hit, and if the HEA output is not required, the output control is performed in each device and can be realized without any external logic by connecting the Output Ports of the respective devices. In this case, HHA/HEA latency = 4 can be selected. When there is multi-hit in the device, invalid HHA is output in the OD port as same as HHA/HEA latency = 5, 6, 7. However, in case of HHA/HEA latency = 4, Invalid flag (OD<15>) does not indicates whether outputting HHA is valid or not. The SMON signal (latency =5) indicates whether the output HHA is valid or not. (See Fig. 5.3.4.2 (a))

If there is a multi-hit in the system or the HEA output is required, collisions on the Output Port happen. In this case, the OEODN control from the SHON signal by the external logic is necessary. (See Fig. 5.3.4.2 (b))

Timing in a Cascaded System

Fig. 5.3.4.3 shows the timing by the external control logic in a cascaded system. The OEODN signal must be controlled by the external logic. The latency of OEODN is 1.
t1: latency of SHON (Latency is 4 in Fig. 5.3.4.3)
t2: delay time of the SHON signal
t3: latency of FLON (Latency is 1.5 = 3 clock.)
t4: delay time of the FLON signal
t5: output latency of the OD port (HHA latency is 5 in Fig. 5.3.4.1(a/b))
t6: delay time of the OD port signal
t7: setup time of the OEODN signal
t8: delay time of the signal from the external control logic

OPSL: OD<20:0> output is selected by OPSL input.

Hit/Mis-hit: It indicates whether the search result is hit or not.

MHN: It indicates whether the search result is multi-hit or not.

HEA output: The SCONF register indicates whether HEA output is necessary or not when there are no hits. (0: no output, 1: output)

FLON: It indicates whether CAM table is full or not.

	OPSL *1	Hit /Mis-hit	MHN	HEAoutput	FLON	OD output
HHA state	1	0	0	x	x	HHA(invalid)(*2)
	1	0	1	x	x	HHA(*3)
	1	1	1	0	x	Hi-Z
	1	1	1	1	0	HEA(invalid)(*4)
	1	1	1	1	1	HEA(*5)
MEMHHA state	0	0	0	x	x	Invalid
	0	0	1	x	x	MEMHHA
	0	1	1	0	x	Hi-Z
	0	1	1	1	0	Hi-Z
	0	1	1	1	1	Hi-Z

Bit15 of the OD port (OD<15>) is Valid flag which indicates status of the outputting HHA/HEA.

0:Valid, 1:Invalid

Bit14 of the OD port (OD<14>) is HHA/HEA flag which indicates whether output of the OD port is HHA or HEA.

0:HHA output 1:HEA output

(*1) Even if OPSL is set to "1" after the MEMHHA output is determined (if latency is 6, after then), HHA or HEA is output in the right way. If OPSL is set to "0" before the MEMHHA output is determined (if the latency is 6,before then), the MEMHHA searched before is output. Refer to Fig. 5.3.4.2.

(*2) OD<20:16>: DEVID is output.
OD<15> :1 (invalid)
(in case of HHA/HEA latency = 5, 6, 7)
OD<15> :x (unknown) (in case of HHA/HEA latency = 4)
OD<14> :0 (HHA)
OD<13:12>: unknown
OD<11:0> : HHA

(*3) OD<20:16>: DEVID is output.
OD<15> :0 (valid)
(in case of HHA/HEA latency = 5, 6, 7)
OD<15> :x (unknown) (in case of HHA/HEA latency = 4)
OD<14> :0 (HHA)
OD<13:12>: unknown
OD<11:0> : HHA

(*4) OD<20:16>: DEVID is output.
OD<15> :1 (invalid)
(in case of HHA/HEA latency = 5, 6, 7)
OD<15> :x (unknown) (in case of HHA/HEA latency = 4)
OD<14> :1 (HEA)
OD<13:12>: unknown
OD<11:0> : HEA

(*5) OD<20:16>: DEVID is output.
OD<15> :0 (valid)
(in case of HHA/HEA latency = 5, 6, 7)
OD<15> :x (unknown) (in case of HHA/HEA latency = 4)
OD<14> :1 (HEA)
OD<13:12>: unknown
OD<11:0> : HEA

Table 5.3.4.1 Output conditions of the Output Port

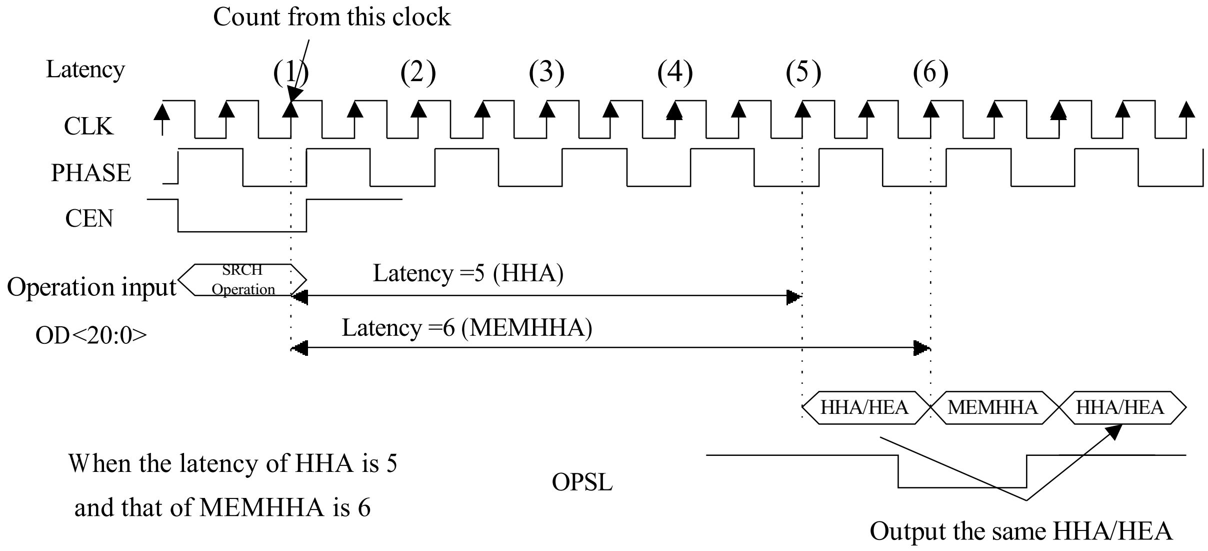


Fig. 5.3.4.1(a) Timing of the Output Condition

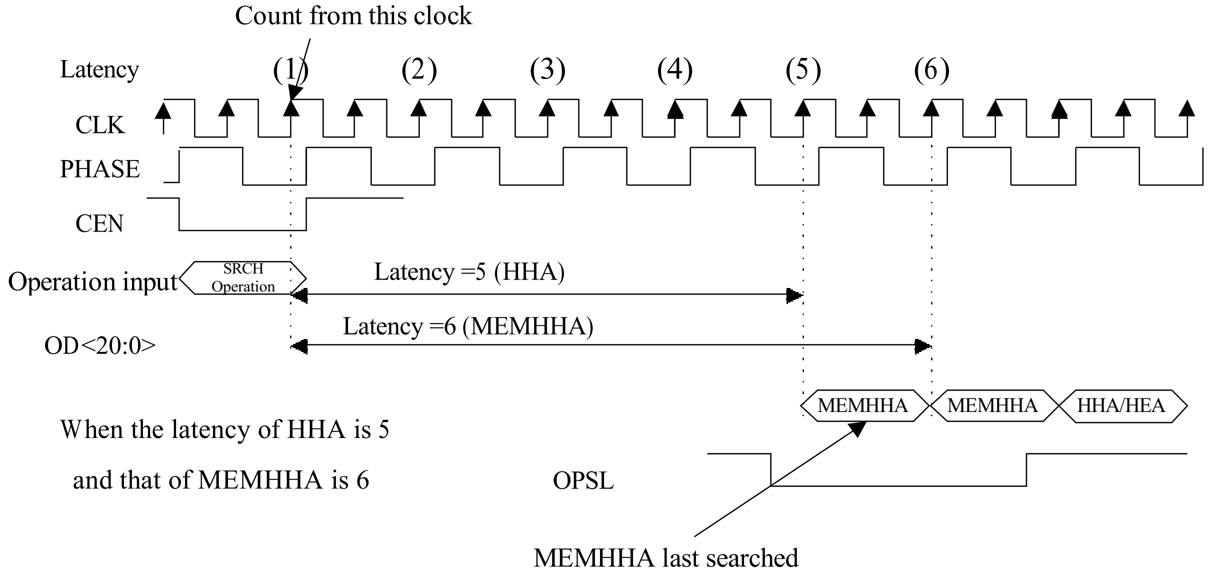


Fig. 5.3.4.1(b) Timing of the Output Condition

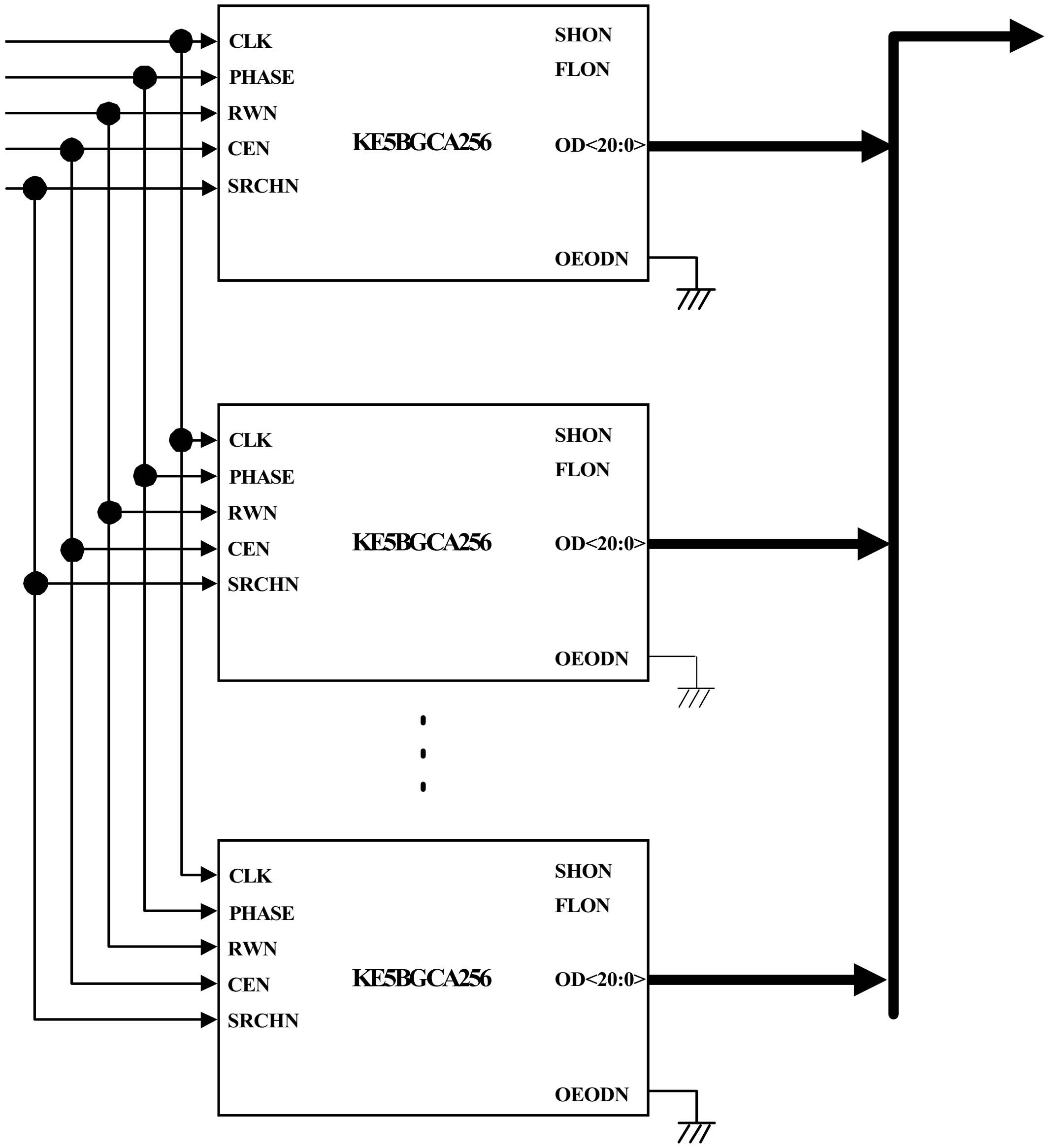


Fig.5.3.4.2 (a) simple cascade connection example

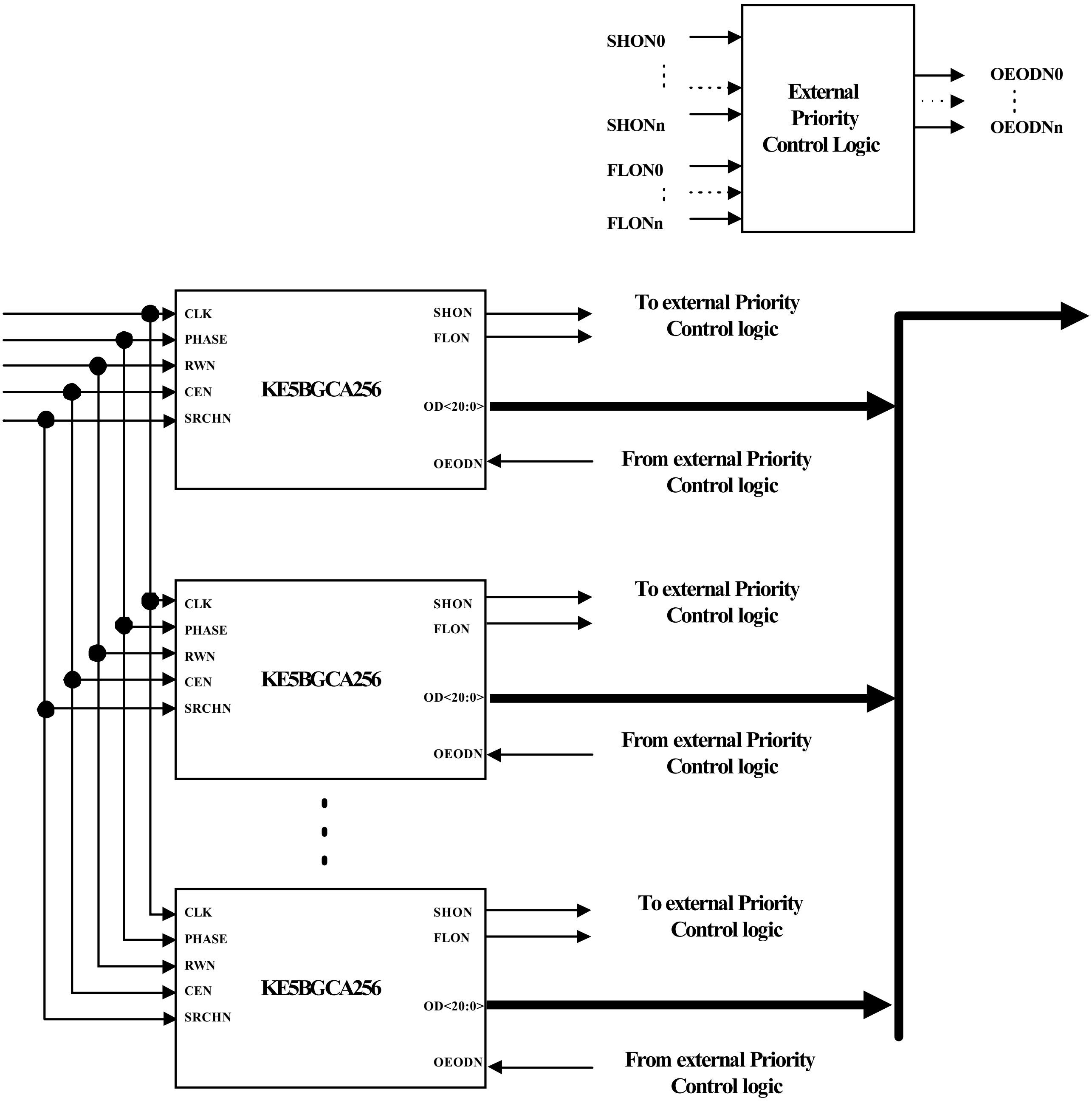

SHON0
SHONn
FLON0
FLONn
External Priority Control Logic
OEODN0
OEODNn
CLK
PHASE
RWN
CEN
SRCHN
KE5BGCA256
SHON
FLON
OD<20:0>
OEODN
To external Priority Control logic
From external Priority Control logic

Fig.5.3.4.2 (b) cascade connection example (signals of the Output Port)

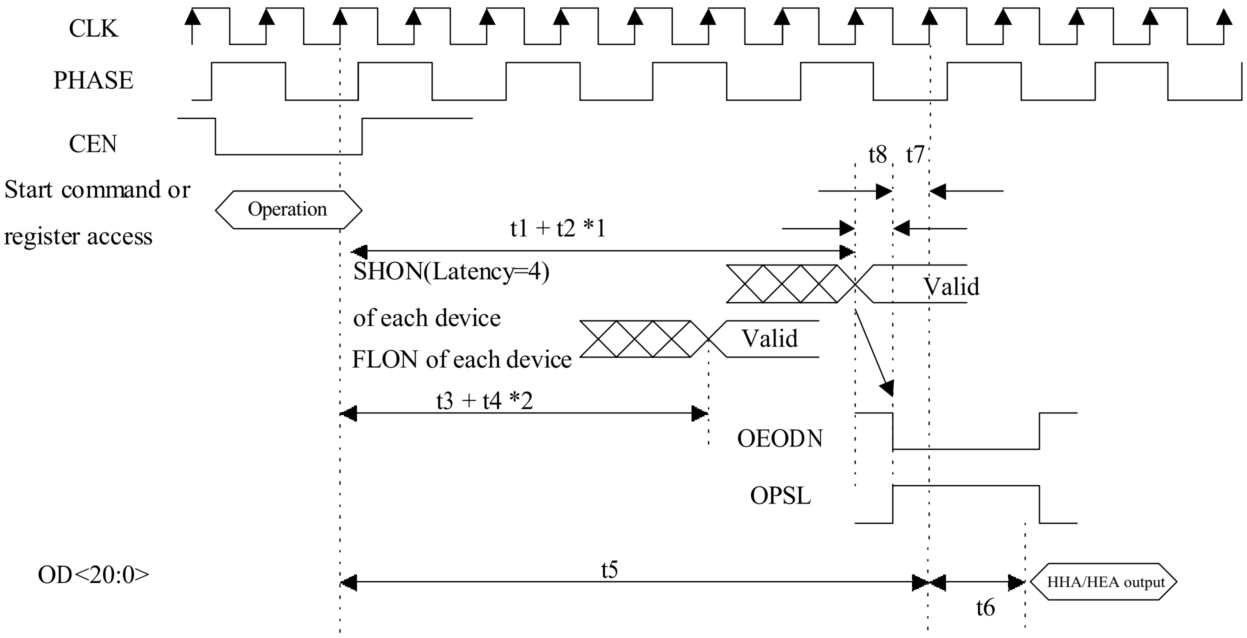


Fig. 5.3.4.3 Timing design in a cascaded system

6. CommandDescriptions

6.1 Command Functions

All commands are executed by writing the 16-bit OP-code into the COML register. Table 6.1 shows the command names, operation codes, functions and descriptions.

Command Group	Command name (OP-code)	Cycle No.	Function	Description
Reset	SRST (0000H)	2	Software Reset	Executes Device reset. The function of this command is the same as a low pulse input to the RSTN pin. All entries (including entries whose Permanent Bit is set) become empty (inactive) by this command. The flag pins are set as follows: PHON = High, PMON = High, FLON = High SHON = High, SMON = High
Configuratior	STR_DEVID (2000H)	1	DEVID mode start	Switches the device to the DEVID mode in order to define the Device ID.
	END_DEVID (2800H)	1	DEVID mode end	Ends the DEVID mode.
	NXT_PR (3000H)	1	Shift DEVID Priority	Shifts the DEVID priority to the next device in the DEVID mode.
CAM Table	SRCH1 *1 (4000H)	1	Search	Searches with data in the CMP1 register.
	SRCH2 *1 (4200H)	1	Search	Searches with data in the CMP2 register.
	PRG_AL *2 (6000H)	1	Purge	All entries become empty (inactive) by this command. However, an entry whose Permanent Bit is set to "1" does not become empty by this command.
	PRG_AC *2 (6040H)	1	Purge	All entries whose Access Bit is set to "1" become empty (inactive) by this command. However, an entry whose Permanent Bit is set to "1" does not become empty by this command.
	PRG_NAC *2 (6080H)	1	Purge	All entries whose Access Bit is not set to "1" become empty (inactive) by this command. However, an entry whose Permanent Bit is set to "1" does not become empty by this command.

Table 6.1 Command table

Command Group	Command name (OP-code)	Cycle No.	Function	Description
CAM Table	RST_AC (A000H)	1	Reset all Access Bits	Clears Access Bits of all entries.
	RST_PM (A010H)	1	Reset all Permanent Bits	Clears Permanent Bits of all entries.
	GEN_FL (8004H)	2	Confirm the HEA register	Confirms the empty state of the CAM table. Makes the HEA register store the entry address with the highest empty priority. The content of the HEA register and the status of the FLON pin are also changed.
	NXT_HE (8008H)	2	Renew the HEA register	Makes the HEA register store an entry address with the next empty priority. The content of the HEA register and the status of the FLON pin are also changed.
Move	STR1_AR *1 (C000H)	1	Store	Moves data in the CMP1 register into the entry indicated by the AR register.
	STR1_HHA *1 (C001H)	1	Store	Moves data in the CMP1 register into the entry indicated by the HHA register according to the search result of the CMP1 register write or the SRCH1 command.
	STR1_HEA *1 (C002H)	1	Store	Moves data in the CMP1 register into the entry indicated by the HEA register.
	STR1_HEAAI*1 (C00AH)	2	Store	Moves data in the CMP1 register into the entry indicated by the HEA register. Renews the HEA register simultaneously.
	STR1_AUT*1 (C003H)	1	Store	Moves data in the CMP1 register into the entry indicated by the HHA register according to the CMP1 register write or the SRCH1 command if the search result is a hit. Moves data in the CMP1 register into the entry indicated by the HEA register if the search result is no hit.
	STR1_AUTAI*1 (C00BH)	2	Store	Moves data in the CMP1 register into the entry indicated by the HHA register according to the CMP1 register write or the SRCH1 command if the search result is a hit. Moves data in the CMP1 register into the entry indicated by the HEA register if the search result is no hit. Renews the HEA register simultaneously.

Table 6.1 Command table (cont'd)

Command Group	**Command name (OP-code)**	**Cycle No.**	**Function**	**Description**
	STR2_AR *1 (C200H)	1	Store	Moves data in the CMP2 register into the entry indicated by the AR register.
	STR2_HHA *1 (C201H)	1	Store	Moves data in the CMP2 register into the entry indicated by the HHA register according to the search result of the CMP2 register write or the SRCH2 command.
Move	STR2_HEA *1 (C202H)	1	Store	Moves data in the CMP2 register into the entry indicated by the HEA register.
	STR2_HEAAI*1 (C20AH)	2	Store	Moves data in the CMP2 register into the entry indicated by the HEA register. Renews the HEA register simultaneously.
	STR2_AUT*1 (C203H)	1	Store	Moves data in the CMP2 register into the entry indicated by the HHA register according to the CMP2 register write or the SRCH2 command if the search result is a hit. Moves data in the CMP2 register into the entry indicated by the HEA register if the search result is no hit.
	STR2_AUTAI*1 (C20BH)	2	Store	Moves data in the CMP2 register into the entry indicated by the HHA register according to the CMP2 register write or the SRCH2 command if the search result is a hit. Moves data in the CMP2 register into the entry indicated by the HEA register if the search result is no hit. Renews the HEA register simultaneously.
Other	NOP (E000H)	1	No operation	Executes no operation.

Table 6.1 Command table (cont'd)

*1 Mask operation by each bit can be executed by the MASK registers (MASK0 ~ MASK11). These MASK registers can be selected by the MS<3:0> pins or the CNTL1 register.

*2 After the Purge (PRG_*) command is executed, the status of the Access Bit of each word is kept. Execute the RST_AC command in order to clear all Access Bits.

6.2 Command Format

The OP-code field :OP<15:0> is made up of the following fields.

OPE(3bits):OP<15:13>
This field defines the type of operation assigned as below.
0H : Reset operation
1H : Device configuration
2H : Search operation
3H : Purge operation
4H : Empty priority operation
5H : Attribute bit operation
6H : Store operation
7H : undefined (no operation)

CONF(2bits):OP<12:11>
This field defines the type of command in device configuration.
0H:STR_DEVID command
1H:END_DEVID command
2H:NXT_PR command
3H : undefined

CMP(2bits):OP<10:9>
This field defines the selection of the Comparand registers.
0H : CMP1 selects
2H : CMP2 selects
3H : undefined
4H : undefined

PRG(3bits):OP<8:6>
This field defines the type of purge.
0H:PRG_AL command
1H:PRG_AC command
2H:PRG_NAC command
3H : undefined
4H : undefined
5H : undefined
6H : undefined
7H : undefined

RST(2bits):OP<5:4>
This field defines the Attribute bit to be reset.
0H : Access Bit
1H : Permanent Bit
2H : undefined
3H : undefined

GEN(2bits):OP<3:2>
This field defines the HEA operation method.
0H : no operation
1H : GEN_FL operation (determines HEA)
2H : NXT_HE operation (renews HEA)
3H : undefined

AR/HHA/HEA(2bits):OP<1:0>
This field defines the destination address of the Store command.
0H : AR
1H : HHA
2H : HEA
3H : STR_AUT command

	Ope (3bits)	Config mode	CMP sel	PRG mode	RST mode	GEN	AR /HHA /HEA	Device select method		Op-code (16 bits) MSB LSB
Group	3bits	2bits	2bits	3bits	2bits	2bits	2bits	Broadcast	Devsel	
SRST	0	X	X	X	X	X	X	○	△ *1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
STR_DEVID	1	0	X	X	X	X	X	○	△ *1	0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
END_DEVID	1	1	X	X	X	X	X	○	△ *1	0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0
NXT_PR	1	2	X	X	X	X	X	○	△ *1	0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0
SRCH1	2	X	0	X	X	X	X	○	○	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SRCH2	2	X	1	X	X	X	X	○	○	0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0
PRG_AL	3	X	X	0	X	X	X	○	○	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
PRG_AC	3	X	X	1	X	X	X	○	○	0 1 1 0 0 0 0 0 0 1 0 0 0 0 0 0
PRG_NAC	3	X	X	2	X	X	X	○	○	0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0
GEN_FL	4	X	X	X	X	1	X	○	○	1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
NXT_HE	4	X	X	X	X	2	X	○ *2	○ *3	1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0
RST_AC	5	X	X	X	0	X	X	○	○	1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
RST_PM	5	X	X	X	1	X	X	○	○	1 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0
STR1_AR	6	X	0	X	X	X	0	○ *4	○	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
STR1_HHA	6	X	0	X	X	X	1	○ *5	○ *6	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1
STR1_HEA	6	X	0	X	X	0	2	○ *2	○ *3	1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0
STR1_HEAAI	6	X	0	X	X	2	2	○ *2	○ *3	1 1 0 0 0 0 0 0 0 0 0 0 1 0 1 0
STR1_AUT *7	6	X	0	X	X	0	3	○ *2	○ *3	1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1
STR1_AUTAI *7	6	X	0	X	X	2	3	○ *2	○ *3	1 1 0 0 0 0 0 0 0 0 0 0 1 0 1 1
STR2_AR	6	X	1	X	X	X	0	○ *4	○	1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0
STR2_HHA	6	X	1	X	X	X	1	○ *5	○ *6	1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 1
STR2_HEA	6	X	1	X	X	0	2	○ *2	○ *3	1 1 0 0 0 0 1 0 0 0 0 0 0 0 1 0
STR2_HEAAI	6	X	1	X	X	2	2	○ *2	○ *3	1 1 0 0 0 0 1 0 0 0 0 0 1 0 1 0
STR2_AUT *7	6	X	1	X	X	0	3	○ *2	○ *3	1 1 0 0 0 0 1 0 0 0 0 0 0 0 1 1
STR2_AUTAI *7	6	X	1	X	X	2	3	○ *2	○ *3	1 1 0 0 0 0 1 0 0 0 0 0 1 0 1 1
NOP	7	X	X	X	X	X	X	○	△ *1	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

Table 6.2 Command Format and Conditions for Execution

Notes; ○: Executable

△ : Executable (device not selectable. See annotations)

X : Don't care

*1 The command is executable for all devices (a device cannot be selected).

*2 Only the device with empty priority accepts the command.

*3 The command is not executed when the selected device does not have an empty entry.

*4 The command is executable for all devices (but not usually used).

*5 Only the device with a single hit priority accepts the command.

*6 Only the selected device with a single hit accepts the command. The command is not executed when there is a multi-hit or no hit in the device.

*7 When the search result is a hit, the Mask register which is used in the write to the address indicated by HHA is determined by STR1_HHA/STR2_HHA in the CNTL register. When the search result is no hit, the Mask register which is used in the write to the address indicated by HEA is determined by STR1_HEA/STR2_HEA in the CNTL register although the Mask register is selected by the external pin (GCMS of the CNTL1 register is “1”).

Table 6.2 Command Format and Conditions for Execution (cont'd)

7. Register Descriptions

7.1 Overview

Most of the registers of this device are 64 bits in width. The 32 bits on the MSB side are assigned to the High side, and the 32 bits on the LSB side are assigned to the Low side. Registers are classified into six functional groups (Command Register Group, Control Status Register Group, Memory R/W Register Group, Configuration Register Group, Comparand Register Group, and Table Status Register Group). An overview of each register group is presented below.

(1) Command Register Group

This group has only one register, the COM register, which is used to execute commands by writing the OP-code (Refer to Chapter 6).

(2) Control Register Group

This group has three registers, the CNTL1, the CNTL2, and the DEVID registers. The CNTL1 register specifies the definition of the Mask register selection, the operation of the Access and Permanent Bit, the endian, and the Input mode. The CNTL2 register specifies the output latency of the Output Port. The DEVID register is used to store the Device ID in a cascaded system.

(3) Memory R/W Register Group

This group has ten registers: the DEVSEL, the AR, the MEMAR, the MEMARAI, the MEMAR_AT, the MEMHHA, the MEMHHA_AT, the MEMHEA, the MEMHEAAI, and the MEMHEA_AT registers. The DEVSEL register is used to select the device in a cascaded system. The AR register is used to specify the absolute address used for the read/write operation of the MEMAR register. The MEMAR register is used to read/write the contents of the CAM table indicated by the AR register. The MEMARAI register is used for automatic increment operation of one AR register after it is accessed. The MEMAR_AT register is used to read/write the attribute data stored in the address indicated by the AR register. The MEMHHA register is used to read/write the data stored in the address indicated by the HHA register. The MEMHHA_AT register is used to read/write the attribute data stored in the address indicated by the HHA register. The MEMHEA register is used to read/write the data stored in the address indicated by the HEA register. The MEMHEAAI register is used to automatically renew the HEA register after it is accessed. The MEMHEA_AT register is used to read/write the attribute data stored in the address indicated by the HEA register.

(4) Configuration Register Group

This group has two types of registers, the MASK registers and the SCONF register. The MASK registers set the mask pattern with a unit of one bit in the search operation or the write operation to the CAM data. The SCONF register defines the search configuration.

(5) Comparand Register Group

This group has two registers, the CMP1 and the CMP2 registers, each 64-bit wide. These registers are used for the search operation or the write operation, where the contents of these registers are written in the entry.

(6) Table Status Register Group

This group has two registers, the HHA and the HEA registers. The HHA register is used to store the hit address with the highest priority. The HEA is used to store the empty address with the highest priority.

7.2 Register Addresses

Table 7.2.1 shows the Register Addresses.

Group	Register name	Address
(1)Command	COML	00H
	—	01H
(2)Control status	CNTL1L	02H
	CNTL1H	03H
	CNTL2L	04H
	—	05H
	DEVIDL	06H
	DEVIDH	07H
(3)Memory R/W	DEVSELL	08H
	—	09H
	ARL	0AH
	—	0BH
	MEMARL	0CH
	MEMARH	0DH
	MEMARAIL	0EH
	MEMARAIH	0FH
	MEMAR_ATL	10H
	—	11H
	MEMHHAL	12H
	MEMHHAH	13H
	MEMHHA_ATL	14H
	—	15H
	MEMHEAL	16H
	MEMHEAH	17H
	MEMHEAAIL	18H
	MEMHEAAIH	19H
	MEMHEA_ATL	1AH
	—	1BH
(4)Configuration	MASK0L	1CH
	MASK0H	1DH
	MASK1L	1EH
	MASK1H	1FH
(4)Configuration	MASK2L	20H
	MASK2H	21H
	MASK3L	22H
	MASK3H	23H
	MASK4L	24H
	MASK4H	25H
	MASK5L	26H
	MASK5H	27H
	MASK6L	28H
	MASK6H	29H
	MASK7L	2AH
	MASK7H	2BH
	MASK8L	2CH
	MASK8H	2DH
	MASK9L	2EH
	MASK9H	2FH
	MASK10L	30H
	MASK10H	31H
	MASK11L	32H
	MASK11H	33H
	SCONFL	36H
	SCONFH	37H
(5)Comparand	CMP1L	38H
	CMP1H	39H
	CMP2L	3AH
	CMP2H	3BH
(6)Table status	HHAL	3CH
	—	3DH
	HEAL	3EH
	—	3FH

Table 7.2.1 Register Address

7.3 Register Bit Maps

(1) Command Register Group

COM (Command) Register

COML: ADD<5:0>=00H

Each command is executed by writing the OP-code in the 16 bits of the LSB side of this register. See Chapter 6 for details of command op-code/function/execution condition. This register is only allowed to write.

COML Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0

Bits	Name	Function	After RSTN(SRST)
15-0	OP<15:0>	OP-code(16-bit)	Unknown

(2) Control Status Register Group

CNTL1 (Control1) Register

CNTL1L : ADD<5:0>=02H, CNTL1H: ADD<5:0>=03H

This 64-bit register specifies the definition of the MASK registers, the value of the Permanent and Access bits in the write operation by the MEMAR or the MEMHEA registers, the Input mode, and the endian control of the automatic increment function.

CNTL1H Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
		HEPM	HEAC	ARPM	ARAC	GDMS	DHE3	DHE2	DHE1	DHE0	DHH3	DHH2	DHH1	DHH0	DAR3
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DAR2	DAR1	DAR0	GCMS	CHE23	CHE22	CHE21	CHE20	CHH23	CHH22	CHH21	CHH20	CAR23	CAR22	CAR21	CAR20

CNTL1L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHE13	CHE12	CHE11	CHE10	CHH13	CHH12	CHH11	CHH10	CAR13	CAR12	CAR11	CAR10	GBMS	GB23	GB22	GB21
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GB20	GB13	GB12	GB11	GB10	GAMS	GA23	GA22	GA21	GA20	GA13	GA12	GA11	GA10	AISL	DSL

Bits	Name	Function	After RSTN(SRST)
61	HEPM	Sets the Permanent Bit when writing MEMHEA or MEMHEAAI, executing STR1_HEA or STR2_HEA, or executing STR1_AUT or STR2_AUT after the last search result is no hit.	0
60	HEAC	Sets the Access Bit when writing MEMHEA or MEMHEAAI, executing STR1_HEA or STR2_HEA, or executing STR1_AUT or STR2_AUT after the last search result is no hit.	0
59	ARPM	Sets the Permanent Bit when writing MEMAR or MEMARAI, or executing STR1_AR or STR2_AR.	0
58	ARAC	Sets the Access Bit when writing MEMAR or MEMARAI, or executing STR1_AR or STR2_AR.	0
57	GDMS 0 1	Selection method of the MASK registers in group D Group D is designated by the external pin, MS<3:0> Group D is designated by the control register.	0
56-53	DHE<3:0>	Designates the MASK register when writing table by MEMHEA or MEMHEAAI.	0000
52-49	DHH<3:0>	Designates the MASK register when writing table by MEMHHA.	0000
48-45	DAR<3:0>	Designates the MASK register when writing table by MEMAR or MEMARAI.	0000

Bits	Name	Function	After RSTN(SRST)
44	GCMS 0 1	Selection method of the MASK registers in group C Group C is designated by the external pin, MS<3:0> Group C is designated by the control register. However, the MASK register is designated according to CHE1<3:0> or CHE2<3:0> when executing STR1_AUT or STR2_AUT after the last search result is no hit.	0
43-40	CHE2<3:0>	Designates the MASK register when writing a table by STR2_HEA, or designates the MASK register when executing STR2_AUT after the last search result is no hit.	0000
39-36	CHH2<3:0>	Designates the MASK register when writing a table by STR2_HHA, or designates the MASK register when executing STR2_AUT after the last search result is a hit.	0000
35-32	CAR2<3:0>	Designates the MASK register when writing a table by STR2_AR.	0000
31-28	CHE1<3:0>	Designates the MASK register when writing a table by STR1_HEA, or designates the MASK register when executing STR1_AUT after the last search result is no hit.	0000
27-24	CHH1<3:0>	Designates the MASK register when writing a table by STR1_HHA, or designates the MASK register when executing STR1_AUT after the last search result is a hit.	0000
23-20	CAR1<3:0>	Designates the MASK register when writing a table by STR1_AR.	0000
19	GBMS 0 1	Selection method of the MASK registers in group B Group B is designated by the external pin, MS<3:0>. Group B is designated by the control register.	0
18-15	GB2<3:0>	Designates the MASK register when searching by the SRCH2 command.	0000
14-11	GB1<3:0>	Designates the MASK register when searching by the SRCH1 command	0000
10	GAMS 0 1	Selection method of the MASK registers in group A Group A is designated by the external pin, MS<3:0>. Group A is designated by the control register.	0
9-6	GA2<3:0>	Designates the MASK register when searching by CMP2 and the SRCHN pin.	0000
5-2	GA1<3:0>	Designates the MASK register when searching by CMP1 and the SRCHN pin.	0000

Bits	Name	Function	After RSTN(SRST)
1	AISL	Sets the address increment condition in writing the MEMARAI or MEMHEAAI registers when DAT<31:0> input is 32-bit mode, or in reading the MEMARAI or MEMHEAAI registers.	0
	0	Access to the Low side	
	1	Access to the High side	
0	DSL	Register Access Method	0
	0	The data is stored in the buffer of the device when the PHASE signal is "0" and then is written in the registers with a unit of 32 bits. (When 32 bits on the high/low side of MEMAR, MEMARAI, MEMHHA, MEMHEA, or MEMHEAAI is written, the other 32 bits on the low/high side is masked. (The Access, Permanent, or Empty Bits are set by the write operation of only the half side, 32 bits.)	
	1	The registers in the device are written with a unit of 64 bits. (When the PHASE signal is "1," 32 bits on the high side is stored in the buffer. When the PHASE signal changes to "0," 32 bits on the low side is stored in the buffer. Then, the high side and the low side are combined to 64 bits and written in the registers.) (The least bit of ADD<5:0> is ignored (don't care) and the data is written with a unit of 64 bits.)	

CNTL2 (Control2) Register
CNTL2L : ADD<5:0>=04H

This register specifies the latency of HHA, MEMHHA, and SHON. It is prohibited to modify-write the CNTL2 register right after the search operation. Four NOP commands or an 8 clock wait must be inserted after the search operation.

CNTL2L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												MEML	HOL	OUTL1	OUTL0

Bits	Name	Function	After RSTN(SRST)

3	MEML
	0
	1
		Output Port: Defines the latency of MEMHHA output
		Latency = 6
		Latency = 7
			0

2	HOL
	0
	1
		SHON latency: Defines the latency of SHON
		Latency = 4
		Latency = 5
			0

1-0	OUTL<1:0>
	00
	01
	10
	11
		Output Port: Defines the latency of HHA/HEA output.
		Latency=5
		Latency=6
		Latency=7
		Latency=4 (*1)
			00

(*1) When HHA/HEA Latency = 4, Invalid flag (Bit15 of OD port) is unknown. Therefore, this flag can not be used to confirm whether the output HHA is invalid (multi-hit result) or not. The SMON signal (latency =5) indicates whether the search result is multi-hit or not.

DEVID Register
DEVIDL : ADD<5:0>=06H, DEVIDH : ADD<5:0>=07H

This register stores the number of each device (Device ID) for the operation of a cascaded system. It is necessary to access this register and to set the unique Device ID for each device in a cascaded system after each Device Reset operation. The LD bit of the last device must be set to “1,” and that of other devices must be set to “0.” The LD is set to “1” when a low pulse is given to the RSTN pin, or the SRST command is issued. It is not necessary to write the LD bit in a single device system, but the LD bit must be set to “1” if the Device ID is written. This register is allowed to read/ write only in the DEVID mode.

DEVIDH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32

DEVIDL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD											DI4	DI3	DI2	DI1	DI0

Bits	Name	Function	After RSTN(SRST)
15	LD 0 1	Last Device flag Not Last Device Last Device	1
4-0	DI<4:0>	Device ID	00000

(3) Memory R/W Register Group

DEVSEL Register

DEVSELL:ADD<5:0>=08H

This register selects and accesses specific devices (Device Select) in a cascaded system. The BR bit is set to “1,” which means accessing all devices (Broadcast) immediately after the Device Reset operation. When accessing only one specific device, it is necessary to write BR = “0” (not Broadcast) and the Device ID which the user wishes to select in the DS<4:0> bits in this register.

DEVSELL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	DS4	DS3	DS2	DS1	DS0

Bits	Name	Function	After RSTN(SRST)
15	BR	Broadcast flag	1
	0	Not Broadcast	
	1	Broadcast	
4-0	DS<4:0>	Device ID to be accessed	00000

AR Register
ARL : ADD<5:0>=0AH

This register specifies the absolute address that is used for accessing the CAM by the MEMAR register. The data written in this register (00000000H ~ 00000FFFH) is the absolute address of the CAM. It is possible to read/write the stored data of the CAM specified by the absolute address by first writing the absolute address in this register then executing a read/write operation of the MEMAR register.

ARL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Bits	Name	Function	After RSTN(SRST)
11-0	AR<11:0>	Absolute address of the CAM table	ALL 0

MEMAR Register
MEMARL:ADD<5:0>=0CH,MEMARH:ADD<5:0>=0DH

This 64-bit register operates as a port for accessing the entry data of the CAM indicated by the AR register. When the entry data is accessed, “0” is input in the Empty Bit and the value defined by the CNTL1 register is input in the Permanent and Access Bits.

MEMARH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MA63	MA62	MA61	MA60	MA59	MA58	MA57	MA56	MA55	MA54	MA53	MA52	MA51	MA50	MA49	MA48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MA47	MA46	MA45	MA44	MA43	MA42	MA41	MA40	MA39	MA38	MA37	MA36	MA35	MA34	MA33	MA32

MEMARL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Bits	Name	Function	After RSTN(SRST)
63-0	MA<63:0>	Entry data indicated by the AR register	Unknown

Empty Bit : "0" is input.

Permanent Bit : The value defined by the CNTL1 register is input.

Access Bit : The value defined by the CNTL1 register is input.

MEMARAI Register
MEMARAIL:ADD<5:0>=0EH,
MEMARAIH:ADD<5:0>=0FH

This 64-bit register operates as a port for accessing the entry data of the CAM indicated by the AR register. When the entry data is accessed, “0” is input in the Empty Bit and the value defined by the CNTL1 register is input in the Permanent and Access Bits. The increment operation of the AR register is executed when this register is accessed. This operation is executed by access to this register in the 64-bit input mode. It is also executed by access to either the low side or the high side according to the definition of the endian of the CNTL1 register in the 32-bit input mode and the read operation.

MEMARAIH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MA63	MA62	MA61	MA60	MA59	MA58	MA57	MA56	MA55	MA54	MA53	MA52	MA51	MA50	MA49	MA48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MA47	MA46	MA45	MA44	MA43	MA42	MA41	MA40	MA39	MA38	MA37	MA36	MA35	MA34	MA33	MA32

MEMARAIL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Bits	Name	Function	After RSTN(SRST)
63-0	MA<63:0>	Entry data indicated by the ARAI register	Unknown

Empty Bit : "0" is input.

Permanent Bit : The value defined by the CNTL1 register is input.

Access Bit : The value defined by the CNTL1 register is input.

MEMAR_AT Register
MEMAR_ATL:ADD<5:0>=10H

This 64-bit register operates as a port for accessing the attribute data of the entry in the CAM indicated by the AR register.

MEMAR_ATL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										MSEM	EM	MSPM	PM	MSAC	AC

Bits	Name	Function	After RSTN(SRST)
5	MSEM 0 1	Empty Bit Mask EM is written in the Empty Bit. No change in the Empty Bit	Unknown
4	EM	Empty Bit data	Unknown
3	MSPM 0 1	Permanent Bit Mask PM is written in the Permanent Bit. No change in the Permanent Bit	Unknown
2	PM	Permanent Bit data	Unknown
1	MSAC 0 1	Access Bit Mask AC is written in the Access Bit. No change in the Access Bit	Unknown
0	AC	Access Bit data	Unknown

MEMHHA Register
MEMHHAL:ADD<5:0>=12H,
MEMHHAH:ADD<5:0>=13H

This 64-bit register operates as a port for accessing the entry data of the CAM indicated by the HHA register. Even if the entry data is modified-written by this register, the Empty, Permanent, and Access Bits of the entry do not change.

MEMHHAL Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MA63	MA62	MA61	MA60	MA59	MA58	MA57	MA56	MA55	MA54	MA53	MA52	MA51	MA50	MA49	MA48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MA47	MA46	MA45	MA44	MA43	MA42	MA41	MA40	MA39	MA38	MA37	MA36	MA35	MA34	MA33	MA32

MEMHHAH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Bits	Name	Function	After RSTN(SRST)
63-0	MA<63:0>	Entry data indicated by the HHA register	Unknown

The Empty, Permanent, and Access Bits do not change.

MEMHHA_ATRegister
MEMHHA_ATL:ADD<5:0>=14H

This 64-bit register operates as a port for accessing the attribute data of the entry in the CAM indicated by the HHA register.

MEMHHA_ATL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										MSEM	EM	MSPM	PM	MSAC	AC

Bits	Name	Function	After RSTN(SRST)
5	MSEM 0 1	Empty Bit Mask EM is written in the Empty Bit. No change in the Empty Bit	Unknown
4	EM	Empty Bit data	Unknown
3	MSPM 0 1	Permanent Bit Mask PM is written in the Permanent Bit. No change in the Permanent Bit	Unknown
2	PM	Permanent Bit data	Unknown
1	MSAC 0 1	Access Bit Mask AC is written in the Access Bit. No change in the Access Bit	Unknown
0	AC	Access Bit data	Unknown

MEMHEA Register
MEMHEAL:ADD<5:0>=16H,
MEMHEAH:ADD<5:0>=17H

This 64-bit register operates as a port for accessing the entry data of the CAM indicated by the HEA register. When the entry data is accessed, “0” is input in the Empty Bit and the value defined by the CNTL1 register is input in the Permanent and Access Bits.

MEMHEAH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MA63	MA62	MA61	MA60	MA59	MA58	MA57	MA56	MA55	MA54	MA53	MA52	MA51	MA50	MA49	MA48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MA47	MA46	MA45	MA44	MA43	MA42	MA41	MA40	MA39	MA38	MA37	MA36	MA35	MA34	MA33	MA32

MEMHEAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Bits	Name	Function	After RSTN(SRST)
63-0	MA<63:0>	Entry data indicated by the HEA register	Unknown

Empty Bit : "0" is input.

Permanent Bit : The value defined by the CNTL1 register is input.

Access Bit : The value defined by the CNTL1 register is input.

MEMHEAAI Register
MEMHEAAIL:ADD<5:0>=18H,
MEMHEAAIH:ADD<5:0>=19H

This 64-bit register operates as a port for accessing the entry data of the CAM indicated by the HEA register. When the entry data is accessed, “0” is input in the Empty Bit and the value defined by the CNTL1 register is input in the Permanent and Access Bits. The renew operation of the HEA register is executed when this register is accessed. This operation is executed by access to this register in the 64-bit input mode. It is also executed by access to either the low side or the high side according to the definition of the endian of the CNTL1 register in the 32-bit input mode.

MEMHEAAIH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MA63	MA62	MA61	MA60	MA59	MA58	MA57	MA56	MA55	MA54	MA53	MA52	MA51	MA50	MA49	MA48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MA47	MA46	MA45	MA44	MA43	MA42	MA41	MA40	MA39	MA38	MA37	MA36	MA35	MA34	MA33	MA32

MEMHEAAIL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA53	MA4	MA35	MA2	MA1	MA0

Bits	Name	Function	After RSTN(SRST)
63-0	MA<63:0>	Entry data indicated by the HEA register	Unknown

Empty Bit : "0" is input.

Permanent Bit : The value defined by the CNTL1 register is input.

Access Bit : The value defined by the CNTL1 register is input.

MEMHEA_AT Register
MEMHEA_ATL:ADD<5:0>=1AH

This 64-bit register operates as a port for accessing the attribute data of the entry in the CAM indicated by the HEA register.

MEMHEA_ATL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										MSEM	EM	MSPM	PM	MSAC	AC

Bits	Name	Function	After RSTN(SRST)
5	MSEM 0 1	Empty Bit Mask EM is written in the Empty Bit. No change in the Empty Bit	Unknown
4	EM	Empty Bit data	Unknown
3	MSPM 0 1	Permanent Bit Mask PM is written in the Permanent Bit. No change in the Permanent Bit	Unknown
2	PM	Permanent Bit data	Unknown
1	MSAC 0 1	Access Bit data AC is written in the Access Bit. No change in the Access Bit	Unknown
0	AC	Access Bit data	Unknown

(4) Configuration Register Group

MASK(0~11) Register

MASK0L : ADD<5:0>=1CH, MASK0H : ADD<5:0>=1DH,
MASK1L : ADD<5:0>=1EH, MASK1H : ADD<5:0>=1FH,
MASK2L : ADD<5:0>=20H, MASK2H : ADD<5:0>=21H,
MASK3L : ADD<5:0>=22H, MASK3H : ADD<5:0>=23H,
MASK4L : ADD<5:0>=24H, MASK4H : ADD<5:0>=25H,
MASK5L : ADD<5:0>=26H, MASK5H : ADD<5:0>=27H,
MASK6L : ADD<5:0>=28H, MASK6H : ADD<5:0>=29H,
MASK7L : ADD<5:0>=2AH, MASK7H : ADD<5:0>=2BH,
MASK8L : ADD<5:0>=2CH, MASK8H : ADD<5:0>=2DH,
MASK9L : ADD<5:0>=2EH, MASK9H : ADD<5:0>=2FH,
MASK10L : ADD<5:0>=30H, MASK10H : ADD<5:0>=31H,
MASK11L : ADD<5:0>=32H, MASK11H : ADD<5:0>=33H

There are 12, 64-bit Mask registers. Each register represents a different set of mask data. Each Mask register can be set for the search configuration respectively by the SCONF register. The value of these registers after initialization is unknown.

MASK(0~11)H Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
MS63	MS62	MS61	MS60	MS59	MS58	MS57	MS56	MS55	MS54	MS53	MS52	MS51	MS50	MS49	MS48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MS47	MS46	MS45	MS44	MS43	MS42	MS41	MS40	MS39	MS38	MS37	MS36	MS35	MS34	MS33	MS32

MASK(0~11)L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MS31	MS30	MS29	MS28	MS27	MS26	MS25	MS24	MS23	MS22	MS21	MS20	MS19	MS18	MS17	MS16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MS15	MS14	MS13	MS12	MS11	MS10	MS9	MS8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0

Bits	Name	Function	After RSTN(SRST)
63-0	MS<63:0>	Defines the MASK register.	Unknown

SCONF (Search Configuration) Register

SCONFL : ADD<5:0>=36H, SCONFH : ADD<5:0>=37H

This register sets the search configuration for 12 respective MASK registers, such as setting the Access Bit to “0” or “1” when the search result is a hit and setting the output operation for the Output Port.

SCONFH Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
				AS11	HE11	MH11	S11<1:0>		AS10	HE10	MH10	S10<1:0>		AS09	HE09
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MH09	S09<1:0>		AS08	HE08	MH08	S08<1:0>		AS07	HE07	MH07	S07<1:0>		AS06	HE06	MH06

SCONFL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S06<1:0>		AS05	HE05	MH05	S05<1:0>		AS04	HE04	MH04	S04<1:0>		AS03	HE03	MH03	S03<1>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S03<0>	AS02	HE02	MH02	S02<1:0>		AS01	HE01	MH01	S01<1:0>		AS00	HE00	MH00	S00<1:0>	

Bits	Name	Function	After RSTN(SRST)
59-4	AS*	Indicates whether the Access Bit which is hit is set to "1" or not.	0
	0	Not set	
	1	Set	
58-3	HE*	Indicates whether HEA is output or not in a no hit case.	0
	0	No output	
	1	Output	
57-2	MH*	Indicates whether the 16-bit fragment of MEMHHA is output or not.	0
	0	No output	
	1	Output	
56-0	S*<1:0>	When outputting MEMHHA, designates which 16-bit fragment of 64 bits to be output.	00
	00	MEMHHA<15:0>	
	01	MEMHHA<31:16>	
	10	MEMHHA<47:32>	
	11	MEMHHA<63:48>	

*: 00~11

(5) Comparand Register Group

CMP1/2 Register

CMP1L : ADD<5:0>=38H, CMP1H : ADD<5:0>=39H,
CMP2L : ADD<5:0>=3AH, CMP2H : ADD<5:0>=3BH

There are two 64-bit Comparand registers which can be used for the search operation and whose content can be written in the entry. When the SRCHN is active in the write operation to these registers, the search operation in the CAM is executed simultaneously.

CMP 1/2H Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
CP63	CP62	CP61	CP60	CP59	CP58	CP57	CP56	CP55	CP54	CP53	CP52	CP51	CP50	CP49	CP48
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
CP47	CP46	CP45	CP44	CP43	CP42	CP41	CP40	CP39	CP38	CP37	CP36	CP35	CP34	CP33	CP32

CMP 1/2L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CP31	CP30	CP29	CP28	CP27	CP26	CP25	CP24	CP23	CP22	CP21	CP20	CP19	CP18	CP17	CP16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bits	Name	Function	After RSTN(SRST)
63-0	CP<63:0>	Definition of the CMP register	ALL 0

(6) Table Status Register Group

HHA (Highest Hit Address) Register

HHAL : ADD<5:0>=3CH

This register stores the entry address of the hit entry after a search operation. When there is a single hit in a cascaded system, the HV flag is set to “0,” and the SYH flag is set to “1.” In other cases in a cascaded system, the HV flag is set to “1,” and the SYH flag is set to “0.” In the LD bit, the Last Device flag of the DEVSEL register of the device with single hit priority is output. When there is a multi-hit in a cascaded system, the SYM flag is set to “1.” When there is a single hit in a device, the HT flag is set to “1.” When there is a multi-hit in a device, the MH flag is set to “1.” SYE is the Empty flag of the cascaded system. The Device ID of the device with single hit priority is output in DI<4:0>. This register is allowed only to read in all modes.

HHAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HV	LD	SYH	SYM	HT	MH	SYE					DI4	DI3	DI2	DI1	DI0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				HA11	HA10	HA9	HA8	HA7	HA6	HA5	HA4	HA3	HA2	HA1	HA0

Bits	Name	Function	After RSTN(SRST)
31	HV 0 1	Single Hit Address Valid flag Valid Invalid	1
30	LD	Last Device flag	1
29	SYH 0 1	Single Hit flag in the cascaded system No Single Hit Single Hit	0
28	SYM 0 1	Multi-Hit flag in the cascaded system No Multi-Hit Multi-Hit	0
27	HT 0 1	Single Hit flag in the device No Single Hit Single Hit	0
26	MH 0 1	Multi-Hit flag in the device No Multi-Hit Multi-Hit	0
25	SYE 0 1	Empty flag in the cascaded system No Empty Entry Empty Entry	1
20-16	DI<4:0>	Device ID	00000
11-0	HA<11:0>	Highest Hit Address	ALL 0

HEA (Highest Empty Address) Register
HEAL: ADD<5:0>=3EH

This register stores the entry address with the highest empty priority among the empty entries. When there is no empty address, the EV flag is set to "1." The Last Device flag of the DEVSEL register of the device with empty priority is output in the LD bit. SYH and SYM are set in the same way as in the HHA register. SYE is the Empty flag in the cascaded system. ET is the Empty flag in the device.

HEAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EV	LD	SYH	SYM	▨	▨	SYE	ET	▨	▨	▨	DI4	DI3	DI2	DI1	DI0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
▨	▨	▨	▨	HE11	HE10	HE9	HE8	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0

Bits	Name	Function	After RSTN(SRST)
31	EV 0 1	Highest Empty Address Valid flag Valid Invalid	1
30	LD	Last Device flag	1
29	SYH 0 1	Single Hit flag in the cascaded system No Single Hit Single Hit	0
28	SYM 0 1	Multi-Hit flag in the cascaded system No Multi-Hit Multi-Hit	0
25	SYE 0 1	Empty flag in the cascaded system No Empty Entry Empty Entry	1
24	ET 0 1	Empty flag in the device No Empty Entry Empty Entry	1
20-16	DI<4:0>	Device ID	00000
11-0	HE<11:0>	Highest Empty Address	ALL 0

7.4 Conditions for Accessing Registers

Table 7.4.1 shows conditions for accessing registers.

				Broadcast			Device Select	
Name		R/W	Address<5:0>	Write	Read	Output Device	Write	Read
COML	Exist	W	00H	○	X	No device	△ *1	X
COMH	Not exist		01H					
CNTL1L	Exist	R/W	02H	○	○	Last Device	△ *1	○
CNTL1H	Exist	R/W	03H	○	○	Last Device	△ *1	○
CNTL2L	Exist	R/W	04H	○	○	Last Device	△ *1	○
CNTL2H	Not exist		05H					
DEVIDL	Exist	R/W	06H	○	○	DEVID priority device	X	X
DEVIDH	Not exist		07H					
DEVSELL	Exist	R/W	08H	○	○	Last Device	△ *1	○
DEVSELH	Not exist		09H					
ARL	Exist	R/W	0AH	○	○	Last Device	△ *1	○
ARH	Not exist		0BH					
MEMARL	Exist	R/W	0CH	○ *2	○	Last device	○	○
MEMARH	Exist	R/W	0DH	○ *2	○	Last device	○	○
MEMARAIL	Exist	R/W	0EH	○ *2	○	Last device	○	○
MEMARAIH	Exist	R/W	0FH	○ *2	○	Last device	○	○
MEMAR_ATL	Exist	R/W	10H	○ *2	○	Last device	○	○
MEMAR_ATH	Not exist		11H					
MEMHHAL	Exist	R/W	12H	○ *3	○	Hit priority device *4	○ *5	○ *6
MEMHHAH	Exist	R/W	13H	○ *3	○	Hit priority device *4	○ *5	○ *6
MEMHHA_ATL	Exist	R/W	14H	○ *3	○	Hit priority device *4	○ *5	○ *6
MEMHHA_ATH	Not exist		15H					
MEMHEAL	Exist	R/W	16H	○ *7	○	Empty priority device *8	○ *9	○ *10
MEMHEAH	Exist	R/W	17H	○ *7	○	Empty priority device *8	○ *9	○ *10
MEMHEAAIL	Exist	R/W	18H	○ *7	○	Empty priority device *8	○ *9	○ *10
MEMHEAAIH	Exist	R/W	19H	○ *7	○	Empty priority device *8	○ *9	○ *10
MEMHEA_ATL	Exist	R/W	1AH	○ *7	○	Empty priority device *8	○ *9	○ *10
MEMHEA_ATH	Not exist		1BH					

Table 7.4.1 Conditions for accessing registers

				Broadcast			Device Select	
Name		R/W	Address<5:0>	Write	Read	Output Device	Write	Read
MASK0L	Exist	R/W	1CH	○	○	Last device	○	○
MASK0H	Exist	R/W	1DH	○	○	Last device	○	○
MASK1L	Exist	R/W	1EH	○	○	Last device	○	○
MASK1H	Exist	R/W	1FH	○	○	Last device	○	○
MASK2L	Exist	R/W	20H	○	○	Last device	○	○
MASK2H	Exist	R/W	21H	○	○	Last device	○	○
MASK3L	Exist	R/W	22H	○	○	Last device	○	○
MASK3H	Exist	R/W	23H	○	○	Last device	○	○
MASK4L	Exist	R/W	24H	○	○	Last device	○	○
MASK4H	Exist	R/W	25H	○	○	Last device	○	○
MASK5L	Exist	R/W	26H	○	○	Last device	○	○
MASK5H	Exist	R/W	27H	○	○	Last device	○	○
MASK6L	Exist	R/W	28H	○	○	Last device	○	○
MASK6H	Exist	R/W	29H	○	○	Last device	○	○
MASK7L	Exist	R/W	2AH	○	○	Last device	○	○
MASK7H	Exist	R/W	2BH	○	○	Last device	○	○
MASK8L	Exist	R/W	2CH	○	○	Last device	○	○
MASK8H	Exist	R/W	2DH	○	○	Last device	○	○
MASK9L	Exist	R/W	2EH	○	○	Last device	○	○
MASK9H	Exist	R/W	2FH	○	○	Last device	○	○
MASK10L	Exist	R/W	30H	○	○	Last device	○	○
MASK10H	Exist	R/W	31H	○	○	Last device	○	○
MASK11L	Exist	R/W	32H	○	○	Last device	○	○
MASK11H	Exist	R/W	33H	○	○	Last device	○	○
SCONFL	Exist	R/W	36H	○	○	Last device	○	○
SCONFH	Exist	R/W	37H	○	○	Last device	○	○
CMP1L	Exist	R/W	38H	○	○	Last device	○	○
CMP1H	Exist	R/W	39H	○	○	Last device	○	○
CMP2L	Exist	R/W	3AH	○	○	Last device	○	○
CMP2H	Exist	R/W	3BH	○	○	Last device	○	○
HHAL	Exist	R	3CH	X	○	Hit priority device *4	X	○ *6
HHAH	Not exist		3DH					
HEAL	Exist	R	3EH	X	○	Empty priority device *8	X	○ *10
HEAH	Not exist		3FH					

Table 7.4.1 Conditions for accessing registers (cont'd)

○	: allowed
△	: allowed but not selectable
X	: not allowed

*1 The write operation is executed for all devices. (It is not possible to specify the device.)

*2 The write operation is executed for all devices (but not usually used).

*3 The write operation is executed only in the device with a single hit. (i.e. no write operation in the device with a multi-hit or no hit)

When there is a multi-hit in the simple cascaded system, the write operation is executed in the device with the highest Hit Priority among devices excluding the one with a multi-hit.

*4 The device with a single hit outputs the data. (The device with a multi-hit or no hit does not output the data.)

When there is a multi-hit in the simple cascaded system, the device with the highest Single Hit Priority among devices, excluding the one with a multi-hit, outputs the data. However, it is necessary that Hit Priority is propagated. When there is no device with a single hit in the system, the Last Device outputs invalid data.

*5 The write operation is not executed when there is a multi-hit or no hit in the selected device.

*6 Invalid data is output when there is a multi-hit or no hit in the selected device.

*7 The write operation is not executed when there is no device with Empty Priority. (i.e. Write operation is executed only in the device with Empty Priority.)

*8 Data is output from the device with Empty Priority. (When there is no device with Empty Priority in the cascaded system, the Last Device outputs invalid data.)

*9 The write operation is not executed when the selected device does not have empty entry.

*10 Invalid data is output when the selected device does not have Empty Priority.

Table 7.4.1 Conditions for accessing registers (cont'd)

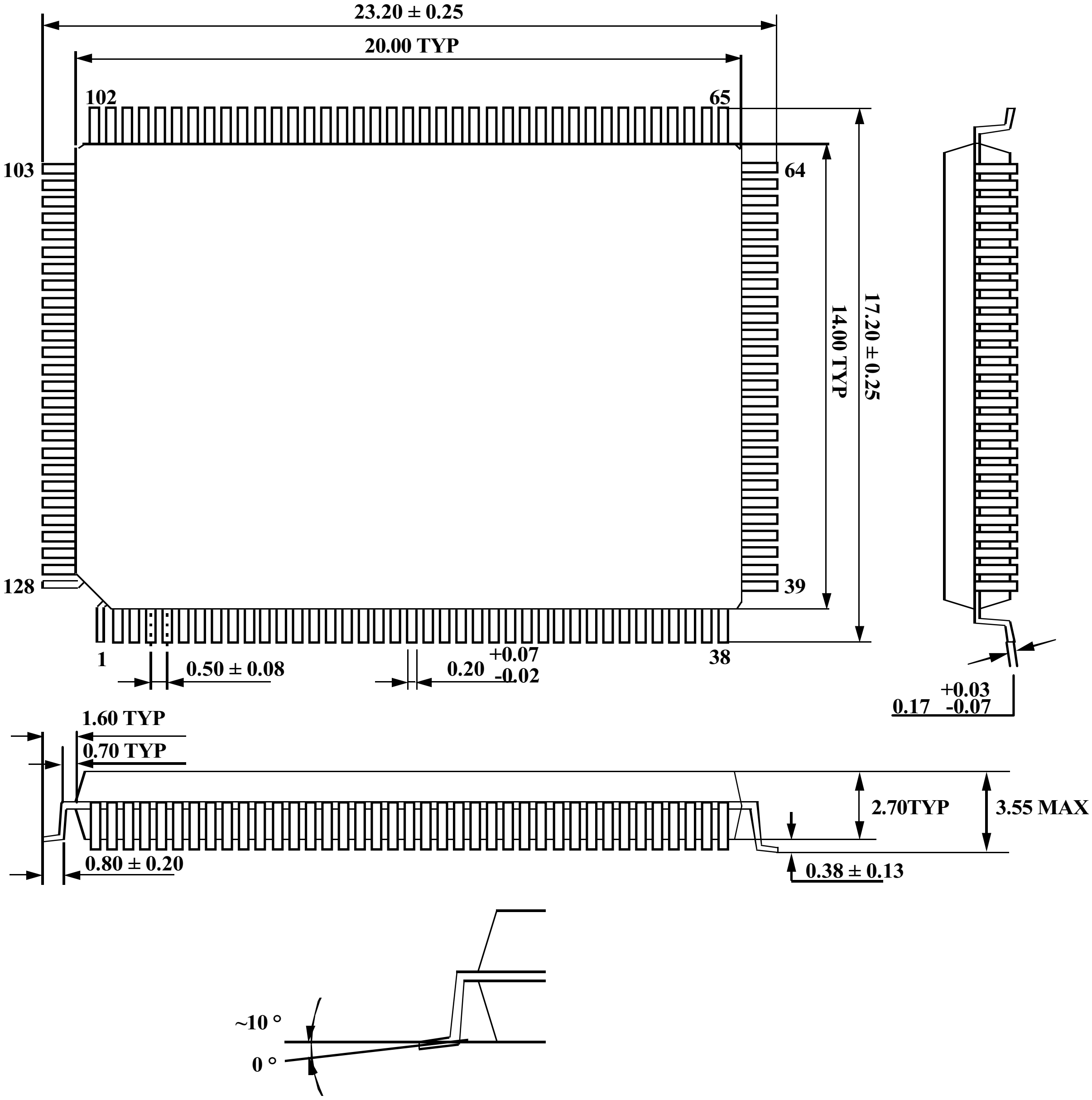
8. Package/Ordering Information

8.1 Ordering Information

Part Number	**Package**	**Marking**
KE5BGCA256ACFP	**DPH SQFP128 *1**	**KE5BGCA256A**

*1 DPH (Die Pad Heat Spreader)

8.2 Package Drawing



Unit: mm

9. Electrical Characteristics

9.1 Absolute Maximum Rating

ITEM	SYMBOL	STANDARD CONDITION	UNIT	NOTE
Supply Voltage	VDD	-0.3 ~ 4.0	V	
Input Voltage	VI	-0.3 ~ VDD +0.3	V	*1
Output Voltage	VO	-0.3 ~ VDD +0.3	V	*1
I/O Voltage	VIO	-0.3 ~ VDD +0.3	V	*1
Storage Temperature	TSTG	-40 ~ +125	°C	

*1 Input/Output pins are not 5V tolerant I/O pins.

9.2 Operating Range

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	TA	0	+25	+70	°C

9.3 DC Characteristics

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 8mA, 4mA *2
Output High Voltage	VOH	2.4			V	IOH = -8mA, -4mA *2
Input Leakage Current	IIL	-10			µA	VIN = GND
	IIH			10	µA	VIN = VDD
Output Leakage Current	IOZ	-10		10	µA	Output is high impedanc
Standby Current	IDDS			T.B.D.	µA	
Dynamic Operating Current	IDDOP		T.B.D.		mA	

*2 In case of FLON, PHON, PMON pins : IOL = 4mA, -4mA Other output pins : IOL = 8mA, -8mA

9.4 AC Characteristics

TA = 0 ~ 70 °C, VDD = 3.3 V ± 0.3V

No.	Parameter	MIN	MAX	Unit	Note
1	CLK cycle time	15		ns	
2	CLK width high	5		ns	
3	CLK width low	5		ns	
4	DAT<31:0> setup time to CLK	3		ns	
5	DAT<31:0> hold time after CLK	1		ns	
6	ADD<5:0> setup time to CLK	3		ns	
7	ADD<5:0> hold time after CLK	1		ns	
8	PHASE setup time to CLK	3		ns	
9	PHASE hold time after CLK	1		ns	
10	SRCHN setup time to CLK	3		ns	
11	SRCHN hold time after CLK	1		ns	
12	RWN setup time to CLK	3		ns	
13	RWN hold time after CLK	1		ns	
14	CEN setup time to CLK	3		ns	
15	CEN hold time after CLK	1		ns	
16	MS<3:0> setup time to CLK	3		ns	
17	MS<3:0> hold time after CLK	1		ns	
18	OEDATN setup time to CLK	3		ns	
19	OEDATN hold time after CLK	1		ns	
20	OEODN setup time to CLK	3		ns	
21	OEODN hold time after CLK	1		ns	
22	OPSL setup time to CLK	8		ns	
23	OPSL hold time after CLK	1		ns	
24	PHIN setup time to CLK	3		ns	*1
25	PHIN hold time after CLK	3		ns	*1
26	PMIN setup time to CLK 1	3		ns	*1
27	PMIN hold time after CLK 1	3		ns	*1

*1 When the operation which needs priority determination falls under one of the cases shown below, the setup/hold time must be counted from 3 clock after the input operation .

1) MEMHHA (Read/Write)

2) MEMHEA (Read/Write), MEMHEAAI (Read/Write)

3) STR1_HHA, STR2_HHA command

4) STR1_HEA, STR2_HEA, STR1_HEAAI, STR2_HEAAI command

5) STR1_AUT, STR2_AUT, STR1_AUTAI, STR2_AUTAI command

*1 When the operation which needs priority determination is HHA or HEA (Read) operation, the setup/hold time must be counted from 5 clock after the input operation . See Fig. 9.4.1.

No.	Parameter	MIN	MAX	Unit	Note
28	PMIN setup time to CLK 2	3		ns	*1a
29	PMIN hold time after CLK 2	2		ns	*1a
30	FLIN setup time to CLK	3		ns	*1
31	FLIN hold time after CLK	3		ns	*1
32	CLK high to DAT<31:0> active		17	ns	*2
33	DAT<31:0> valid from CLK		20	ns	*2
34	DAT<31:0> hold after CLK	3		ns	*2
35	CLK high to OD<20:0> active		17	ns	*2
36	OD<20:0> valid from CLK		20	ns	*2
37	OD<20:0> hold after CLK	3		ns	*2
38	CLK high to SHON active 1		16	ns	*2
39	CLK high to SMON active 1		16	ns	*2
40	CLK high to SHON active 2		16	ns	*3
41	CLK high to SMON active 2		16	ns	*3
42	CLK high to PHON active 1		65	ns	*4
43	CLK high to PHON inactive 1	5		ns	*4
44	CLK high to PMON active 1		65	ns	*4
45	CLK high to PMON inactive 1	5		ns	*4
46	CLK high to FLON active 1		55	ns	*4
47	CLK high to FLON inactive 1	5		ns	*4
48	CLK high to PHON active 2		50	ns	*5
49	CLK high to PHON inactive 2	5		ns	*5
50	CLK high to PMON active 2		50	ns	*5
51	CLK high to PMON inactive 2	5		ns	*5
52	CLK high to PMON active 3		25	ns	*6
53	CLK high to PMON inactive 3	4		ns	*6
54	CLK high to FLON active 2		50	ns	*5
55	CLK high to FLON inactive 2	5		ns	*5

*1a When the operation which needs priority determination is NXT_PR command operation, the setup/hold time must be counted from 2 clock after the input operation . See Fig. 9.4.1.

*2 Counted from CLK when PHASE is low. Latency must be added. See Fig. 9.4.2.

*3 SHON and SMON transition by the SRST command. See Fig. 9.4.3.

*4 When the operation which changes the priority falls under one of the cases shown below, this must be counted from 3 clock after operation input. See Fig. 9.4.4.

1) Search operation by the SRCHN pin 2) Search operation by the SRCH command
3) MEMHEAAI (Read/Write) 4) Execution of the NXT_HEA, GEN_FL, STR1_HEAAI, STR2_HEAAI, STR1_AUTAI, or STR2_AUTAI commands

*5 PHON, PMON and FLON transition from high to low by the SRST command. See Fig. 9.4.5.

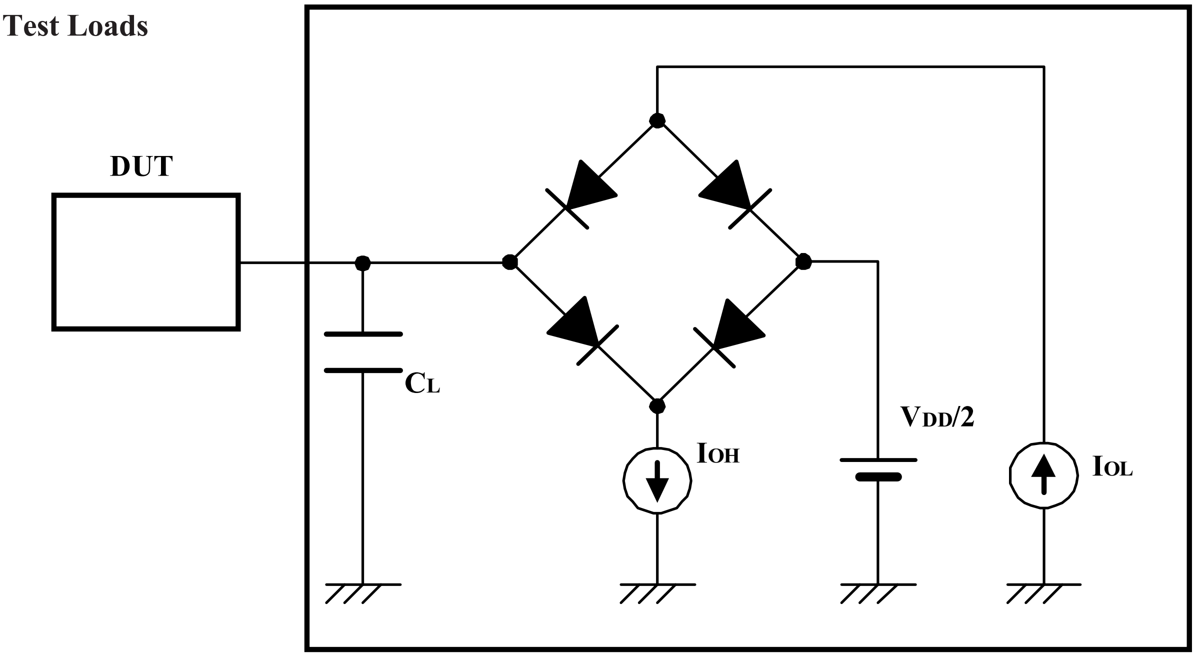
*6 PMON transition by the STR_DEV, END_DEV, or NXT_PR commands. See Fig. 9.4.6.

No.	Parameter	MIN	MAX	Unit	Note
56	PHIN to PHON active		18	ns	
57	PHIN to PMON active		18	ns	
58	PMIN to PMON active		18	ns	
59	FLIN to FLON active		18	ns	
60	RSTN low to PHON active		45	ns	
61	RSTN low to PMON active		45	ns	
62	RSTN low to FLON active		45	ns	
63	RSTN width low	60		ns	

Note: Characteristics are measured under the following conditions:

Input "H" level	3.3 V
Input "L" level	0.0 V
Input "H" reference voltage	1.5 V
Input signal through rate	1.0 ns/V
Output judgment level	VDD/2
Load capacitance (CL)	100 pF (DAT<31:0>)
Load capacitance (CL)	50 pF (other than DAT<31:0>)
"H" level output loading current (IOH)	-4 mA (FLON, PHON, PMON pins), -8mA (other pins)
"L" level output loading current (IOL)	4 mA (FLON, PHON, PMON pins), 8mA (other pins)

Test Loads



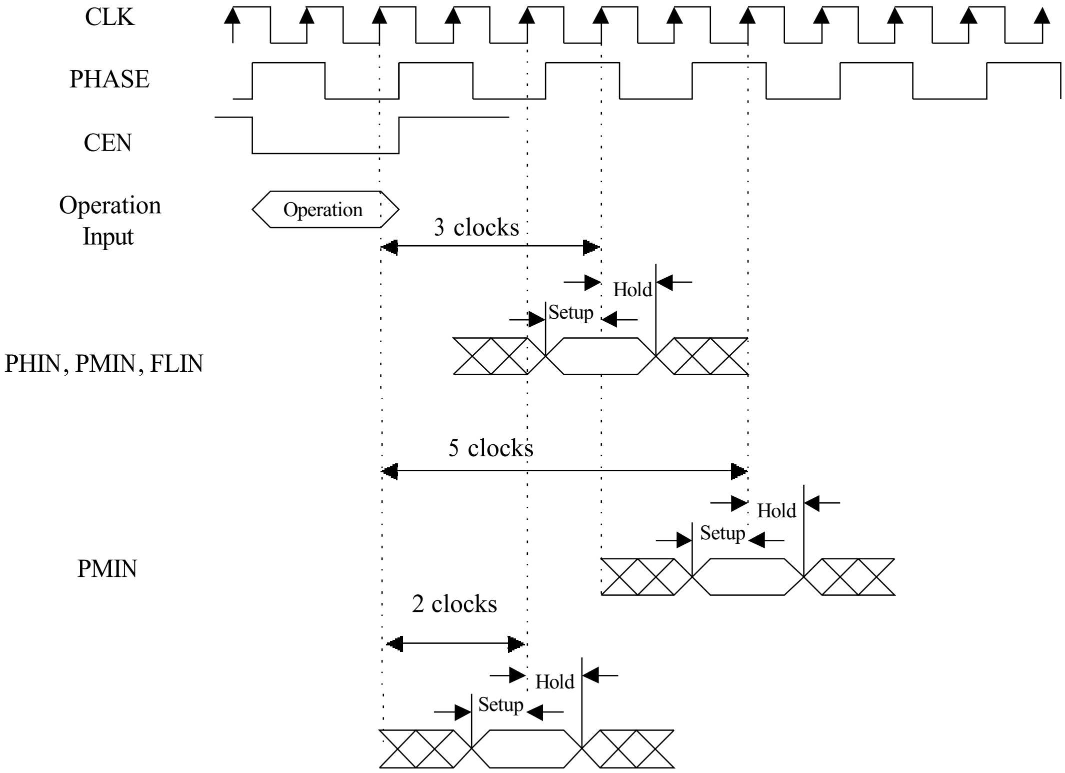


Fig. 9.4.1 Setup/hold time count of PHIN, PMIN, and FLIN

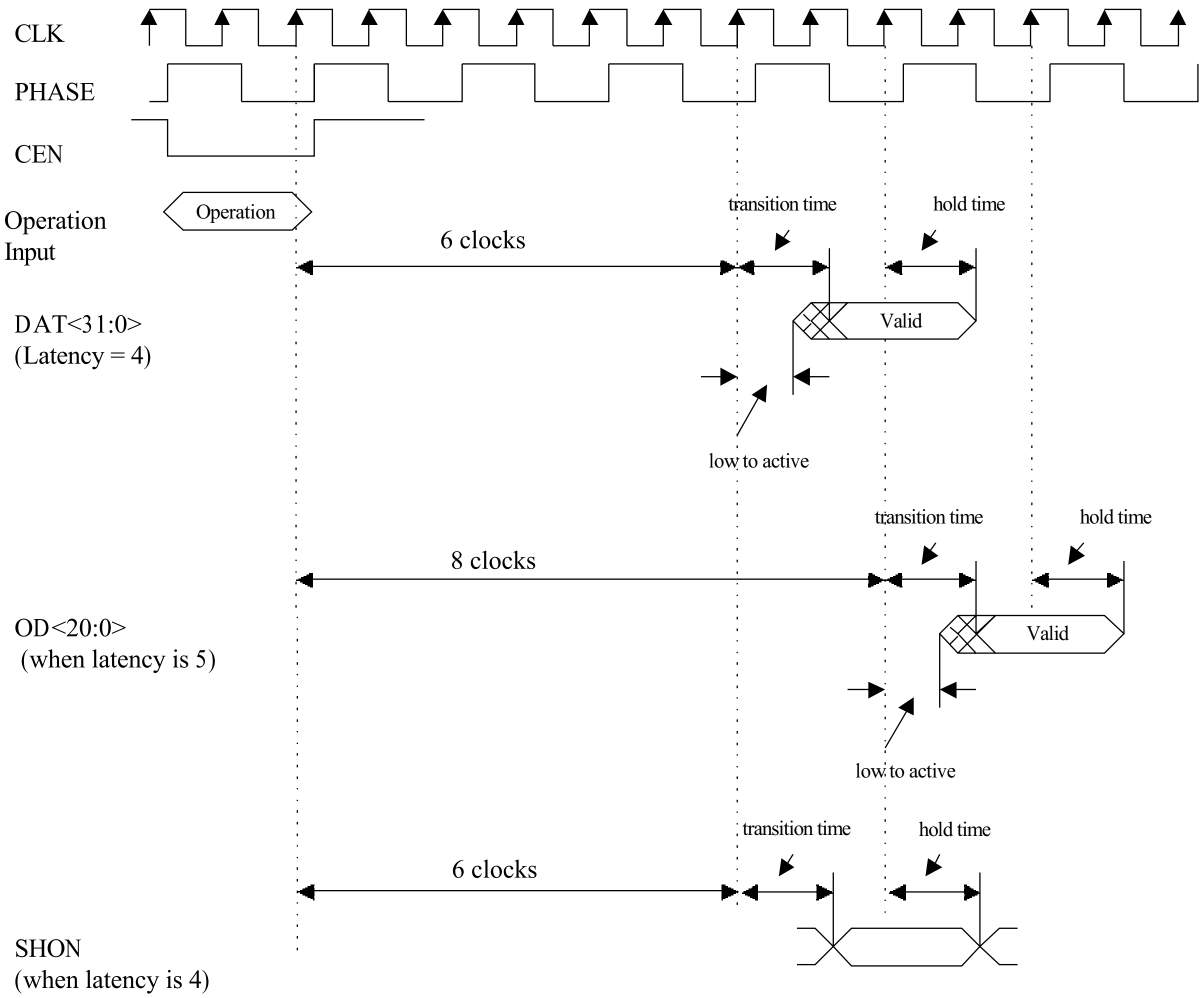


Fig. 9.4.2 Output cycle of DAT<31:0>, OD<20:0>, SHON, and SMON

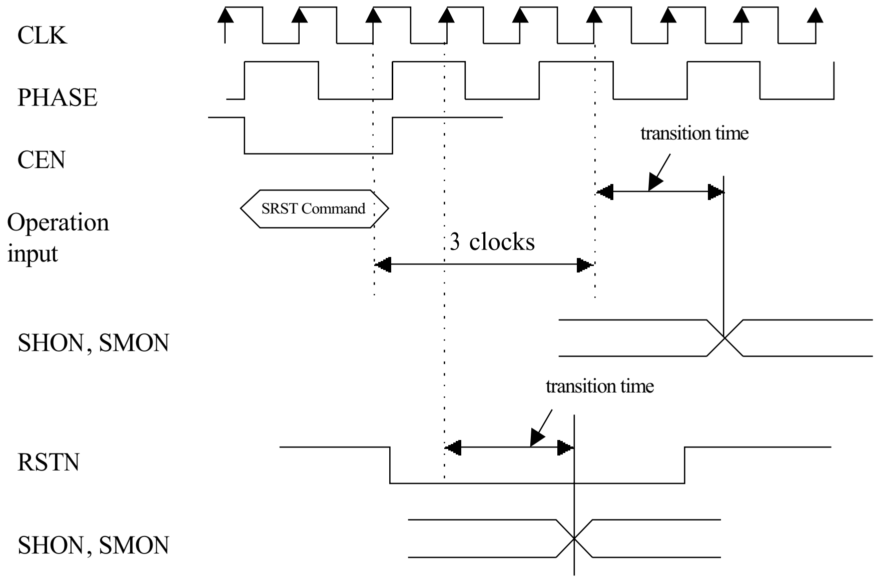


Fig. 9.4.3 Output cycle of SHON and SMON

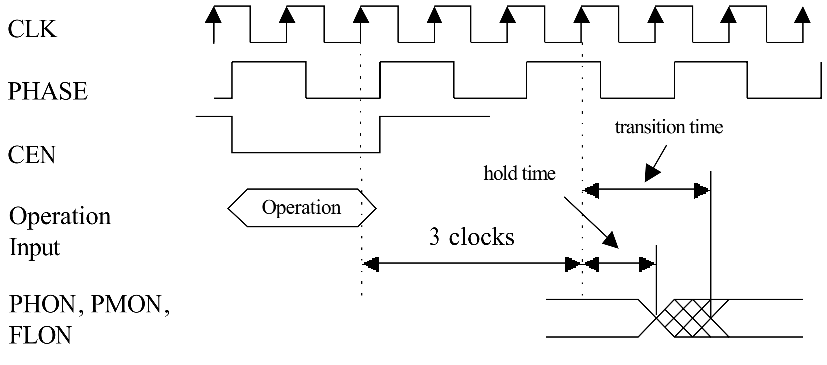


Fig. 9.4.4 Output cycle of PHON, PMON, and FLON

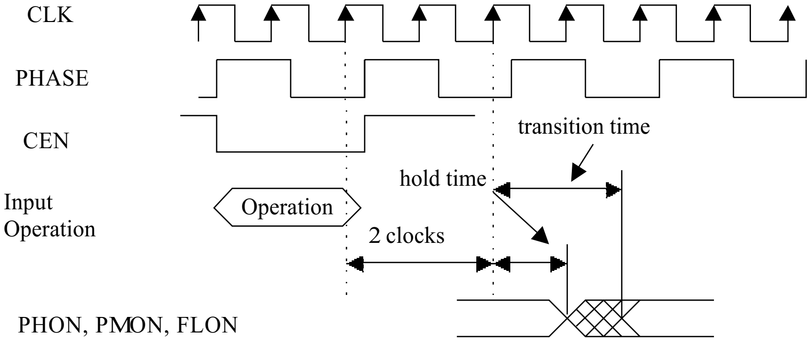


Fig. 9.4.5 Output cycle of PHON, PMON, and FLON

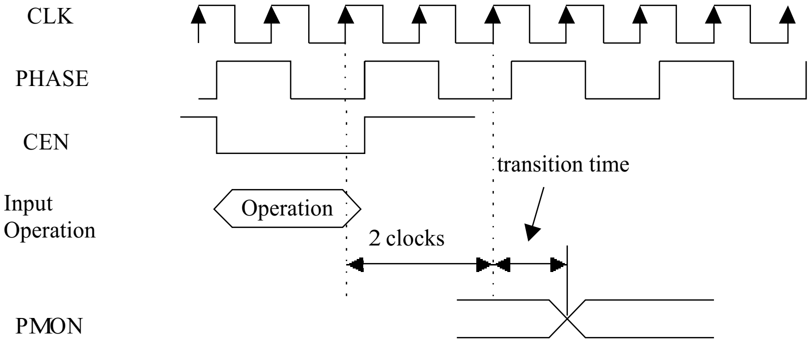
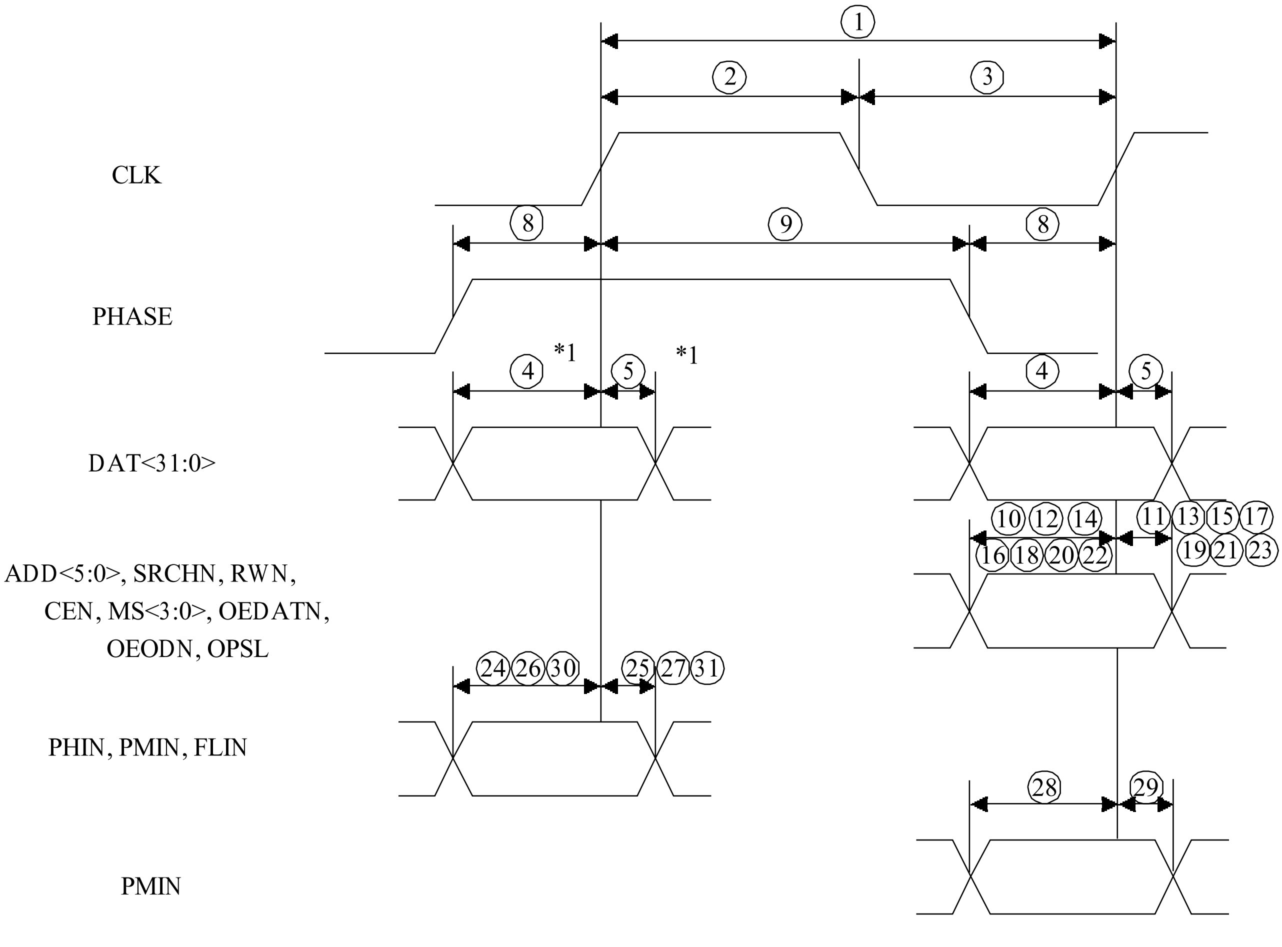
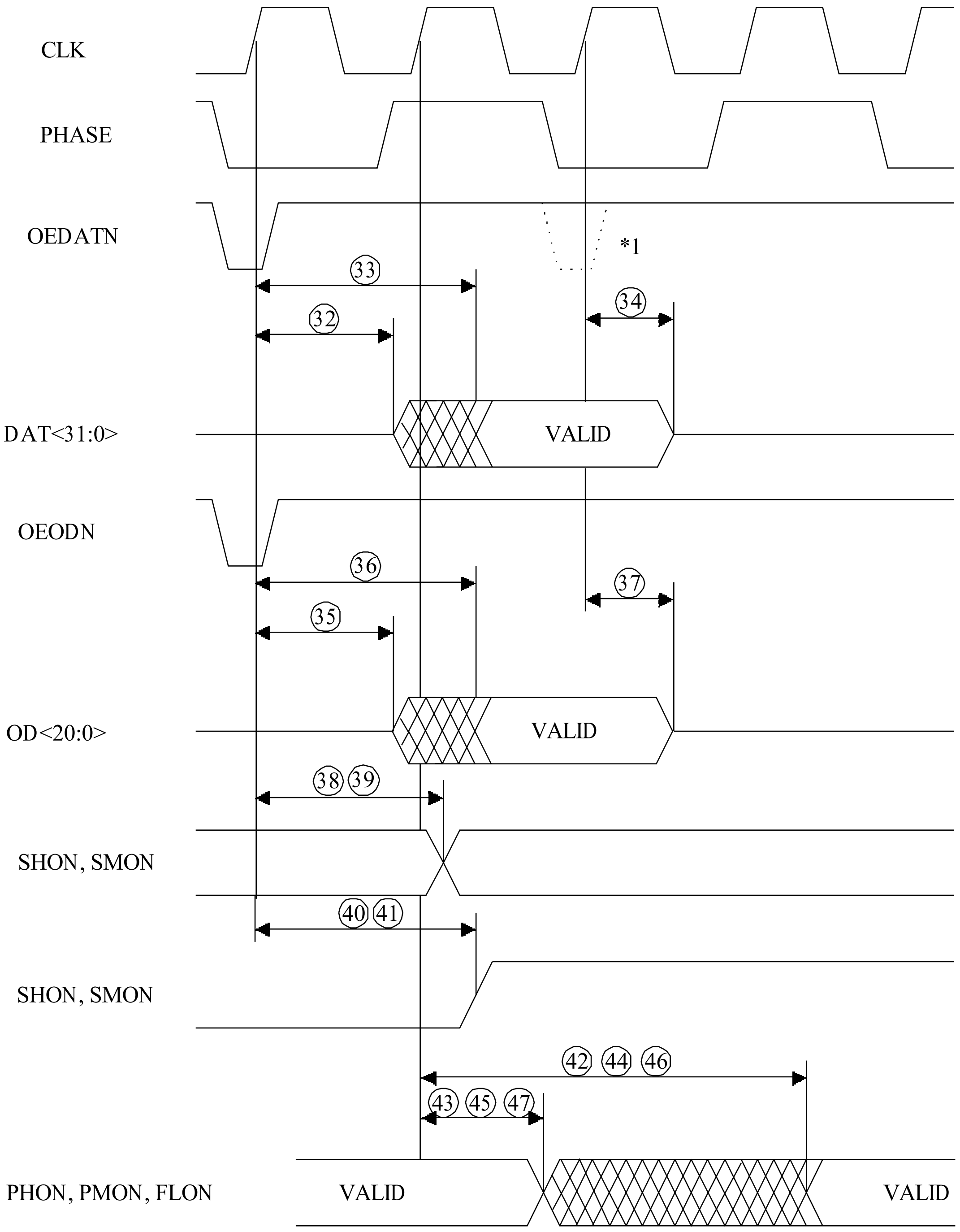


Fig. 9.4.6 Output cycle of PMON



*1 Necessary when the input mode is 64 bits.

Fig.9.4.7 (a) AC Specifications



*1 When the read operation has finished, this is Hi-Z even if OEDATN is "0."

Fig.9.4.7 (b) AC Specifications (cont'd)

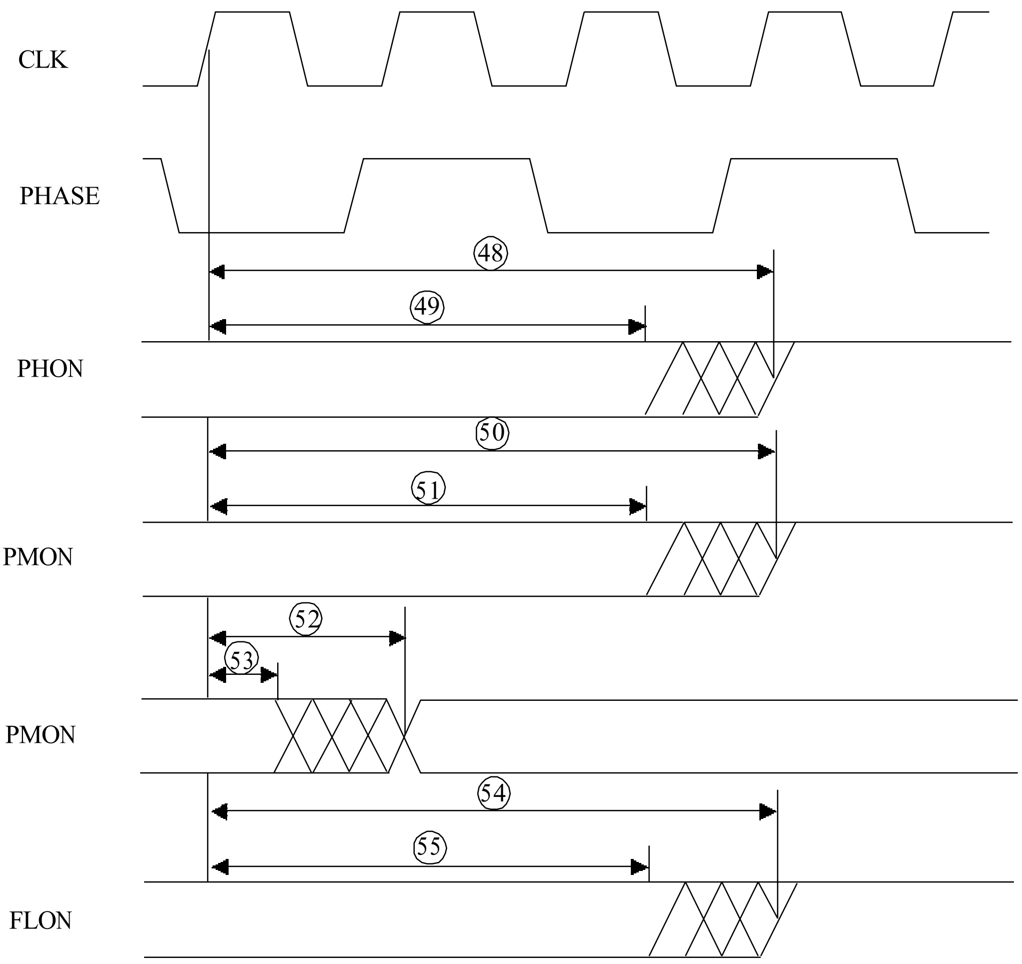


Fig.9.4.7 (c) AC Specifications (cont'd)

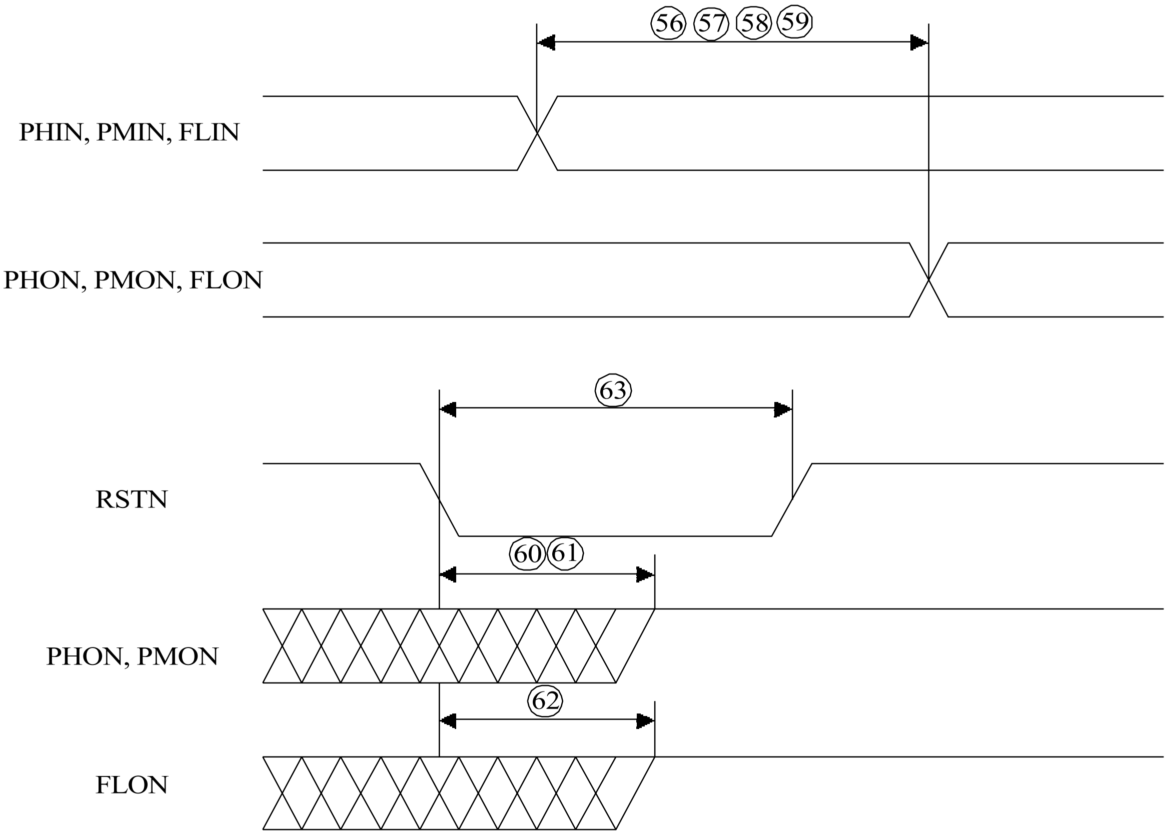


Fig.9.4.7 (d) AC Specifications (cont'd)

9.5. Power Consumption

The power consumption requirements for KE5BGCA256 differ from operating conditions. This section explains the methods of estimation for power consumption under both normal and worst-case operating conditions.

A) Power Consumption under normal operating conditions

Fig. 9.5.1 shows differences in power consumption between a search operation and another operation such as Read and Write.

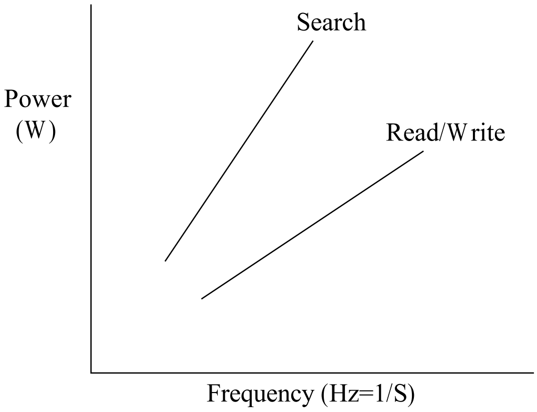


Fig. 9.5.1 Power Consumption under Normal Operating Condition

The power consumption is calculated by the following equation:

Pt = Psrch + Prw (W)

Where

Pt: Total power consumption (W)
Psrch: Power consumption for a search operation (W)
Prw: Power consumption for operations other than search

Psrch and Prw are given by the following equation:

Psrch = Ksrch * Fsrch (W)

Ksrch: Constant = 7.77E-8 (W*S)
Fsrch: Number of searches per second (1/S)

Prw = Krw * Frw (W)

Krw: Constant = 3.14E-8 (W*S)
Frw: Number of operations other than search per second (1/S)

Example:

If two search operations and two read/write operations are performed every 200nsec, the power consumption is as follows:

Psrch = 7.77E-8 x 2 / 200E-9 = 0.777 (W)
Prw = 3.14E-8 x 2 / 200E-9 = 0.314 (W)

The total is: Pt = 0.777 + 0.314 = 1.091 (W)

B) Power consumption under worst-case conditions

The power consumption is susceptible to such conditions as voltage, temperature, and process. Table 9.5.1 shows process, voltage, and temperature derating factors to be considered for predictions in a worst-case behavior.

Temperature	Temperature Deratings	Supply Voltage	Voltage Deratings	Process	Process Deratings
125••	1.06	3.600V	1.20	worst	1.02
100••	1.04	3.465V	1.10	typical	1.00
90••	1.03	3.300V	1.00	best	0.98
85••	1.03	3.135V	0.89		
70••	1.02	3.000V	0.81		
25••	1.00				
0••	1.00				

Table 9.5.1 Derating Factors for Power Consumption

In order to calculate the power consumption under various operating conditions, apply the relevant derating factors in Table 9.5.1 to the power consumption value calculated under typical operating conditions.

C) Guidelines for package mounting

The recommended maximum junction temperature of KE5BGCA256 is 110°C. Ensure that the estimated chip power is equal to or less than the value calculated by the following equation:

$$\mathbf{P} \leq (\mathrm{Tjrmax} - \mathrm{Ta}) / \theta\,\mathrm{ja}$$

Where

Tjrmax: Recommended maximum junction temperature (=110°C)
Ta: Ambient temperature
θja: Package thermal impedance
= 22.9°C/W and no air flow
19.5°C/W and air flow at 0.5m/S

Notes:

**The package thermal impedance value assumes the printed circuit board wiring density as 100%. For multiple-layer printed circuit boards, the value is defined as the total sum of the wiring density of each layer. For instance, a triple-layer printed circuit board may allocate 30% of its wiring density to the first layer and second layer and 40% to the third layer, totaling 100%. If the wiring density value exceeds 100%, the package thermal impedance will be reduced.*

***It is necessary to attach a heatsink or a fin on this device according to users environment. Consult the local Kawasaki LSI sales office.*

History of revises

Ver. 1.0.0 => Ver. 1.1.0

1) Section 9.5 "Power Consumption" is added.

Ver.1.1.0=>Ver.1.1.1

1) Errata of Part No. is corrected in P8-1;
   KE5BGCA256CFP->KE5BGCA256ACFP

2) Some comments are changed in P8-1 and P8-2.

3) Some comments are changed in P9-15 Notes.

4) East office address is changed in backface.

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