DESCRIPTION

The bridge is intended to adapt an ATA100 Disk drive to a Serial ATA Host.
This chip is a drop-in solution that is compatible with existing ATA software drivers and will run on standard operating systems without modification.

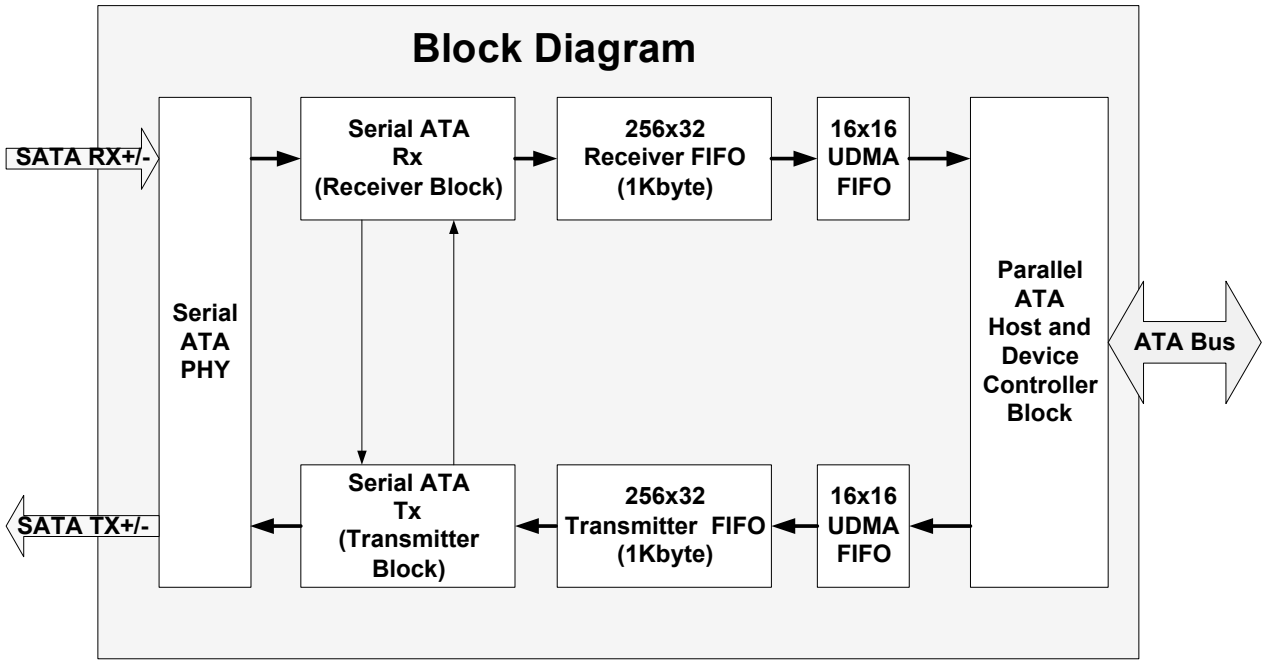
After the wakeup routine is completed between the Host and Bridge with both in alignment, the Bridge will wait for a Host to Device FIS then transfer the Task file parameters to the drive. Any Host to Device FIS will update the Drive Task File. Any Drive Interrupt will initiate a Device to Host FIS to update the Hosts shadow Registers.

With any Drive Task File update, the Bridge will determine the future data transfer direction and transfer type. The DMA control decode in the Host to Device FIS will initiate an Ultra DMA transfer sequence to the transmit FIFO or from the receive FIFO. If a write transfer was decoded a DMA Activate FIS is transmitted to the Host then the Bridge will wait for a Data Host to Device FIS before initiating the Drive data transfer. For a read decode, the bridge will transmit a Data Device to Host FIS when the Drive data transfer starts.

When a power management request primitive is received from the Host, the Bridge will respond with a power management acknowledge primitive then it will idle the Transmit Driver and enter a low power state. To exit this low power state, a wakeup routine must be initiated by the Host.

FEATURES

- Serial ATA rev1 compliant- Generation 1 Target.
- ATA6 compliant Drive interface Host.
- Big Drive Interfacing- 48 bit block Addressing.
- OOB COMRESET and COMAWAKE Detection.
- OOB COMINIT and COMWAKE Generation.
- 8B/10B Encoding and Decoding.
- Separate Cont and Data Scramblers.
- 32 bit Internal Buses for Encoding/Decoding/CRC Generating/Checking and Scrambling.
- Ultra-DMA with separate 16 bit CRC Generator.
- 15X PLL for Bit Clock Generation- 100 MHz REFCLOCK.
- Clock Recovery PLL for Deserializer and Decoder circuits.
- Primitive Decoder with auto Task File Updating.
- Dual 256 Double Word Transmit/Receive FIFO’s for over run prevention.
- Auto Inserted Hold Primitives to prevent under runs.
- Receiver impedance equalization for best system performance.
- Power Monitor for glitch free Power Off/On cycles.
- Power Management modes activated by the PMREQ Primitives.


Block Diagram
SATA RX+/-
Serial ATA Rx (Receiver Block)
256x32 Receiver FIFO (1Kbyte)
16x16 UDMA FIFO
Parallel ATA Host and Device Controller Block
ATA Bus
Serial ATA PHY
SATA TX+/-
Serial ATA Tx (Transmitter Block)
256x32 Transmitter FIFO (1Kbyte)
16x16 UDMA FIFO