LinearDimensions
SEMICONDUCTOR

LND-TRN902

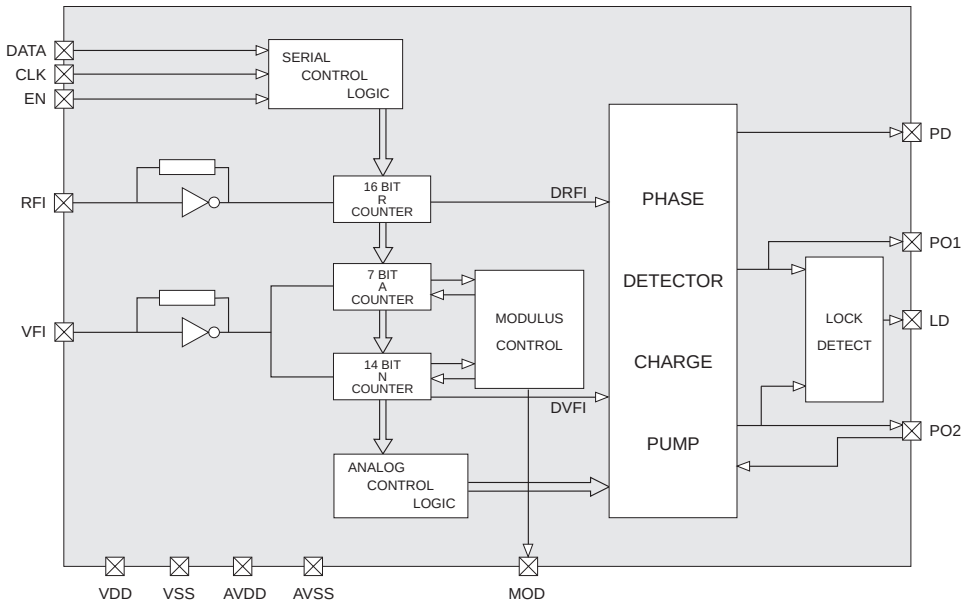
PLL-FREQUENCY SYNTHESIZER

LND-TRN902
PLL-FREQUENCY SYNTHESIZER

Features

- Low operating curremt consumption (typical 4 mA)
- High input sensetivity, high input frequencies (50 MHz)
- Synchronous programming of the counters (n-, n/a, r-counters)
- Switchable modulus trigger edge
- Large dividing ratios for small channel spacing
  - A counter 0 to 127
  - N counter 3 to 16,380
  - R counter 3 to 65,535
- Serial control:
- 3-wire bus: data, clock (<10 MHz), enable
- Switchable polarity and programmable phase detector current
- 2 programmable outputs
- Digital phase detector output signals (e.g. for external charge pump)
- DRFIN, DVFI outputs (e.g. for prescalar standby)
- External current setting for PD output
- Lock detect outpuut with gated anti-backlash pulse (quasi digital lock detect)
- ESD protection in accordance with MIL-STDs

Block Diagram



Linear Dimensions, Inc. 445 East Ohio Street, Chicago, IL 60611 p 312.3211810 f 312.321.1830

Pin Definitions and Functions

Pin No.	Symbol	Function
1	RFI	Reference Frequency High sensitivity preamplifier input for the r-counter. The input can be AC-coupled for small input signals or DC-coupled for large input signals.
2	VSS	Ground for the digital logic
3	EN	3-Wire Interface: Enable Enable line of the serial interface with internal pull-up resistor. When EN = H, the input signals CLK and DATA are internally disabled. When EN = L, the received data is transferred to the latches on the positive edge of the EN-signal.
4	DATA	3-Wire Interface: Data Serial data input with internal pull-up resistor. The last two bits before the EN-signal define the destination address.
5	CLK	3-Line Interface : Clock Clock line with internal pull-up resistor. The serial data is read into the internal shift register on the positive edge (see pulse diagram for serial data control)
6	VDD	Positive supply voltage for the digital logic
7	MOD	Modulus Control for external dual modulus prescaler. The modulus output is low at the beginning of the cycle. When the a-counter has reached its set value, MOD switches to high. When the n-counter has reached its set value, MOD switches to low and the cycle starts again. When the prescaler has the counter factor P or P+1 (P for MOD = H, P+1 for MOD =L), the overall scaling factor is NP + A. The value of the a-counter must be smaller than that of the n-counter. The trigger edge of the modulus signal to the input signal can be selected (see programming tables and MOD A, B) according to the needs of the prescaler. In single modulus operation and for standby operation in dual modulus operation, the output is low.
8	VFI	VCO-Frequency High sensitivity preamplifier input for the n-counter. The input can be AC-coupled for small input signals or DC-coupled for large input signals.
9	AVSS	Ground for the analog logic (Note: The pins VDD and AVDD and also pins VSS and AVSS must have the same supply voltage.)
10	PD	Phase Detector Tristate charge pump output. The level of the charge pump output current can be programmed using the digital interface. frequency DVFI < DRFI p-channel current source active frequency DVFI > DRFI n-channel current source active frequency DVFI = DRFI and PLL locked PD-output is tristate standby mode PD-output is tristate The polarity of the output signals of the phase detector can be programmed.
11	AVDD	Positive supply voltage for the analog logic (Note: The pins VDD and AVDD and also pins VSS and AVSS must have the same supply voltage.)
12	PO1	Programmable Output for the signals DRFIN, PHIV, PHIVN and PROBIT. (DRFIN, DVFIN, PHIVN are the inverted signals of DRFI, DVFI, PHIV.)
13	PO2	Programmable I/O-Pin for the output signals DVFI, PHIR and the input signal IREF - The signals PHIR and PHIV are the digital output signals of the phase and frequency detector for use with external active current sources. - The signals DRFIN and DVFIN are the scaled down signals of the reference frequency and VCO-frequency. - The programmed bit PROBIT is assigned to the PO1 output in the internal charge pump mode. The standby mode does not affect this function. - In the internal charge pump mode the input signal IREF determines the value of the PD-output current.
14	LD	Lock Detector (open drain) Unipolar output of the phase detector in the form of a pulse-width modulated signal. The LD-pulse width corresponds to the phase difference. In the locked state the LD-signal is at H-level. In standby mode the output is resistive.

Theory of Operation

The TH7010 is a PLL frequency synthesizer intended for use in a frequency generation loop with a dual modulus prescaler and a VCO. The VCO frequency is divided by the external dual modulus prescaler. This divided signal is fed to the internal A and N counters. The reference frequency is fed to an internal R counter to define the channel spacing. Both frequencies are compared in the phase detector which drives the charge pump. A lock detect is provided to monitor the lock state of the loop. All blocks are programmed by a 3 wire interface.

The division ratio can be calculated as follows :

$$FVCO = (N \times P + A) / R \times FREF$$

FVCO : Output frequency of the external VCO

FREF : Reference oscillator frequency

N : divide ratio of the N counter $3 \le N \le 16380$

A : divide ratio of the A counter $0 \le A \le 127$

R : divide ratio of the R counter $3 \le R \le 65535$

P : divide ratio of the external dual modulus prescaler

The phase detector and charge pump

The phase detector is a digital edge sensitive comparator with UP and DOWN outputs. Both outputs can be monitored at the outputs PO1 and PO2. The phase detector drives a charge pump which is a switch with a tristate state. The output current can be programmed in 8 steps between 0.125 mA and 2 mA with a reference current of 100 µA.

If VFI < RFI, the charge pump delivers a positive current to the external loop filter.

If VFI > RFI, the charge pump sinks a negative current from the external loop filter.

The charge pump output can be inverted by software.

Anti-backlash pulses are generated to extend the very short phase difference between VFI and RFI.

Programming

The TH7010 can be programmed through a 3 wire interface. Four different words can be sent over this interface to program the internal registers. All four words have a 2 bit address part and a variable data part. When EN = L the data is transferred. It is loaded into the internal registers at the rising edge of EN. The last two bits which are transferred form the address bits. When EN = H, the input signals CLK and DATA are internally disabled.

The Status Register contains all status information.

The Reduced Status Register is a reduced version of the Status Register.

The N and A Counter Register and the R Counter Register contain the applicable counter values.

The programming of the device must start with the loading of the Status Register.

The N, A and R counters can be loaded synchronously or asynchronously. If synchronous loading is selected, all counters are loaded when they reach the value zero. As a result, the phase difference between the divided VFI and RFI signals remains the same.

For synchronous loading the following order of programming must be followed :

1. programming of synchronous loading using the Status Register
2. programming of the R counter
3. programming of the N/A counter. The rising edge of EN enables the synchronous loading of all counters at their zero value.

Standby

The TH7010 has two standby modes.

In standby mode 1, the whole device is powered down with the exception of the serial interface.

In standby mode 2, the serial interface and the input amplifiers are active. All other parts are powered down.

Internal Registers

R Counter Register																
1	1	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R134	R14	R15	R16
Note: R16 is the MSB of the R counter value. R16 is the first bit which is transferred to the TH7010.																	

N & A Counter Register																					
Dual Mode																					
0	1	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	A1	A2	A3	A4	A5	A6	A7
Single Mode																					
0	1	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14							
Note: N14 is the MSB of the N counter value; A7 is the MSB of the A counter value. A7 is the first bit which is transferred to the TH7010.																					

Reduced Status Register					
0	0	B14	B13	B12	B11
B11 is the first bit which is transferred to the TH7010.					

Output PD Phase Detector (pin 10)						
B14	B13	B12	Min.	Typ.	Max.	Unit
0	0	0	0.140	0.175	0.210	mA
0	0	1	0.200	0.250	0.300	mA
0	1	0	0.280	0.350	0.420	mA
0	1	1	0.400	0.500	0.600	mA
1	0	0	0.560	0.700	0.840	mA
1	0	1	0.800	1.000	1.200	mA
1	1	0	1.120	1.400	1.680	mA
1	1	1	1.600	2.000	2.400	mA
Stand By				0.1	50	nA
Note: These values are valid under the following conditions VDD = 4.5 ... 5.5 V, Vcp = 2.5 V, Iref = 100 µA.						

Anti Backlash Pulse Width					
B8	B7	Min.	Typ.	Max.	Unit
0	0	1.6	2	2.4	ns
0	1	3.2	4	4.8	ns
1	0	4.8	6	7.2	ns
1	1	8	10	12	ns
The above values are valid for VDD = 4.5 ... 5.5 V					
0	0	1.2	2	2.4	ns
0	1	2.4	4	5.6	ns
1	0	3.6	6	7.2	ns
1	1	8	10	12	ns
The above values are valid for VDD = 2.7 ... 3.3 V					
The best system performance is reached with the shortest ABL pulse					

Internal Registers

Status Register															
0	0	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
B1 is the first bit which is transferred to the TH7010.															

B11	Output bit PROBIT on PO1
0	0
1	1

B10	B9	Input amplifier modes
0	0	single mode
0	1	
1	0	dual mode, FI trigger edge LH
1	1	dual mode, FI trigger edge HL

B6	Stand By 2
0	device in power down, input amplifiers active
1	device active

B5	Stand By 1
0	device in power down
1	device active

B4	PD polarity
0	negative
1	positive
Note: Positive means increasing VCO frequency with increasing voltage.	

B3	B2	PO1	PO2	Modes
0	0	DRFIN	DRVIN	test mode
0	1	PHIV	PHIRN	external charge pump mode
1	0	PHIVN	PHIRN	external charge pump mode
1	1	PROBIT	Iref	internal charge pump mode

B1	Counter loading
0	asynchronous counter load
1	synchronous counter load

Operating Characteristics

Absolute Maximum Ratin gs						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage		- 0.3		7	V
Vin	Input Voltage		- 0.3		VCC + 3	V
Iin	Input Current		- 10		10	mA
TST	Storage Temperature Range		- 40		125	°C

Recommended Operating Conditions

Recommended o peratin g conditions						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage		2.7		5.5	V
Top	Operating Temperature Range		- 40		85	°C
Tj	Junction Temperature		- 10		150	°C

Current Consumption

Current Consum ption						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
Is	Current Consumption	VFI = 90 MHz, VRI = 10 MHz, Ipd = 0.25 mA			3.7	mA
Is	Current Consumption	Standby			10	µA

Characteristics

Inputs VFI VCO Fre quency Input (pin 8), RFI Reference Fre quency Input (pin 1)						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VFI	Input VCO Frequency					
	Dual Mode	VDD = 4.5 ...5.5 V VDD = 2.7 V	4 4		66 [1] 30 [1]	MHz MHz
	Single Mode	VDD = 4.5 ...5.5 V VDD = 2.7 V	4 4		100 [2] 100 [2]	MHz MHz
RFI	Input Reference Frequency	VDD = 4.5 V VDD = 2.7 V	4 4		60 [3] 30 [3]	MHz MHz
VFI	Input VCO Frequency	VDD = 2.7 ... 3.3 V	1		70	MHz
RFI	Input Reference Frequency	VDD = 2.7 ... 3.3 V	1		70	MHz
Vin	Input Voltage	f = 4 ... 70 MHz [4]	100			mVrms
Vin	Input Voltage	f = 4 ... 50 MHz [5]	100			mVrms
SR	Slew Rate	VDD = 2.7 V ... 5.5 V	4			V/µs
Ci	Input Capacitance				3	pF

Note: [1] @ 180 mV
Note: [2] @ 200 mV
Note: [3] @ 100 mV

Characteristics (Continued)

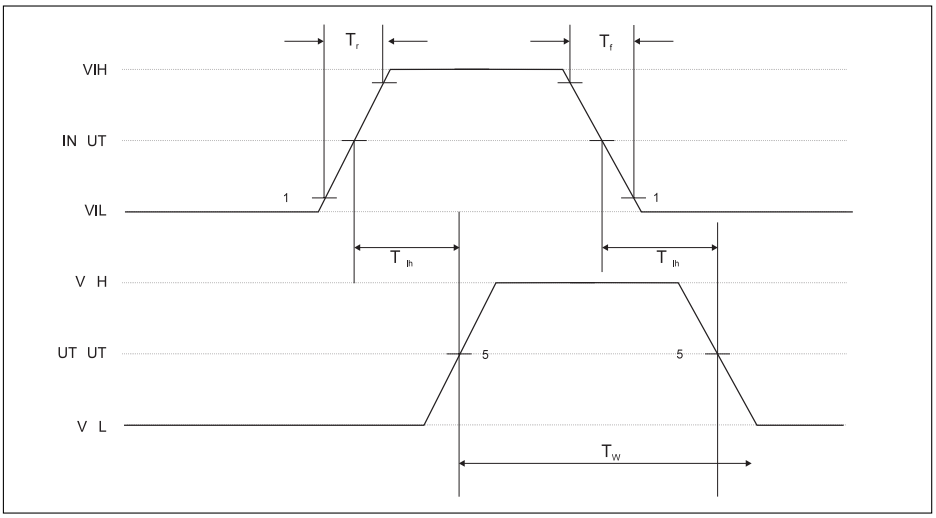
Output PD Phase Detector (pin 10)						
B14	B13	B12	Min.	Typ.	Max.	Unit
0	0	0	0.10	0.175	0.23	mA
0	0	1	0.14	0.250	0.33	mA
0	1	0	0.19	0.350	0.47	mA
0	1	1	0.27	0.500	0.66	mA
1	0	0	0.41	0.700	0.92	mA
1	0	1	0.57	1.000	1.32	mA
1	1	0	0.79	1.400	1.83	mA
1	1	1	1.13	2.000	2.6	mA
Standby				0.1	50	nA
Note: These values are valid under the following conditions VDD = 4.5 ... 5.5 V, Vcp = VDD/2, Iref = 100 µA.						

Output PO1 Programmable Output (pin 12)						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH	Voltage Output High	IOH = 2 mA [1]	VDD - 0.8			V
VOL	Voltage Output Low	IOH = 2 mA [1]			0.4	V
VOH	Voltage Output High	IOH = 1.2 mA [2]	VDD - 0.8			V
VOL	Voltage Output Low	IOH = 1.2 mA [2]			0.4	V
Tr	Rise Time	CL = 10 pF [1]		2.6	7.2	ns
Tf	Fall Time	CL = 10 pF [1]		3	4	ns
Tr	Rise Time	CL = 10 pF [2]		2.8	14.4	ns
Tf	Fall Time	CL = 10 pF [2]		4.5	6	ns
Note [1]: VDD = 4.5 ... 5.5 V Note [2]: VDD = 2.7 ... 3.3 V						

Characteristics (Continued)

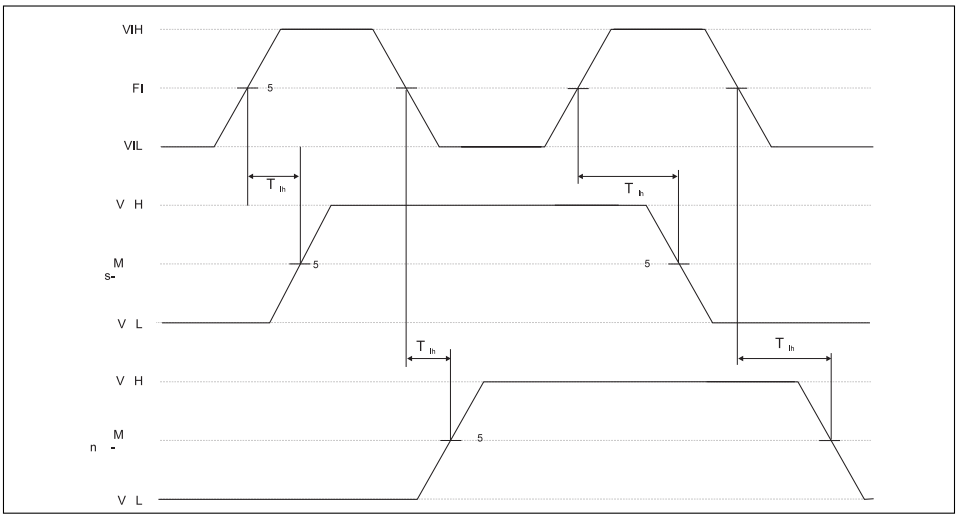
Input - Output PO2 Programmable Input - Output (pin 12)						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
INPUT						
VOH	Voltage Output High	IOH = 2 mA [1]	VDD - 0.8			V
VOL	Voltage Output Low	IOH = 2 mA [1]			0.4	V
VOH	Voltage Output High	IOH = 1.2 mA [2]	VDD - 0.8			V
VOL	Voltage Output Low	IOH = 1.2 mA [2]			0.4	V
Tr	Rise Time	CL = 10 pF [1]		2.6	7.2	ns
Tf	Fall Time	CL = 10 pF [1]		3	4	ns
Tr	Rise Time	CL = 10 pF [2]		2.8	14.4	ns
Tf	Fall Time	CL = 10 pF [2]		4.5	6	ns
OUTPUT						
Vref	Reference Voltage	Iref = 100 µA	0.8	1.2	1.3	V
Note [1]: VDD = 4.5 ... 5.5 V Note [2]: VDD = 2.7 ... 3.3 V						

Ouput LD Lock detect (pin 14)						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VOL	Voltage Output Low	IOL = 0.5 mA [1]			0.4	V
VOL	Voltage Output Low	IOL = 0.5 mA [2]			0.4	V
Tf	Fall Time	CL = 10 pF [1]		3.6	6	ns
Tf	Fall Time	CL = 10 pF [2]		4.5	10	ns
Note [1]: VDD = 4.5 ... 5.5 V Note [2]: VDD = 2.7 ... 3.3 V						



Characteristics (Continued)

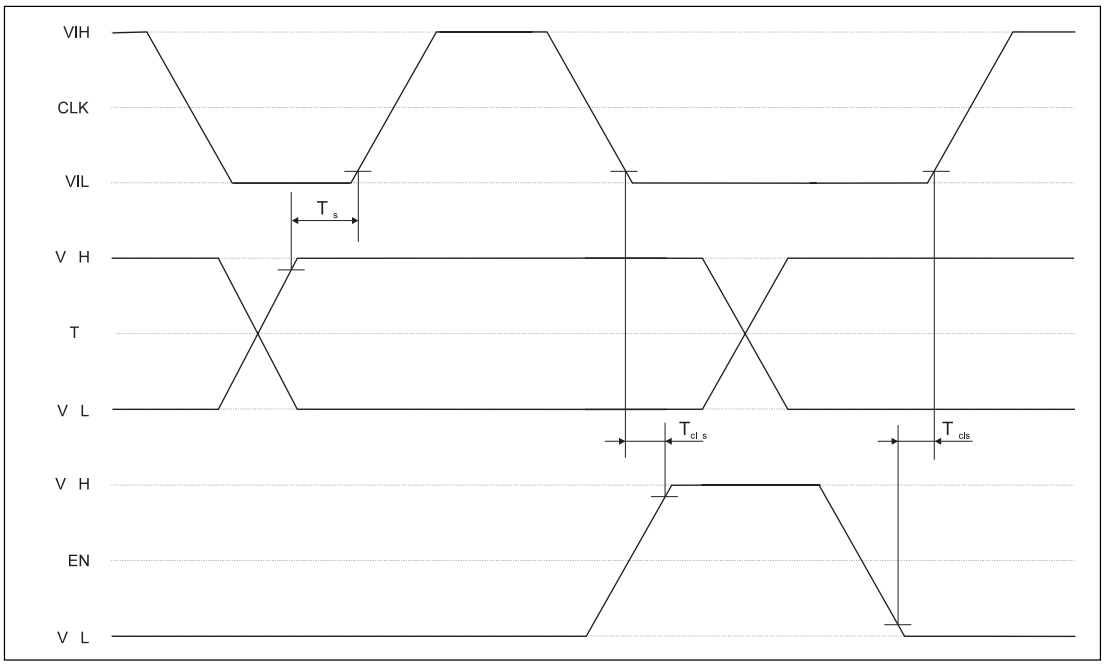
Output MOD Modulus Control Out put (pin 7)						
Sym	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH	Voltage Output High	IOH = - 0.5 mA [1]	VDD - 0.4			V
VOL	Voltage Output Low	IOH = - 0.5 mA [1]			0.4	V
VOH	Voltage Output High	IOH = - 0.3 mA [2]	VDD - 0.4			V
VOL	Voltage Output Low	IOH = - 0.3 mA [2]			0.4	V
Tr	Rise Time	CL = 10 pF [1]		2.6	18	ns
Tf	Fall Time	CL = 10 pF [1]		3	10	ns
Tr	Rise Time	CL = 10 pF [2]		2.8	30	ns
Tf	Fall Time	CL = 10 pF [2]		4.5	19	ns
Tphl	Propagation Delay Time H - L Transition MOD to VCI	CL = 5 pF [1]		10	12	ns
Tplh	Propagation Delay Time L - H Transition MOD to VCI	CL = 5 pF [1]		10	12	ns
Tphl	Propagation Delay Time H - L Transition MOD to VCI	CL = 5 pF [2]		19	22	ns
Tplh	Propagation Delay Time L - H Transition MOD to VCI	CL = 5 pF [2]		17	21	ns
Note [1]: VDD = 4.5 .. 5.5 V Note [2]: VDD = 2.7 .. 3.3 V						



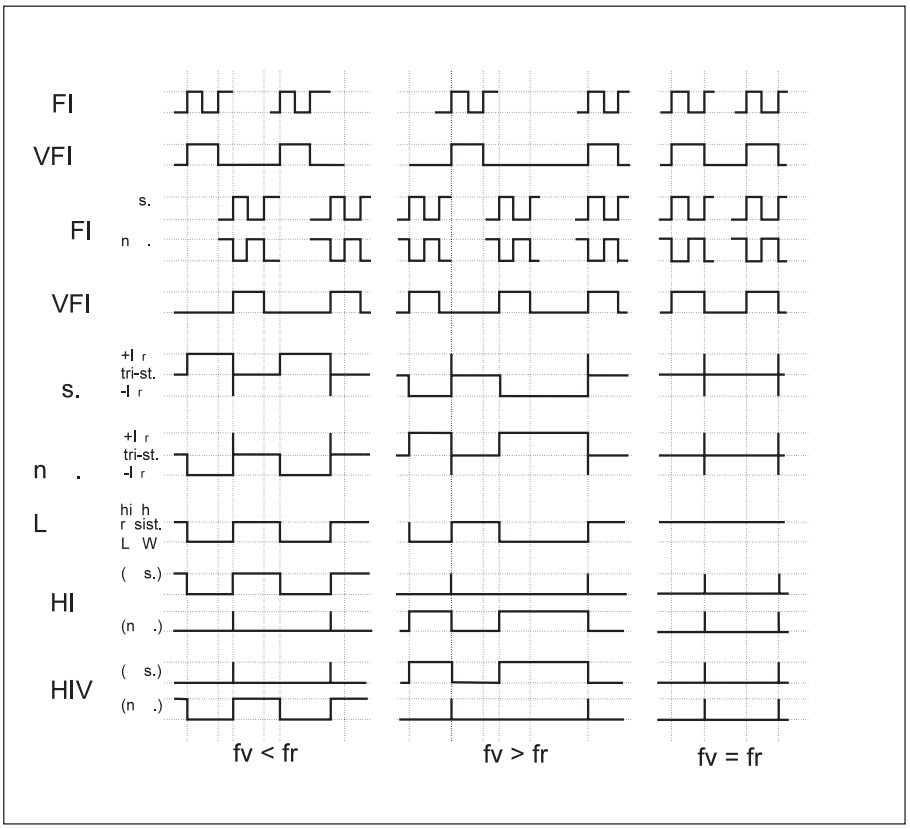
Characteristics (Continued)

Inputs EN (pin 3), Data (pin 4), CLK (pin 5)					
Sym	Parameter	Min.	Typ.	Max.	Unit
VIL	Voltage Input Low			1.5	V
VIL	Voltage Input Low			1.5	V
VIH	Voltage Input High	3.5			V
VIH	Voltage Input High	3.5			V
fclk	Clock Frequency			10	MHz
Tr	Rise Time CLK			1	µs
Tf	Fall Time CLK			1	µs
Tclw	CLK Pulse Width (high)	60			ns
Tds	DATA Setup time	20			ns
Tcles	CLK-Enable Setup Time	20			ns
Tecls	Enable-CLK Setup Time	20			ns
Tenw	EN Pulse Width (high)	60			ns
	Propagation Delay Time Enable - Port1		1		µs
Not : These values are valid under the following conditions: VDD = 2.7 .. .5.5 V					

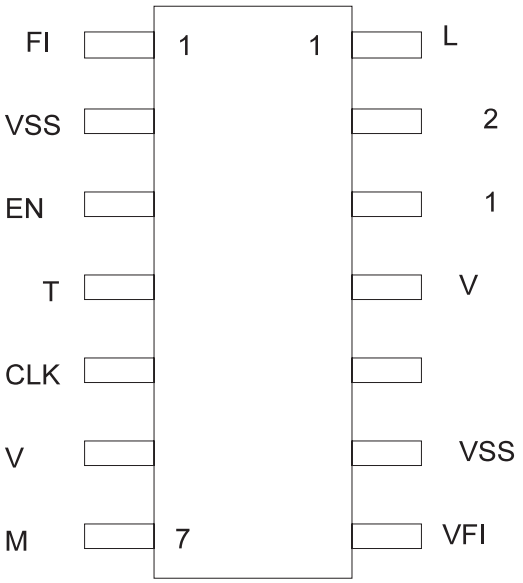
Standby Pin Overview						
	PO1		PO2	LD	PD	MOD
	PHIV	PHIVN				
Standby 1	low	high	high	high resistance	tristate	low
Standby 2	low	high	high	high resistance	tristate	low



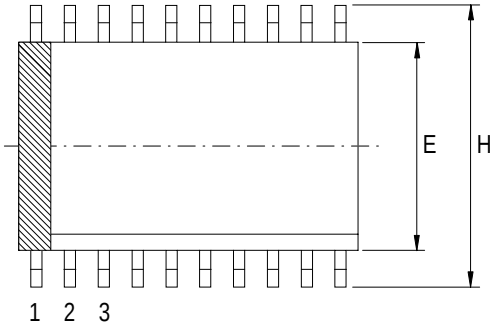
Phase detected output waveforms

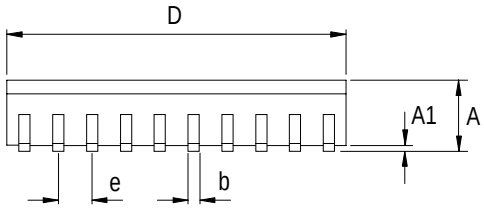


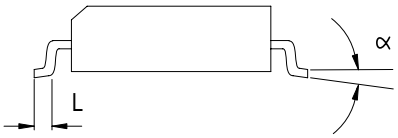
Pinout



Package







Package type		D	E	H	A	A 1	e	b	L	∝	Package code
SOP NB 14	min max	8,56 8,89	3,81 4,09	5,79 6,40	1,35 2,01	0,08 0,30	1,27	0,33 0,51	0,30 1,27	10 °	DC14

Ordering Information

The TH7010 PLL synthesizer is available in a standard 14-pin SOP package and for the operating range -40 °C...+85 °C (Industrial).

The order number is TH7010I (I=Industrial)

Important notice

This data sheet contains preliminary information on new products. The specifications are subject to change without notice.
Verify with your local Thesys Sales Office that you have the latest data sheet before finalizing a design.

Quality Data

Quality data is available on request. Contact:

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