



**LinearDimensions**  
SEMICONDUCTOR

## LND3842A/43A/44A/45A LND3842B/43B/44B/45B

### Current Mode PWM Controller

#### GENERAL DESCRIPTION

The LND3842B/43B/44B/45B and LND3842A/43A/44A/45A are fixed frequency current mode PWM controllers. They are specially designed for OFF-line and DC to DC converter applications with a minimal of external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator. Protection circuitry includes undervoltage lockout and current limiting.

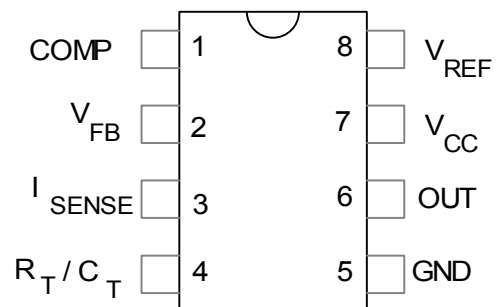
The LND3843B, A and LND3844B, A have UVLO thresholds of 16V(on) and 10 V (off). The corresponding thresholds for the LND3843B, A/45B,A are 8.4 V (on) and 7.6(off). The LND3842B, A and LND3843B, A can operate within 100% duty cycle. The LND3844B, A and LND3845B, A can operate within 50% duty cycle.

The LND384XB has Start-Up current of .45mA(typ).  
The LND384XA has Start-Up current of .17mA(typ).

#### FEATURES

- Low start-up and operating Current
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Operating Frequency up to 500KHZ

#### PIN CONFIGURATION

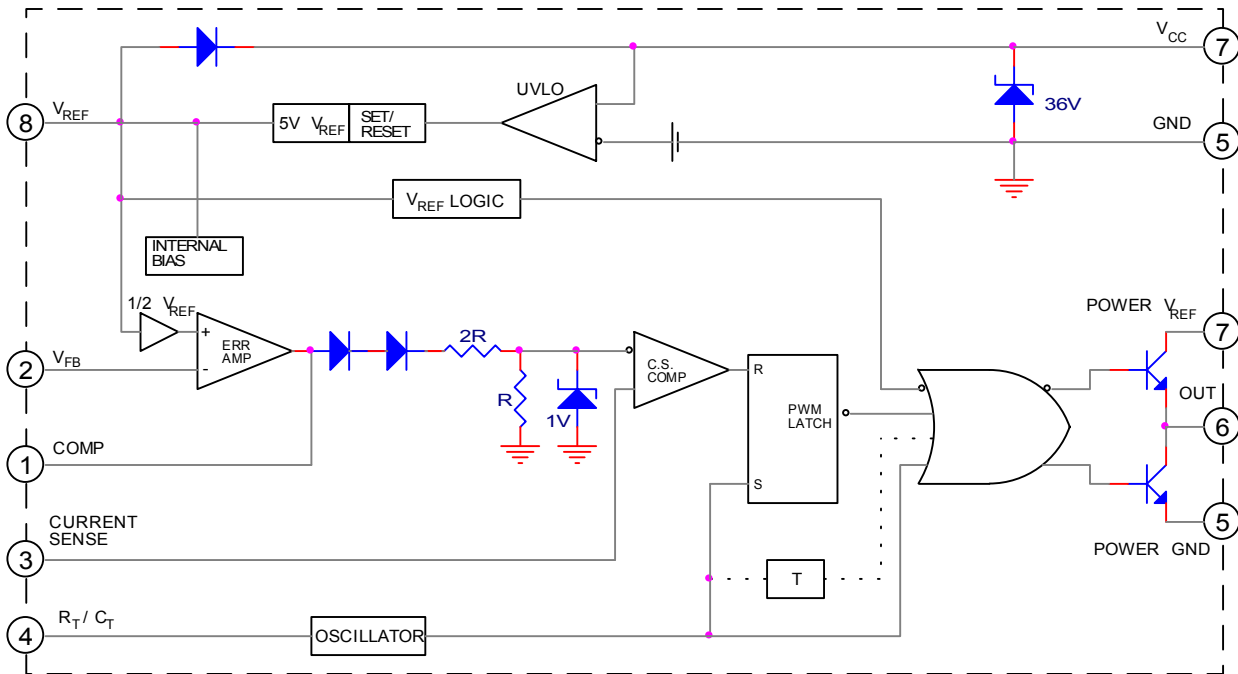




### ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Units
Supply voltage (low impedance source)	V <sub>CC</sub>	30	V
Output Current	I <sub>O</sub>	±1	A
Input Voltage (Analog Inputs pins 2,3)	V <sub>I</sub>	-0.3 to 5.5	V
Error Amp Output Sink Current	I <sub>SINK(E.A)</sub>	10	mA
Power Dissipation (T <sub>A</sub> =25°C)	P <sub>O</sub>	1	W
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Lead Temperature ( soldering 5 sec.)	T <sub>L</sub>	260	°C

### BLOCK DIAGRAM





## ELECTRICAL CHARACTERISTICS

(\*V<sub>CC</sub> =15 V, R<sub>T</sub>=10kΩ ,C<sub>T</sub>=3.3nF, T<sub>A</sub>=0 to 70° C, unless otherwise specified )

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Reference Section</b>						
Reference Output Voltage	V <sub>REF</sub>	T <sub>J</sub> =25°C, I <sub>REF</sub> =1mA	4.9	5.0	5.1	V
Line Regulation	ΔV <sub>REF</sub>	12V≤V <sub>CC</sub> ≤25V		6.0	20	mV
Load Regulation	ΔV <sub>REF</sub>	1mA≤I <sub>REF</sub> ≤20mA		6.0	25	
Short Circuit Output Current	I <sub>SC</sub>	T <sub>A</sub> =25°C		100	180	mA
<b>Oscillator Section</b>						
Oscillation Frequency	f	T <sub>J</sub> =25°C	47	52	57	KHz
Frequency change with Voltage	Δf/ΔV <sub>CC</sub>	12V≤V <sub>CC</sub> ≤25V		0.05	1.0	%
Oscillator Amplitude	V <sub>(OSC)</sub>	(Peak to Peak)		1.6		V
<b>Error Amplitude Section</b>						
Input Bias Current	I <sub>BIAS</sub>	V <sub>FB</sub> =3V		-0.1	-2	μA
Input Voltage	V <sub>I(E,A)</sub>	V <sub>pin1</sub> =2.5V		2.5	2.58	V
Open Loop Voltage Gain	A <sub>VOL</sub>	2V≤V <sub>O</sub> ≤4V	65	90		dB
Power Supply Rejection ratio	PSRR	12V≤V <sub>CC</sub> ≤25V	60	70		
Output Sink Current	I <sub>SINK</sub>	V <sub>pin2</sub> =2.7V, V <sub>pin1</sub> =1.1V	2	7		mA
Output Source current	I <sub>SOURCE</sub>	V <sub>pin2</sub> =2.3V, V <sub>pin1</sub> =5V	-0.5	-1.0		mA
High Output Voltage	V <sub>OH</sub>	V <sub>pin2</sub> =2.3V, R <sub>L</sub> =15kΩ to GND	5.0	6.0		V
Low Output Voltage	V <sub>OL</sub>	V <sub>pin2</sub> =2.7V, R <sub>L</sub> =15kΩ to PIN 8		0.8	1.1	
<b>Current Sense Section</b>						
Gain	G <sub>V</sub>	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	V <sub>I(MAX)</sub>	V <sub>pin1</sub> =5V(note 1)	0.9	1.0	1.1	V
Supply Voltage rejection	SVR	12V≤V <sub>CC</sub> ≤25V(note 1)		70		dB
Input Bias Current	I <sub>BIAS</sub>	V <sub>pin3</sub> = 3V		-3.0	-10	μA
<b>Output Section</b>						
Low Output Voltage	V <sub>OL</sub>	I <sub>sink</sub> =20mA		0.08	0.4	V
		I <sub>sink</sub> =200mA		1.4	2.2	
High Output Voltage	V <sub>OH</sub>	I <sub>sink</sub> =20mA	13	13.5		
		I <sub>sink</sub> =200mA	12	13.0		
Rise Time	t <sub>R</sub>	T <sub>J</sub> =25°C, C <sub>L</sub> =1nF(note 3)		45	150	nS
Fall time	t <sub>F</sub>	T <sub>J</sub> =25°C, C <sub>L</sub> =1nF(note 3)		35	150	nS
<b>Undervoltage Lockout Section</b>						
Start Threshold	V <sub>TH(ST)</sub>	LND3842A,B/44A,B	14.5	16.0	17.5	V
		LND3842A,B/45A,B	7.8	8.4	9.0	
Min. Operating Voltage (After Turn on)	V <sub>OPR(MIN)</sub>	LND3842A,B/44A,B	8.5	10	11.5	V
		LND3842A,B/45A,B	7.0	7.6	8.2	
<b>PWM Section</b>						
Max. Duty Cycle	D <sub>(MAX)</sub>	LND3842A,B/43A,B	95	97	100	%
		LND3842A,B/45A,B	47	48	50	
Min. Duty cycle	D <sub>(MAX)</sub>				0	
<b>Total Standby Current</b>						
Start-Up current	I <sub>ST</sub>	LND3842A/43A/44A/45A		0.17	0.3	mA
		LND3842B/43B/44B/45B		0.45	1	
Operating Supply Current	I <sub>CC(OPR)</sub>	V <sub>PIN3</sub> =V <sub>PIN2</sub> =0V		13	17	mA
Zener Voltage	V <sub>Z</sub>	I <sub>CC</sub> =25mA	30	38		V

\*Adjust V<sub>CC</sub> above the start threshold before setting it to 15V.



Note 1: Parameter measured at trip point of latch with  $V_{pin2}=0$

Note 2: Gain defined as  $A=\Delta V_{pin1}/\Delta V_{pin3}$  :  $0 \leq V_{pin3} \leq 0.8V$ .

Note 3: These parameters, although guaranteed, are not 100% tested in production.

## PIN DESCRIPTION

No	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation
2	$V_{FB}$	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	$I_{SENSE}$	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	$R_T/C_T$	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $R_T$ to $V_{ref}$ and capacitor $C_T$ to ground.
5	GROUND	This pin is the combined control circuitry and power ground
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	$V_{CC}$	This pin is the positive supply of the integrated circuit.
8	$V_{REF}$	This is the reference output. It provides charging current for capacitor $C_T$ through resistor $R_T$ .

## TYPICAL APPLICATIONS

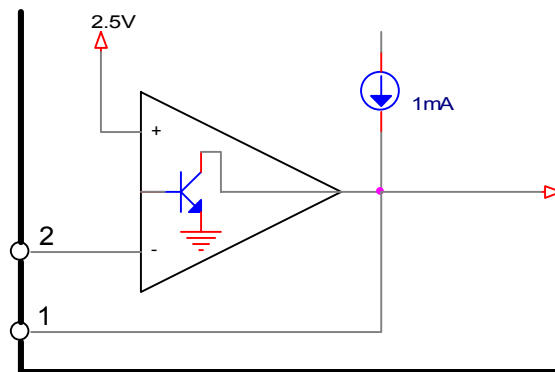


Figure 1. Error Amp Configuration

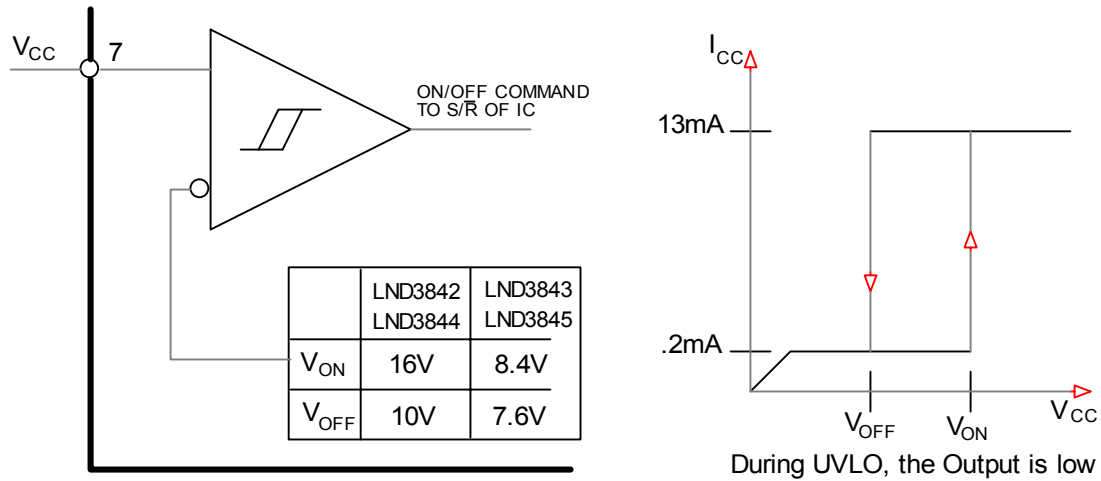


Figure 2. Undervoltage Lockout

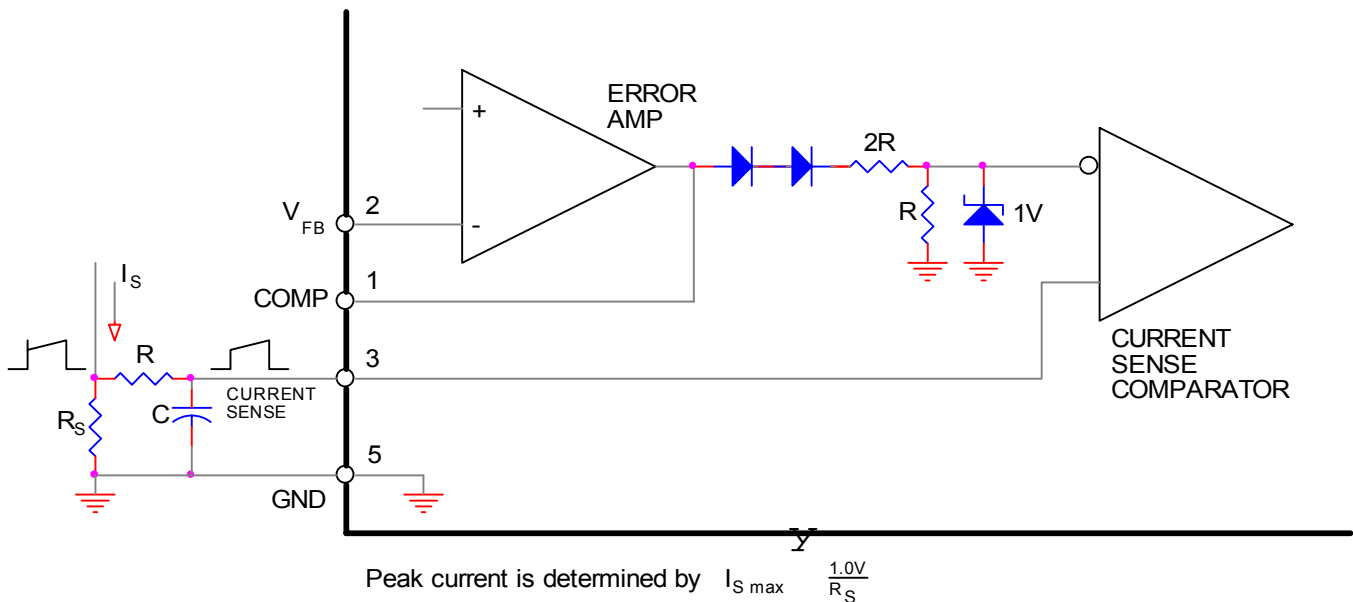


Figure 3. Current Sense Circuit

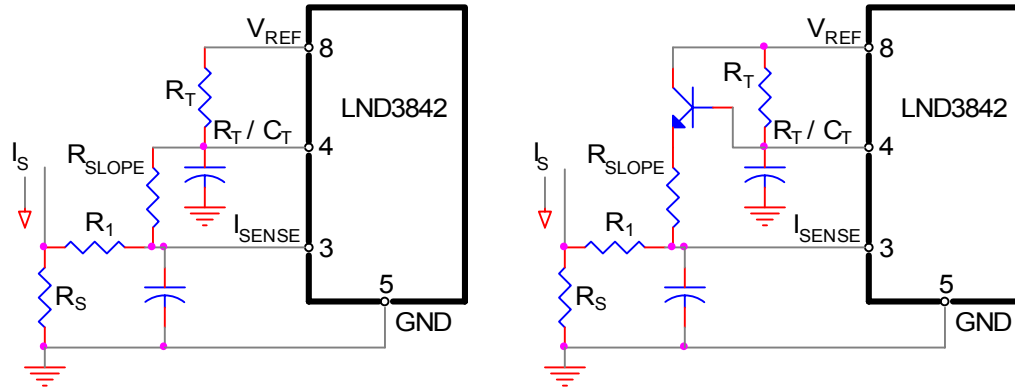
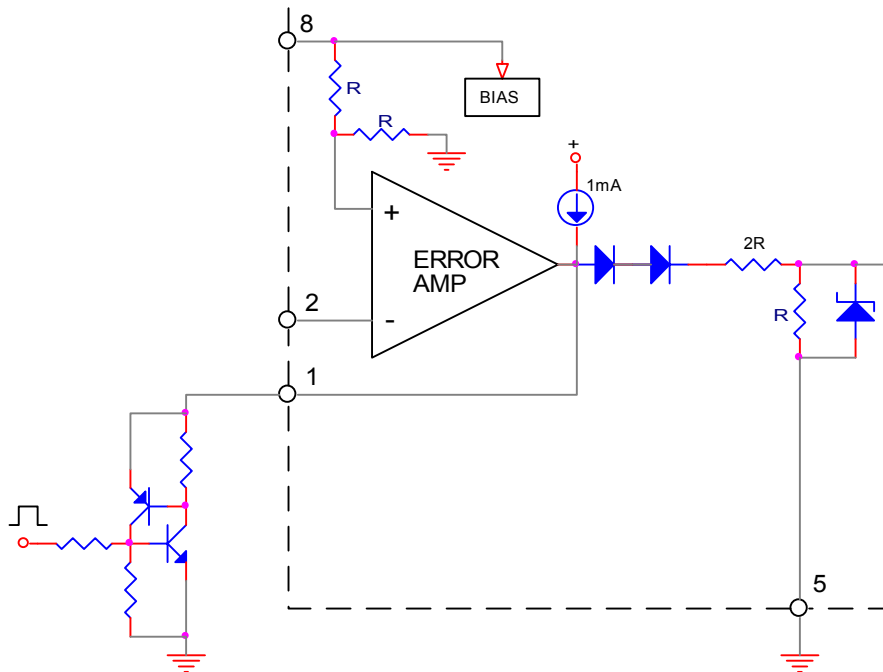
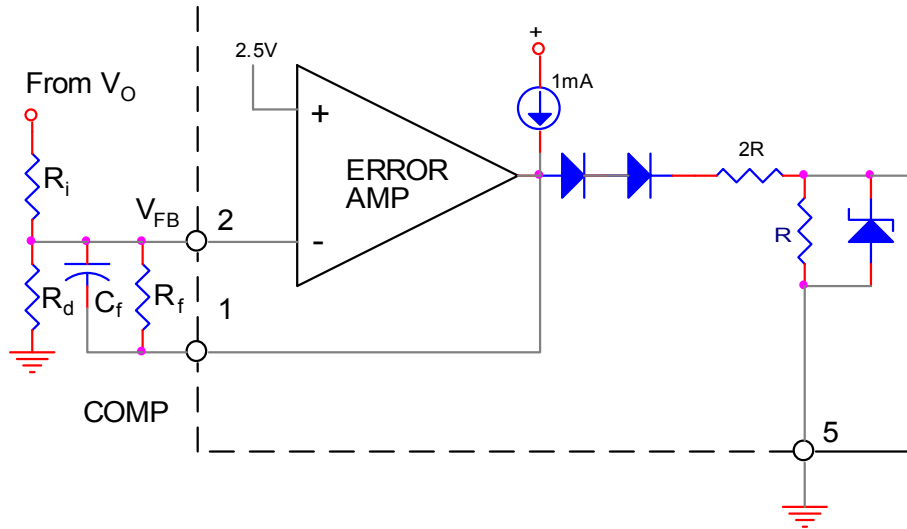


Figure 4. Slope Compensation Techniques

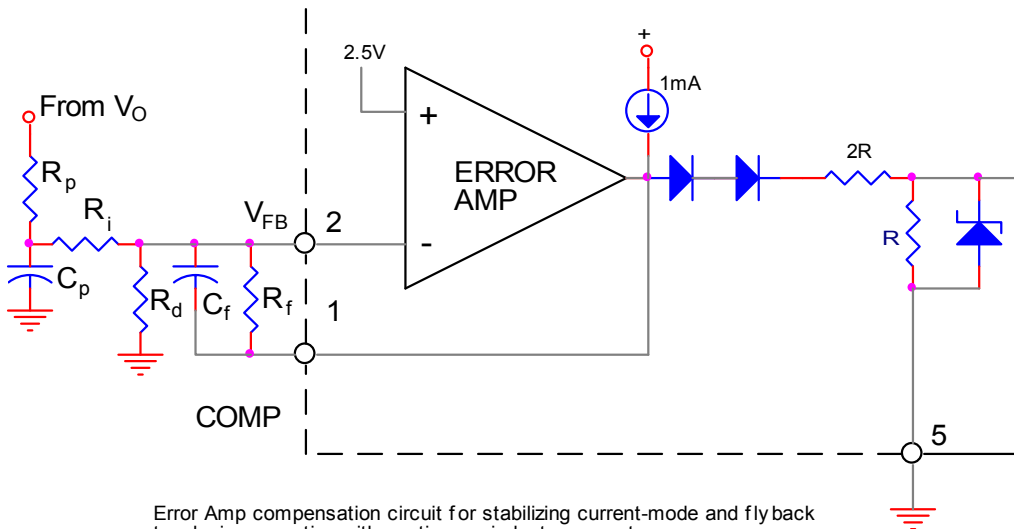


SCR must be selected for a holding current of less than 0.5 mA.  
A simple two transistor circuit can be used in place of the SCR  
as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode and fly back topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

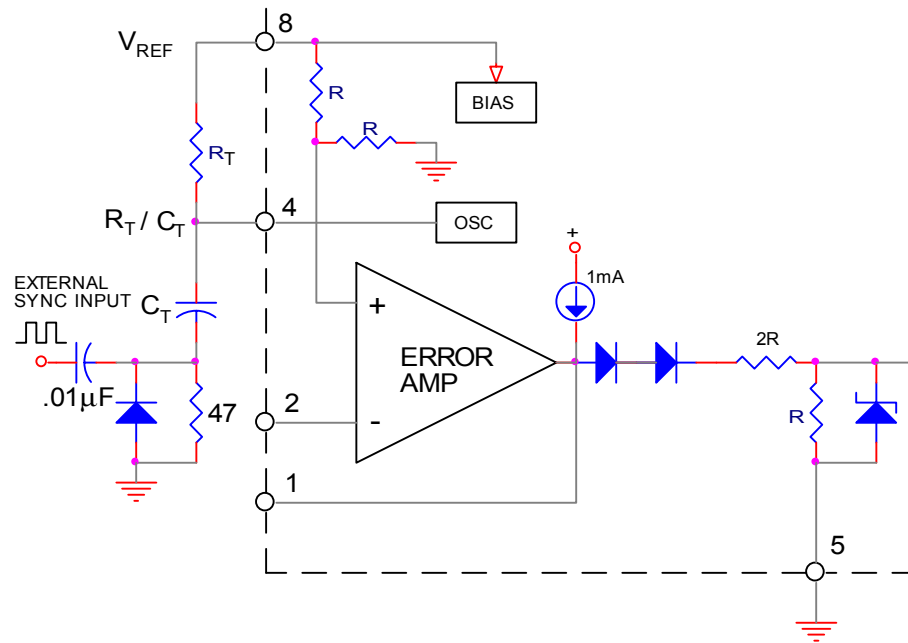


Figure 7. External Clock Synchronization

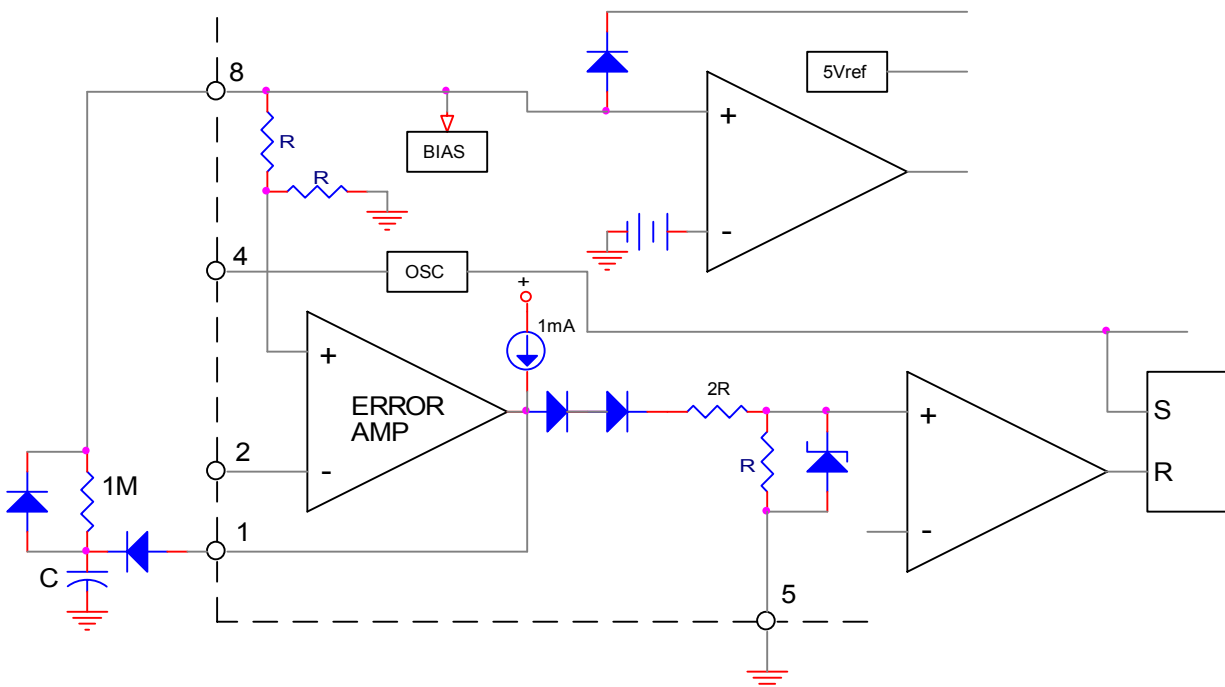


Figure 8. Soft-Start Circuit





### TYPICAL PERFORMANCE CHARACTERISTICS

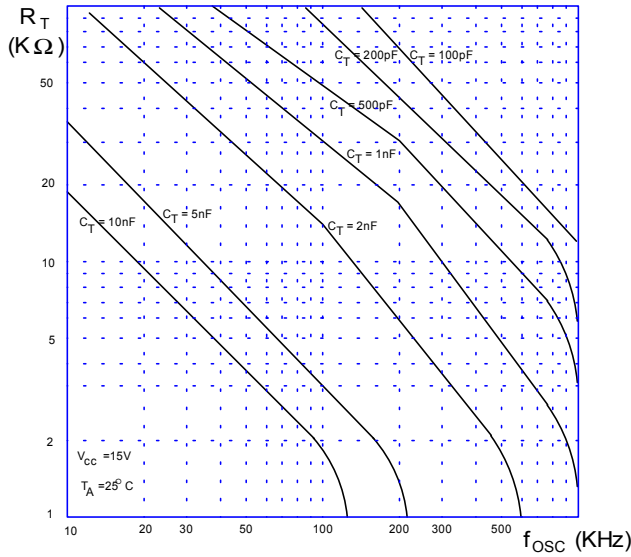


Figure 1. Timing Resistor vs. Oscillator Frequency

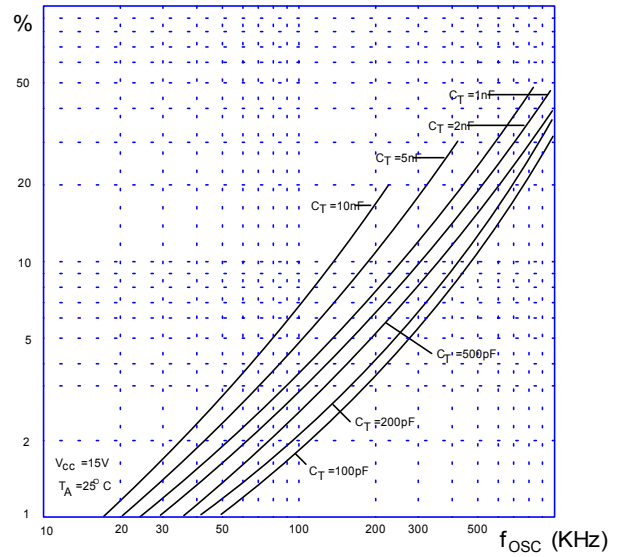


Figure 2. Output Dead-Time vs. Oscillator Frequency

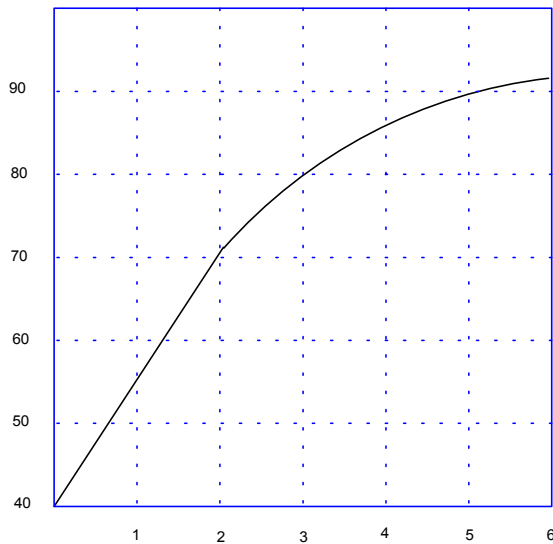


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor

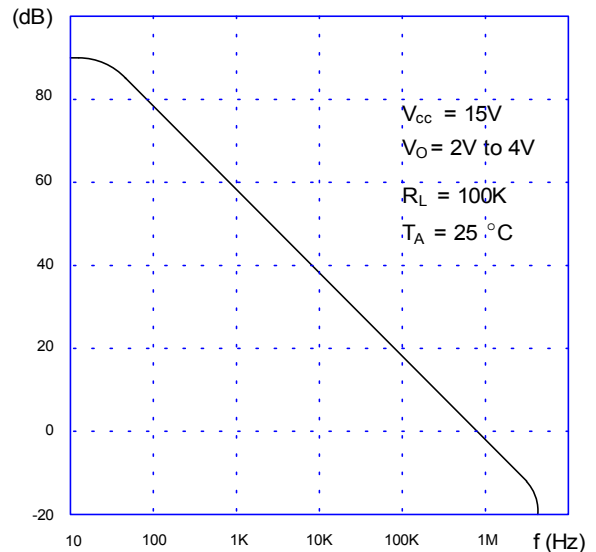


Figure 4. Error Amp Open-Loop Gain vs. Frequency

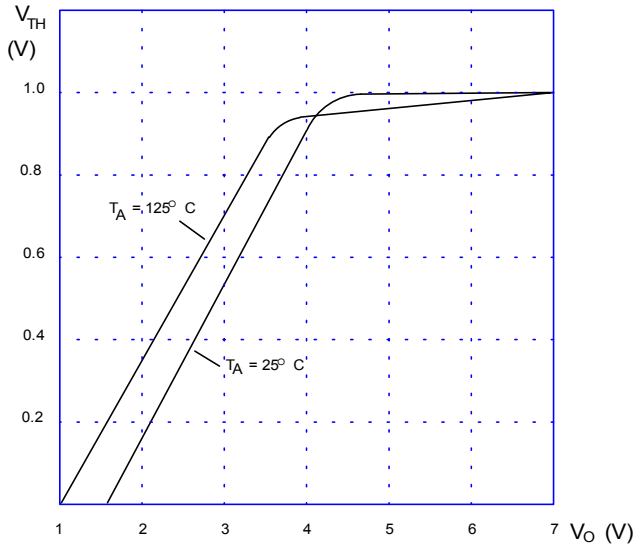


Figure 5. Current Sense Input Threshold vs. Output

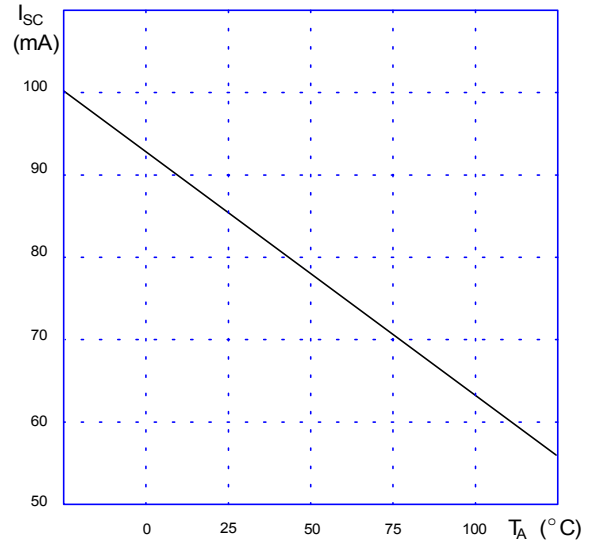


Figure 6. Reference Short Circuit Current vs. Temperature

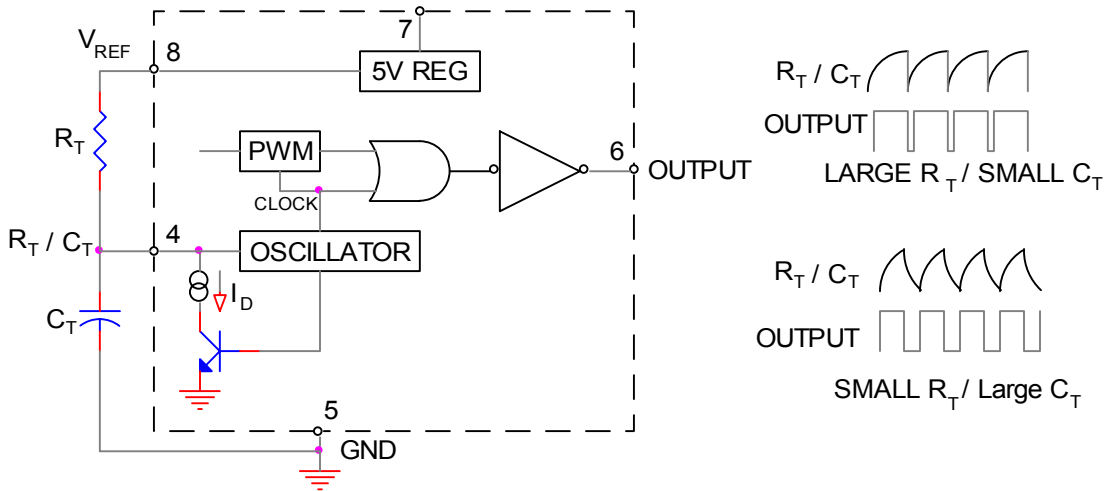


Figure 7. Oscillator and Output Waveforms