Dual, Matched Precision Operational Amplifier

FEATURES

- *Guaranteed* low offset voltage
  - LT1002A 60μV max
  - LT1002 100μV max
- *Guaranteed* offset voltage match
  - LT1002A 40μV max
  - LT1002 80μV max
- *Guaranteed* low drift
  - LT1002A 0.9μV/°C max
  - LT1002 1.3μV/°C max
- *Guaranteed* CMRR
  - LT1002A 110dB min
  - LT1002 110dB min
- *Guaranteed* channel separation
  - LT1002A 132dB min
  - LT1002 130dB min
- *Guaranteed* maching characteristics
- Low noise 0.35μV p-p

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low level signal processing
- Medical instrumentation
- Precision dual limit threshold detection
- Instrumentation amplifiers

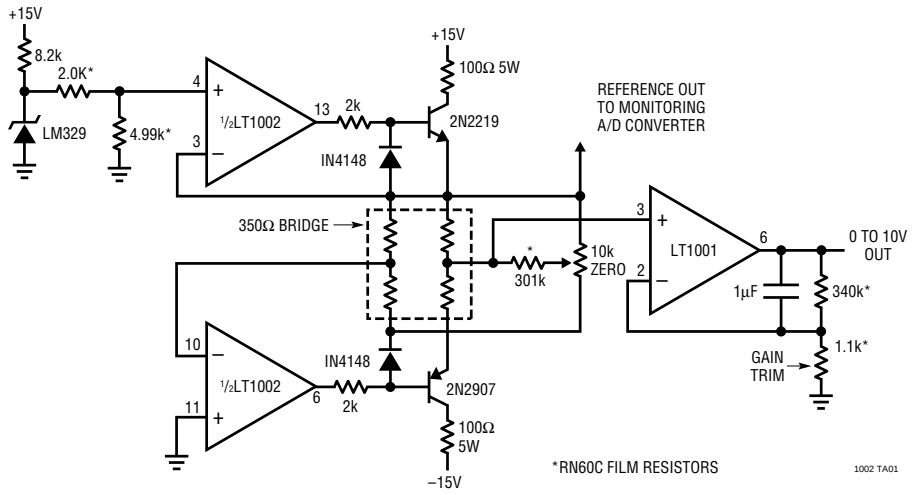
DESCRIPTION

The LT®1002 dual, matched precision operational amplifiers combine excellent individual amplifier performance with tight matching and temperature tracking between amplifiers.

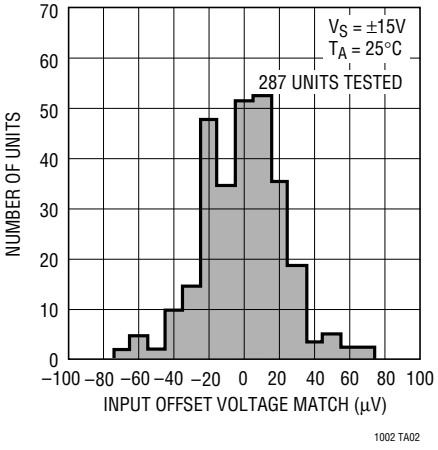
In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters and their matching. Consequently, the specifications of even the low cost commercial grade (the LT1002C) have been spectacularly improved compared to presently available devices.

Essentially, the input offset voltage of all units is less than 80μV, and matching between amplifiers is consistently beter than 60μV (see distribution plot below). Input bias and offset currents, channel separation, common mode and power suply rejections of the LT1002C are all specified at levels which were previsouly attainable only on very expensive, selected grades of other dual devices. Power dissipation is nearly halved compared to the most popular precision duals, without adversely affecting noise or speed performance. A by-product of lower dissipation is decreased warm-up drift. For even better performance in a single precision op amp, refer to the LT1001 data sheet. A bridge signal conditioning application is shown below. This circuit illustrates the requirement for both excellent matching and individual amplifier specifications.

Strain Gauge Signal Conditioner with Bridge Excitation



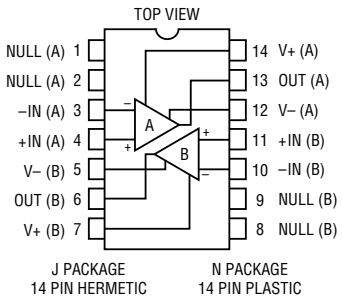
Distribution of Offset Voltage Match



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 6) ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1002AM/LT1002M ..... –55°C to 125°C
LT1002AC/LT1002C ..... 0°C to 70°C
Storage Temperature Range
All Grades ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
14 PIN HERMETIC

N PACKAGE
14 PIN PLASTIC

NOTE: Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B. (Note 6)

ORDER PART NO.	OFFSET VOLTAGE MAX at 25°C
LT1002AMJ	60µV
LT1002MJ	100µV
LT1002ACJ	60µV
LT1002CJ	100µV
LT1002ACN	60µV
LT1002CN	100µV

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

V_S = ±15V, T_A = 25°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/LT1002AC MIN	LT1002AM/LT1002AC TYP	LT1002AM/LT1002AC MAX	LT1002M/LT1002C MIN	LT1002M/LT1002C TYP	LT1002M/LT1002C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1		20	60		25	100	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.3	1.5		0.4	2.0	µV/month
I_{OS}	Input Offset Current			0.3	2.8		0.4	4.2	nA
I_B	Input Bias Current			±0.6	±3.0		±0.7	±4.5	nA
$\overline{e}_n$	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.7		0.38	0.75	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10Hz (Note 5) f_O = 1000Hz (Note 2)		10.3 9.6	20.0 11.5		10.5 9.8	20.0 12.0	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±12V $R_L \geq 1k\Omega$, V_O = ±10V	400 250	800 500		350 220	800 500		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	108	123		105	123		dB
R_{in}	Input Resistance Differential Mode	Note 4	20	100		13	80		MΩ
	Input Voltage Range		±13	±14		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13 ±12	±14 ±13.5		±13 ±12	±14 ±13.5		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/µs
GBW	Gain Bandwidth Product	Note 4	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation per amplifier	No load No load, V_S = ±3V		46 4	75 7		48 4	85 8	mW

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

$V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1002AM MIN	LT1002AM TYP	LT1002AM MAX	LT1002M MIN	LT1002M TYP	LT1002M MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1	●		30	150		45	230	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.2	0.9		0.3	1.3	µV/°C
I_{OS}	Input Offset Current		●		0.8	5.6		1.2	8.5	nA
I_B	Input Bias Current		●		±1.0	±6.0		±1.5	±9.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	122		104	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	102	117		96	117		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation per amplifier	No load	●		55	90		60	100	mW

$V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1002AC MIN	LT1002AC TYP	LT1002AC MAX	LT1002C MIN	LT1002C TYP	LT1002C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1	●		20	100		30	160	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.2	0.9		0.3	1.3	µV/°C
I_{OS}	Input Offset Current		●		0.5	4.2		0.6	5.7	nA
I_B	Input Bias Current		●		±0.7	±4.5		±1.0	±6.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	108	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	105	120		100	120		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.8		±12.5	±13.8		V
P_d	Power Dissipation per amplifier	No Load	●		50	85		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage measured with high speed test equipment, approximately 1second after power is applied.

Note 2: This parameter is tested on a sample basis only.

Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV.

Note 4: Parameter is guaranteed by design.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 6: The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V– supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V– pins should be used.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/AC MIN	LT1002AM/AC TYP	LT1002AM/AC MAX	LT1002M/C MIN	LT1002M/C TYP	LT1002M/C MAX	UNITS
	Input Offset Voltage Match		–	15	40	–	25	80	µV
I_B^+	Average Non-Inverting Bias Current		–	±0.6	±3.5	–	±0.7	±4.8	nA
I_{OS}^+	Non-Inverting Offset Current		–	0.6	3.5	–	0.7	6.0	nA
I_{OS}^-	Inverting Offset Current		–	0.6	3.5	–	0.7	6.0	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	110	132	–	108	132	–	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	108	130	–	102	128	–	dB
	Channel Seperation	f ≤ 10Hz (Note 4)	132	148	–	130	146	–	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted

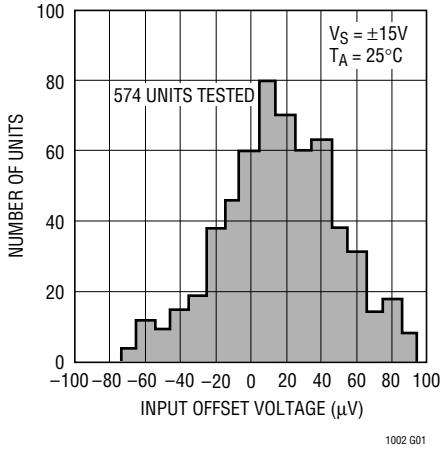
SYMBOL	PARAMETER	CONDITIONS		LT1002AM MIN	LT1002AM TYP	LT1002AM MAX	LT1002M MIN	LT1002M TYP	LT1002M MAX	UNITS
	Input Offset Voltage Match		●	–	50	140	–	60	230	µV
	Input Offset Voltage Tracking		●	–	0.3	1.0	–	0.4	1.5	µV/°C
I_B^+	Average Non-Inverting Bias Current		●	–	±1.5	±6.0	–	±1.8	±10.0	nA
I_{OS}^+	Non-Inverting Offset Current		●	–	1.5	6.5	–	1.8	12.0	nA
I_{OS}^-	Inverting Offset Current		●	–	1.5	6.5	–	1.8	12.0	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	106	126		102	124	–	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	102	122		94	120	–	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted

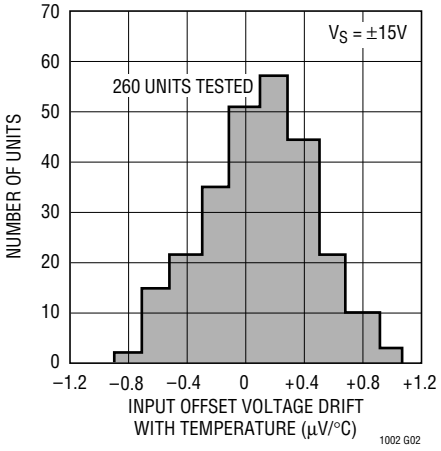
SYMBOL	PARAMETER	CONDITIONS		LT1002AC MIN	LT1002AC TYP	LT1002AC MAX	LT1002C MIN	LT1002C TYP	LT1002C MAX	UNITS
	Input Offset Voltage Match		●	–	30	85	–	45	150	µV
	Input Offset Voltage Tracking		●	–	0.3	1.0	–	0.4	1.5	µV/°C
I_B^+	Average Non-Inverting Bias Current		●	–	±1.0	±4.5	–	±1.2	±7.0	nA
I_{OS}^+	Non-Inverting Offset Current		●	–	1.0	5.0	–	1.2	8.5	nA
I_{OS}^-	Inverting Offset Current		●	–	1.0	5.0	–	1.2	8.5	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	108	130	–	105	128	–	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	105	126	–	98	124	–	dB

TYPICAL PERFORMANCE CHARACTERISTICS

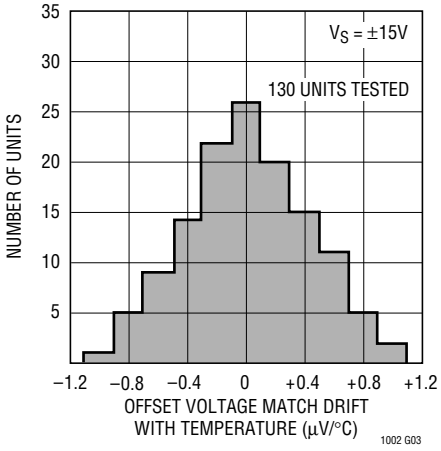
Distribution of Offset Voltage of Individual Amplifiers



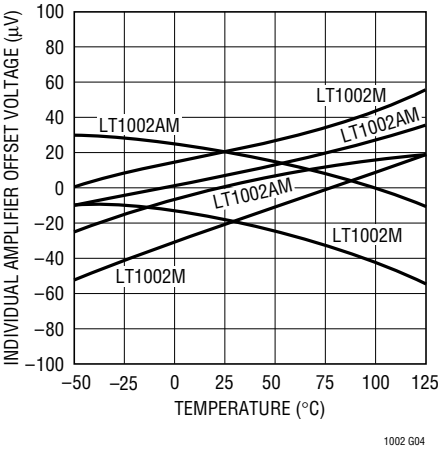
Distribution of Offset Voltage Drift with Temperature (Individual Amplifiers)



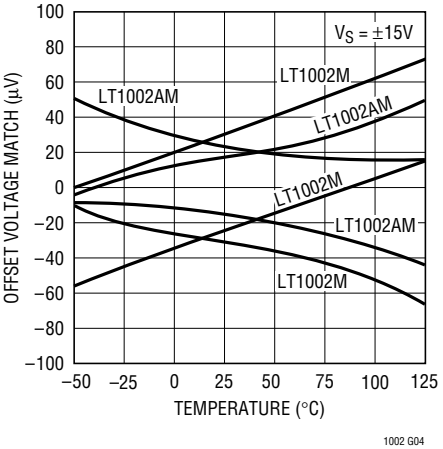
Distribution of Offset Voltage Match Drift with Temperature



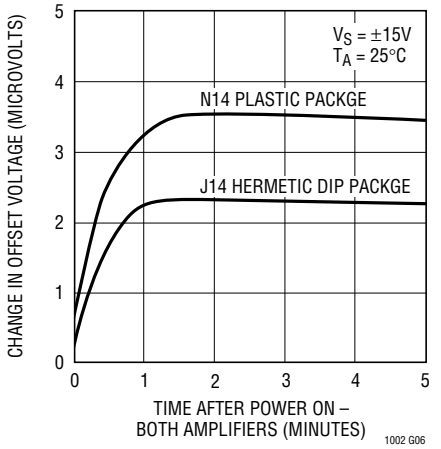
Offset Voltage Drift with Temperature of Six Representative Units



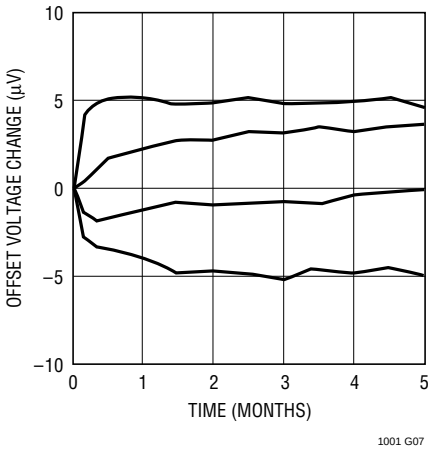
Offset Voltage Tracking with Temperature of Six Representative Units



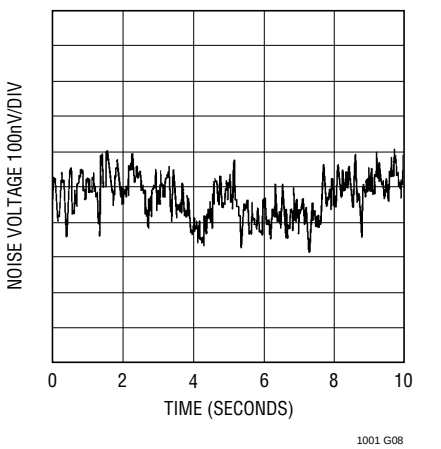
Warm-Up Drift



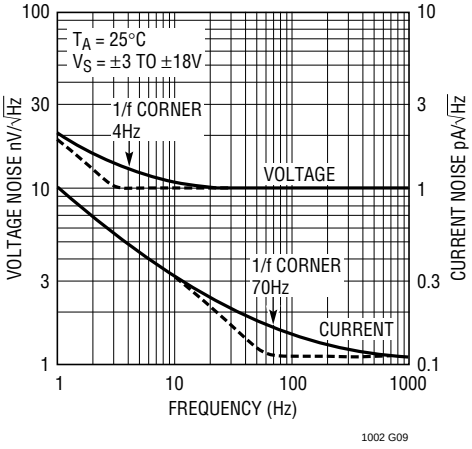
Long Term Stability of Four Representative Units



0.1Hz to 10Hz Noise

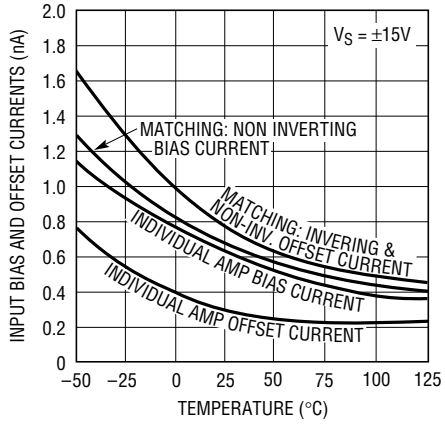


Noise Spectrum

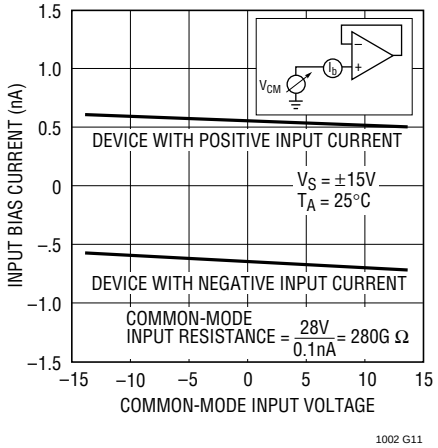


TYPICAL PERFORMANCE CHARACTERISTICS

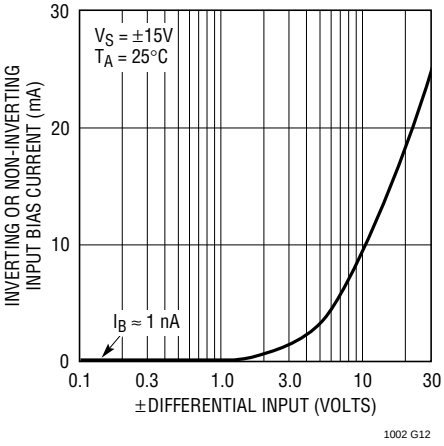
Matching and Individual Amplifier Bias and Offset Currents vs Temperature



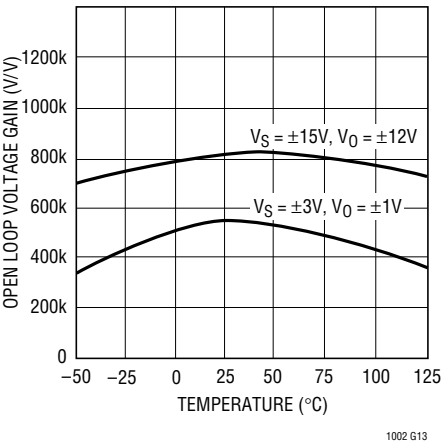
Input Bias Current Over the Common Mode Range



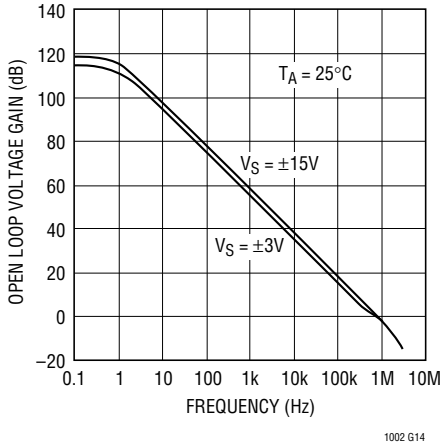
Input Bias Current vs. Differential Input Voltage



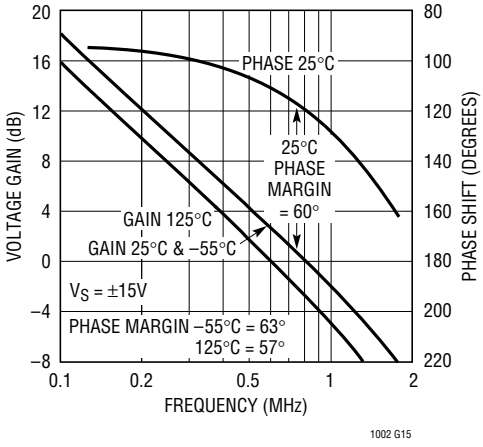
Open Loop Voltage Gain vs Temperature



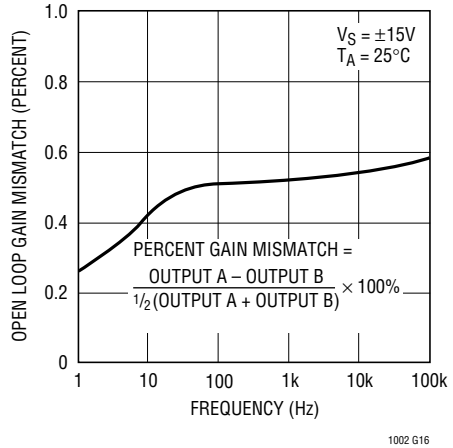
Open Loop Voltage Gain Frequency Response



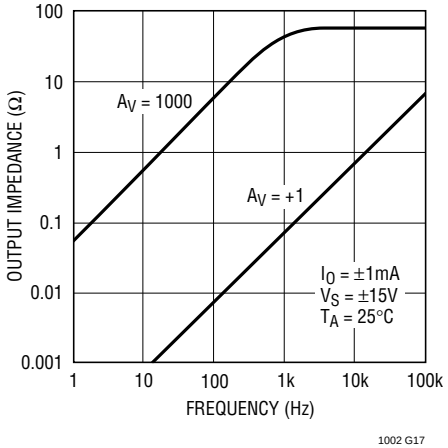
Gain, Phase Shift vs. Frequency



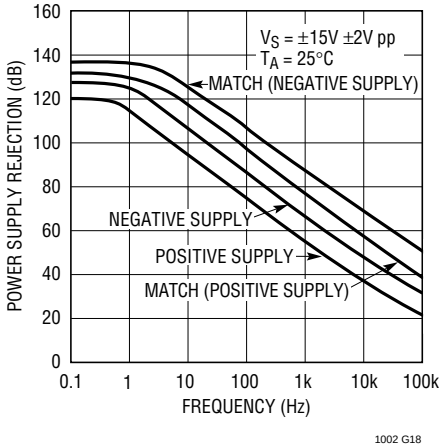
Open Loop Gain Mismatch vs Frequency



Closed Loop Output Impedance

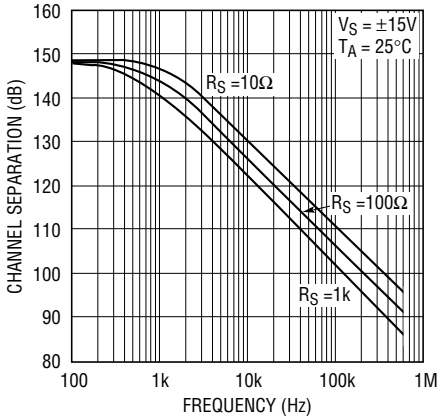


Power Supply Rejection and PSRR Match vs Frequency



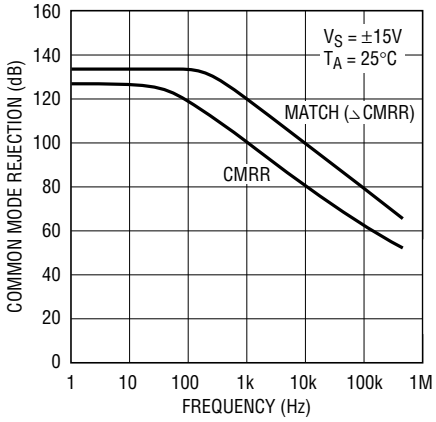
TYPICAL PERFORMANCE CHARACTERISTICS

Channel Separation vs Frequency



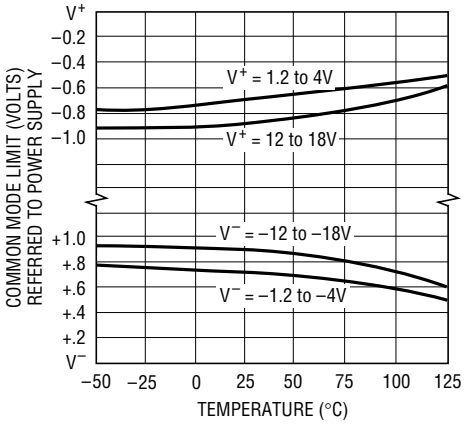
1002 G19

Common Mode Rejection and CMRR Match vs Frequency



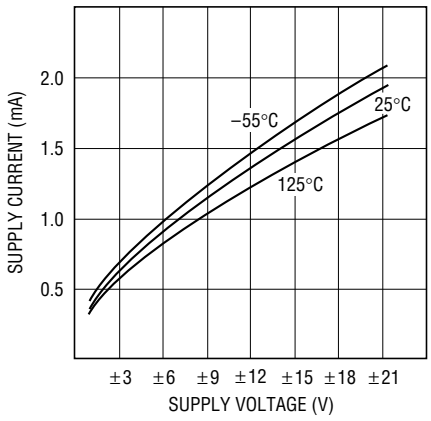
1002 G20

Common Mode Limit vs Temperature



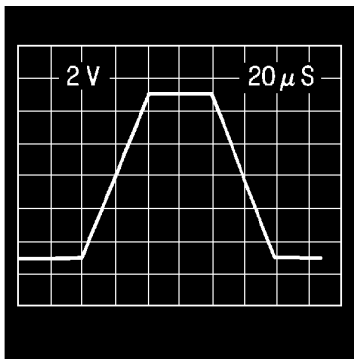
1002 G21

Supply Churrent vs. Supply Voltage For Each Amplifier



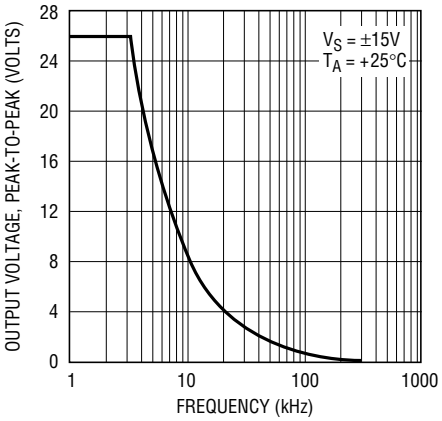
1002 G22

Large Signal Transient Response



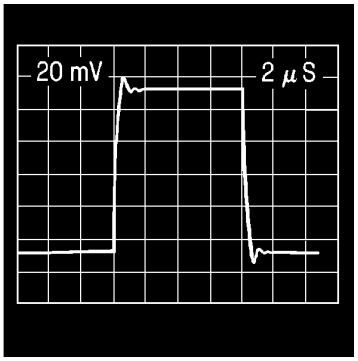
1002 G23

Maximum Undistorted Output vs. Frequency



1002 G24

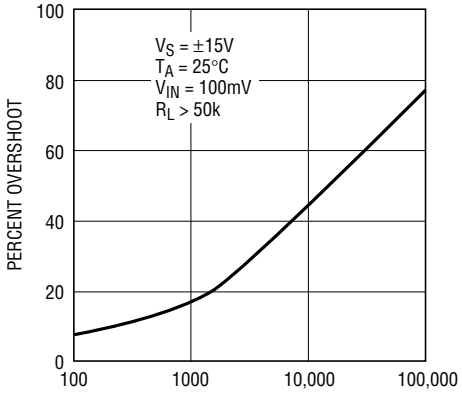
Small Signal Transient Response



A_V = +1, C_L = 50pF

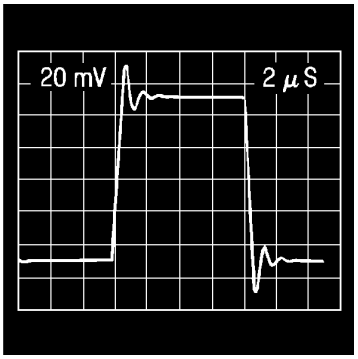
1002 G25

Voltage Follower Overshoot vs Capacitive Load



1002 G26

Small Signal Transient Response

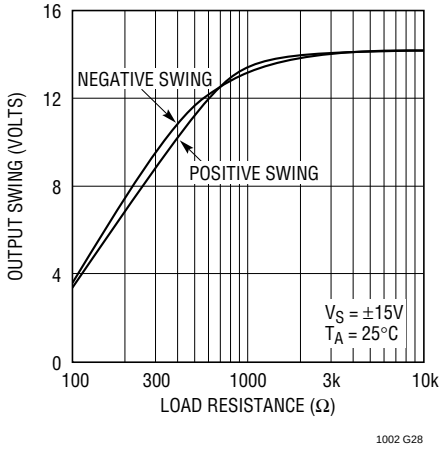


A_V = +1, C_L = 1000pF

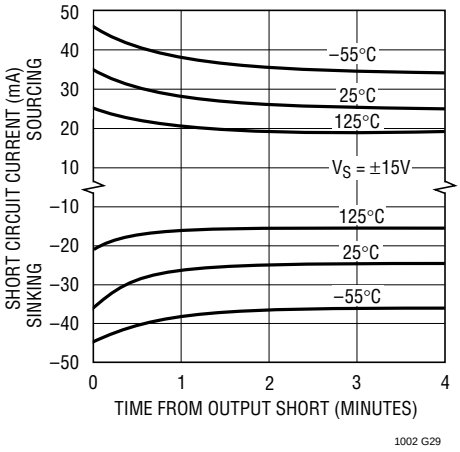
1002 G27

TYPICAL PERFORMANCE CHARACTERISTICS

Output Swing vs. Load Resistance



Output Short Circuit Current vs Time



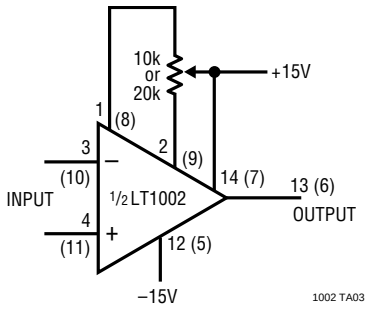
APPLICATIONS INFORMATION

The LT1002 dual amplifier may be inserted directly into OP-10, OP207, OP227 sockets with or without removal of external nulling potentiometers.

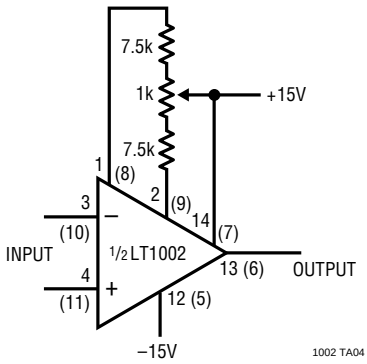
Offset Voltage Adjustment The input offset voltage of the LT1002, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300)μV/°C, e.g. if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C. The adjustment range with a 10k or 20k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of ±100μV.

In matching applications, both amplifiers can be trimmed to zero, or the offset of one amplifier can be trimmed to match the offset of the other. Offset adjustment, however, slightly degrades the gain, common-mode and power-supply rejection match between the two op amps. Fortunately, the guaranteed offset voltage match of the LT1002 is very low, in most applications offset adjustment will be unnecessary.

Standard Adjustment

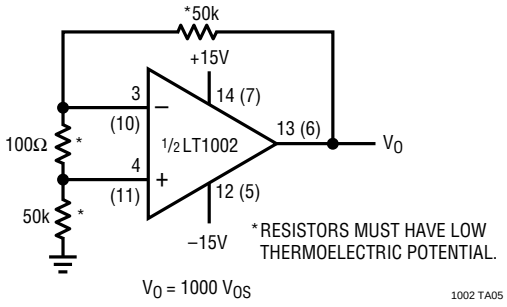


Improved Sensitivity Adjustment

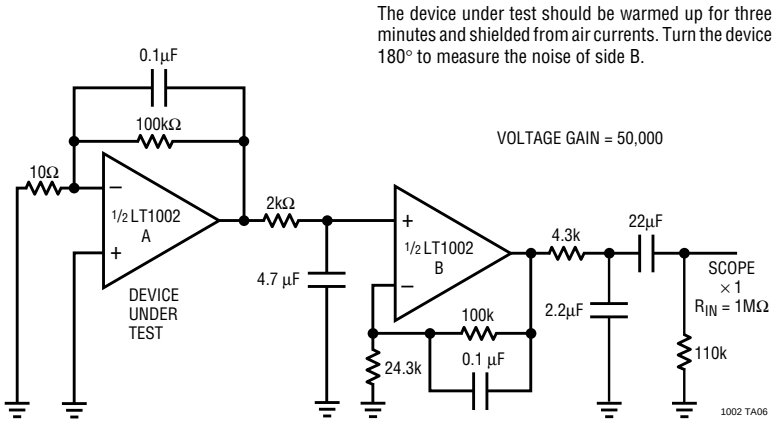


APPLICATIONS INFORMATION

Test Circuit for Offset Voltage and its Drift with Temperature



0.1Hz to 10Hz Noise Test Circuit



(Peak to Peak noise measured in 10 Sec interval)

This circuit is also used as burn-in configuration for the LT1002, with supply voltages increased to ±20V.

Unless proper care is exercised, thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents should be minimized, package leads should be short, the two input leads should be as close together as possible and maintained at the same temperature.

Channel Separation

This parameter is defined as the ratio of the change in input offset voltage of one amplifier to the change in output voltage of the other amplifier causing the offset change.

At low frequencies the LT1002's channel separation is an almost unmeasurable 148dB. As frequency increases, pin to pin capacitance of the package, between the output of one amplifier and the inputs of the other, becomes dominant. Since these pins are non-adjacent, the capacitance is only 0.02pF. To maintain the LT1002's excellent channel separation at higher frequencies, the socket and PC board capacitances should be minimized.

Power supplies

The LT1002 is specified over a wide range of power supply voltages from ±3V to ±18V. Operation with lower supplies is possible, down to ±1.2V (two Ni-Cad batteries). However, with ±1.2V supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V– supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V– pins should be used.

APPLICATIONS INFORMATION

Advantages of Matched Dual Op Amps In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

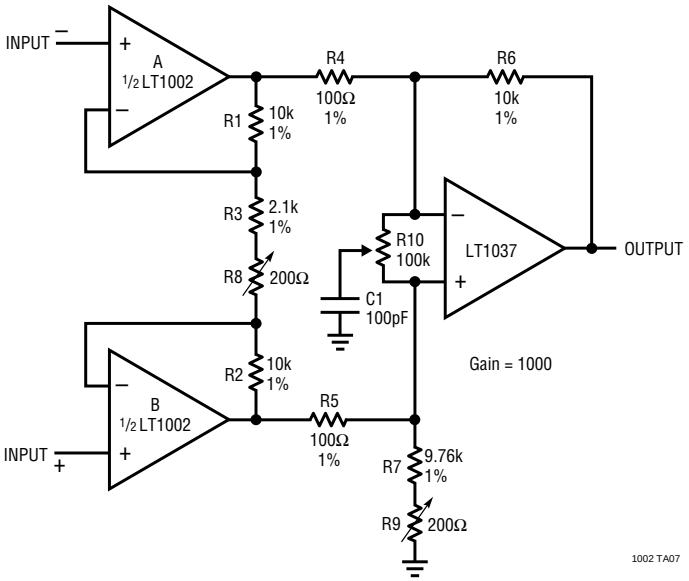
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1002. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS}^-) will cause errors flowing through R1, R2, and R3. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB,
and $CMRR_B = +0.75\mu V/V$ or 122.5dB,
then $\Delta CMRR = 0.25\mu V/V$ or 132dB;
if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB,
then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly, the LT1002, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



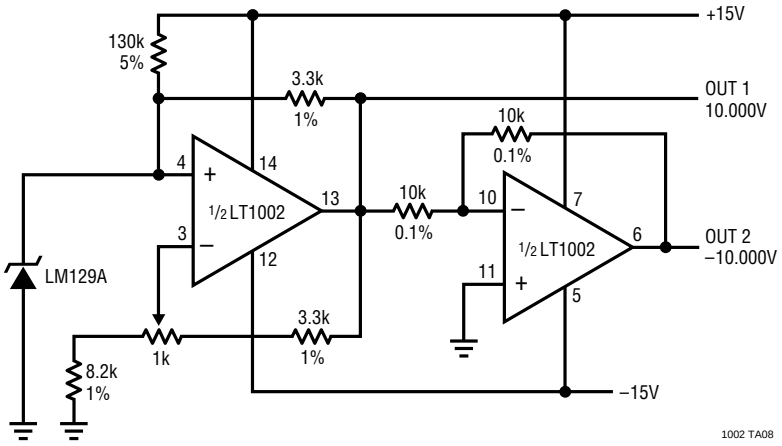
Trim R8 for gain
Trim R9 for DC common mode rejection
Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifier:

Input offset voltage = 25μV
Input bias current = 0.7nA
Input resistance = 200 GΩ
Input offset current = 0.6nA
Input noise = 0.5μV p-p
Power bandwidth ($V_O = \pm 10V$) = 80kHz

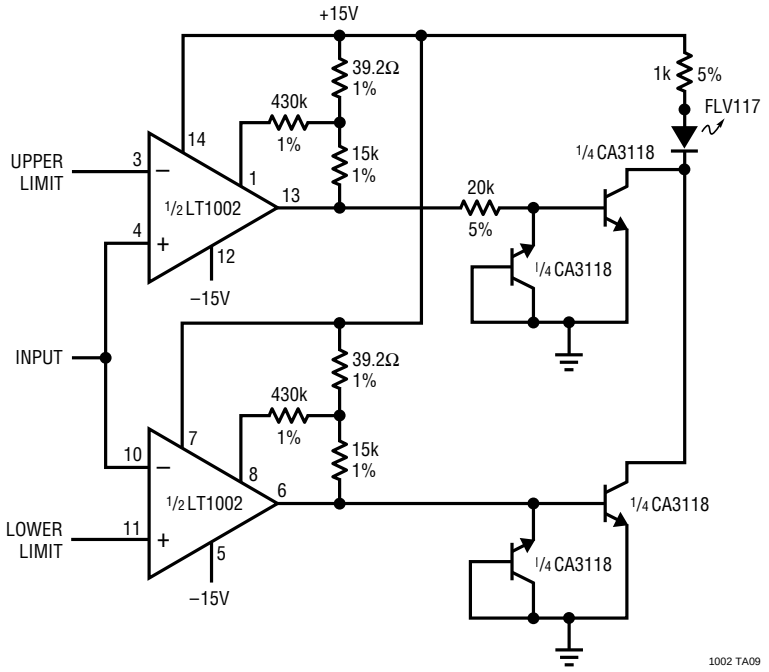
APPLICATIONS INFORMATION

Precision ±10V Reference



The LT1002 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference. The accuracy of the –10V output is limited by the matching of the two 10k resistors.

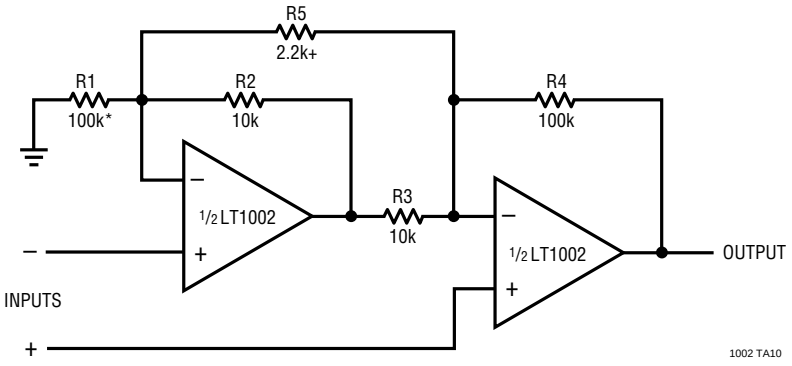
Dual Limit Microvolt Comparator



When the upper or lower limit is exceeded the LED lights up. Positive feedback to one of the nulling terminals creates 5 to 20μV of hysteresis on both amplifiers. This feedback changes the offset voltage of the LT1002 by less than 5μV. Therefore, the basic accuracy of the comparator is limited only by the low offset voltage of the LT1002.

APPLICATIONS INFORMATION

Two Op Amp Instrumentation Amplifier

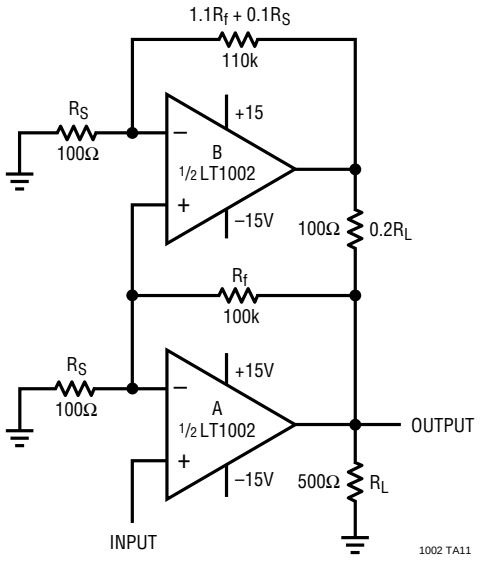


* TRIM FOR COMMON-MODE REJECTION

\+ TRIM FOR GAIN

$$\text{Gain} = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] \approx 100$$

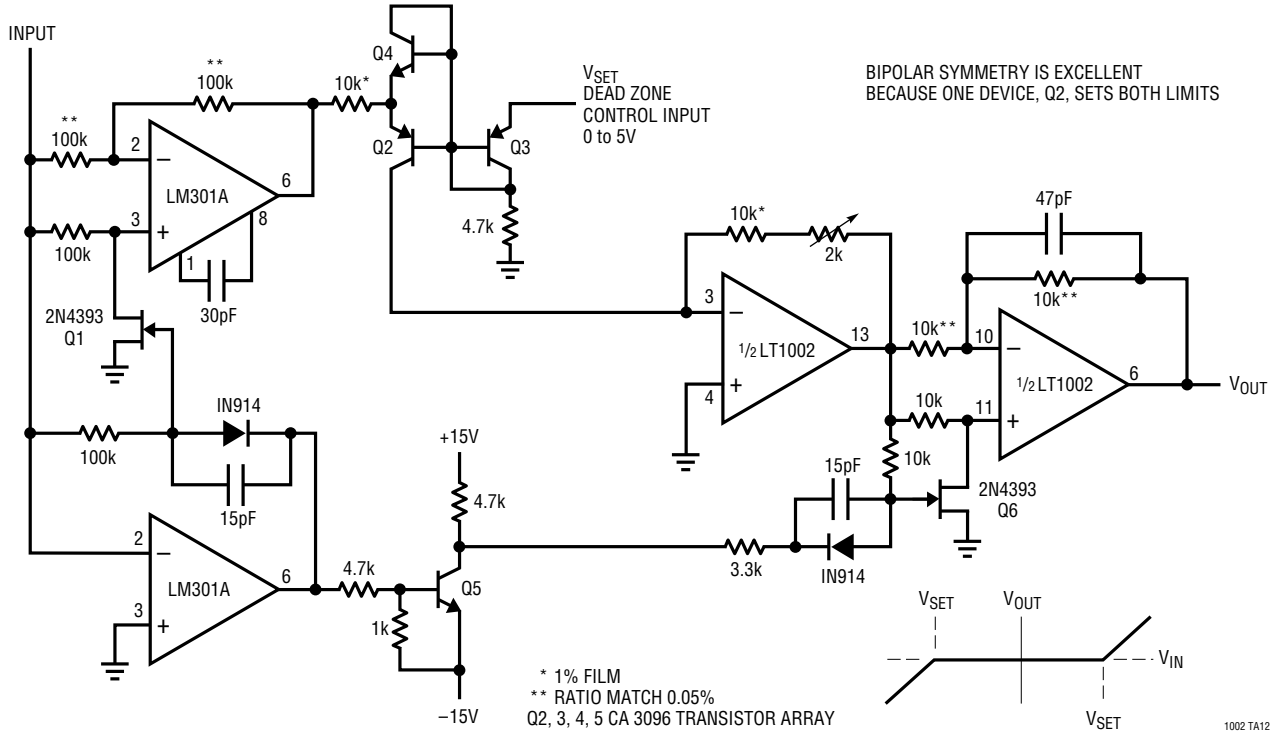
Precision Amplifier Drives 500Ω Load to ±10V



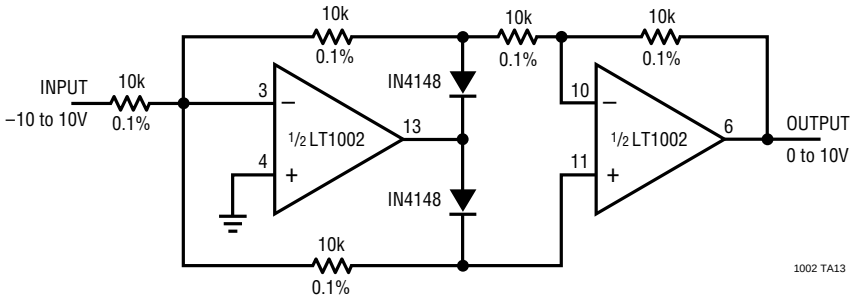
This application utilizes the guaranteed 10mA load driving capability of the LT1002. The offset voltage of amplifier A is the offset of the configuration. Amplifier B provides the additional 10mA load current. When load resistor R_L is removed, amplifier A sinks this current without affecting accuracy. In the gain of 1000 configuration shown, approximately 0.3% gain accuracy can be realized.

APPLICATIONS INFORMATION

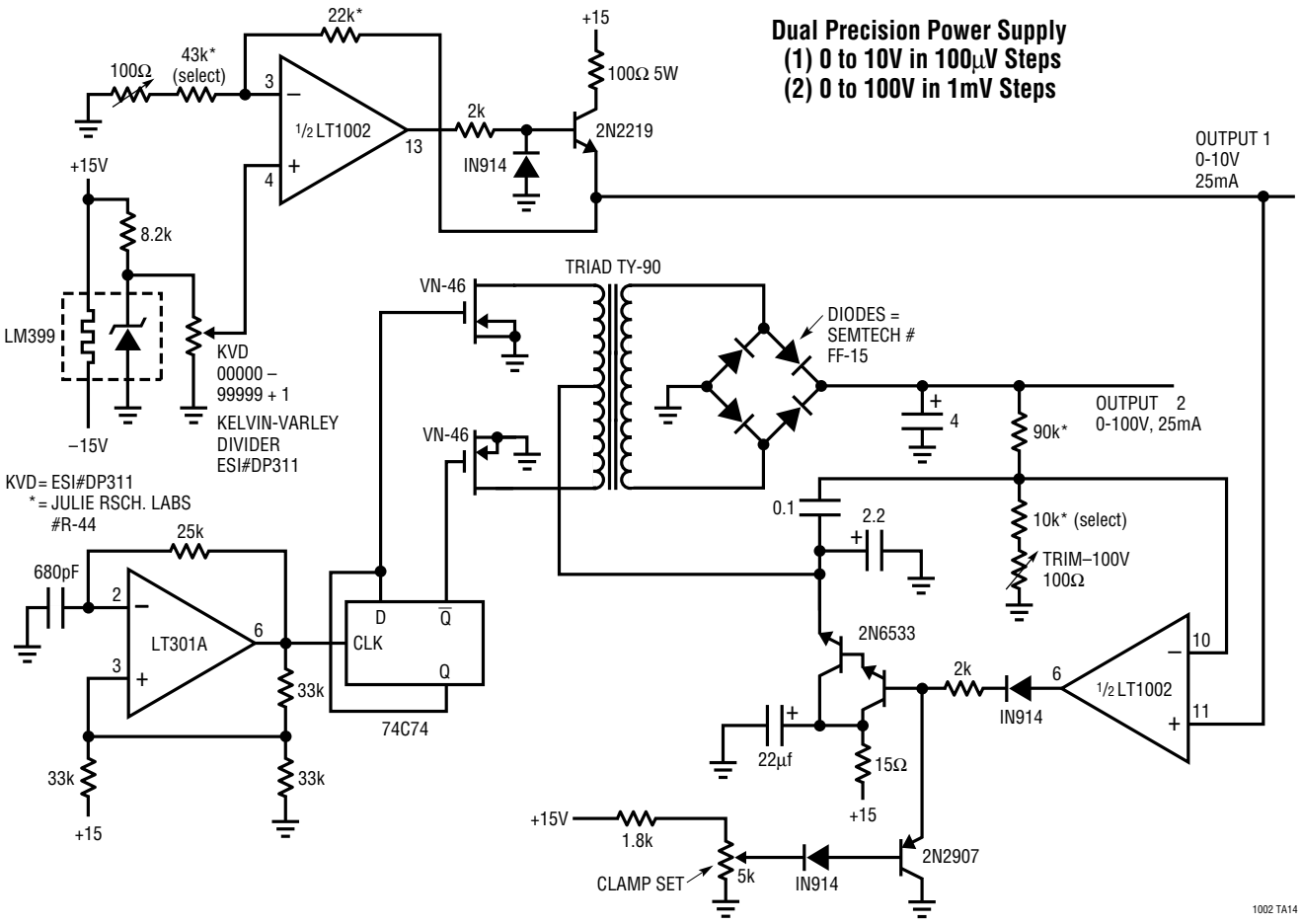
Dead Zone Generator



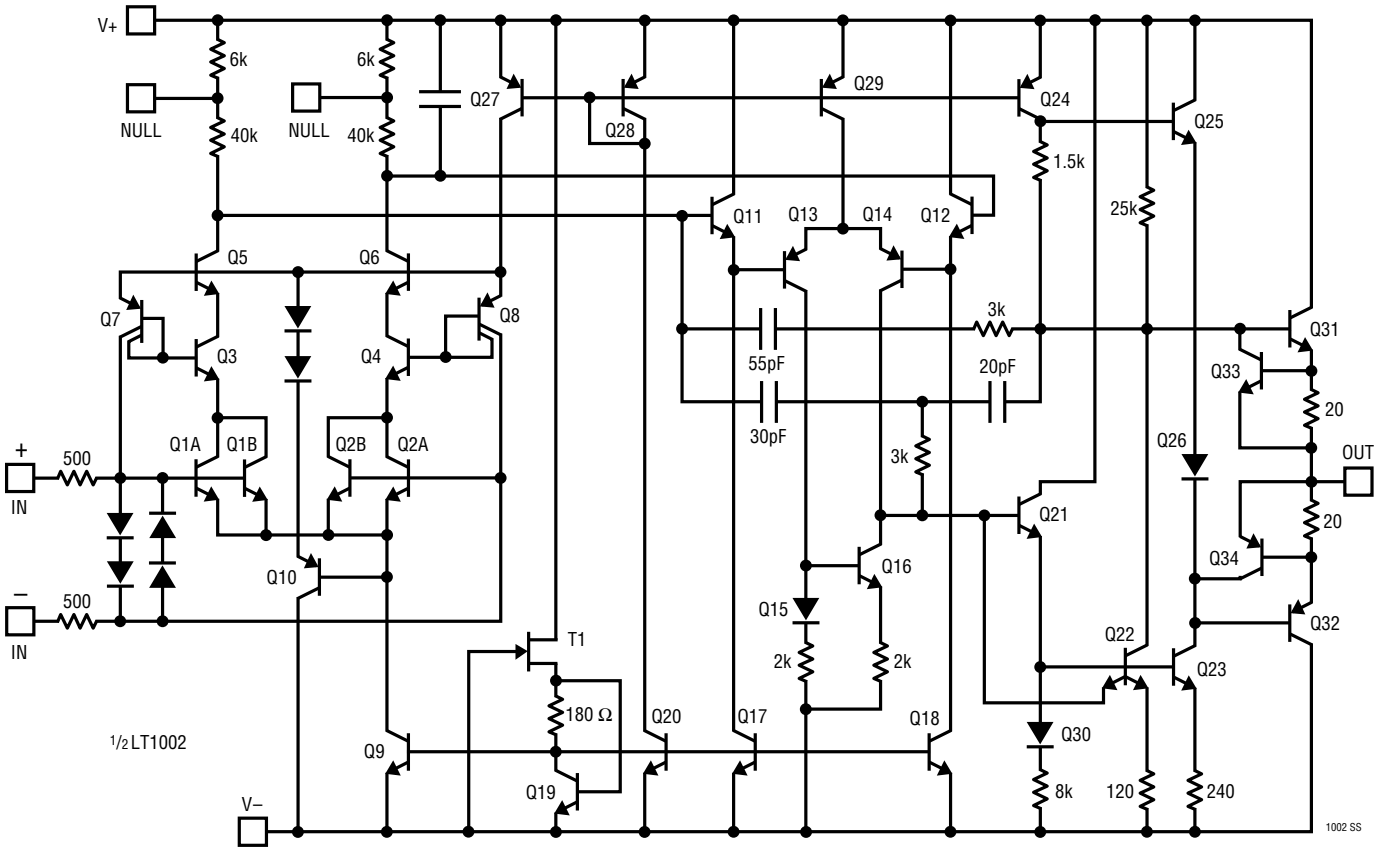
Precision Absolute Value Circuit



APPLICATIONS INFORMATION



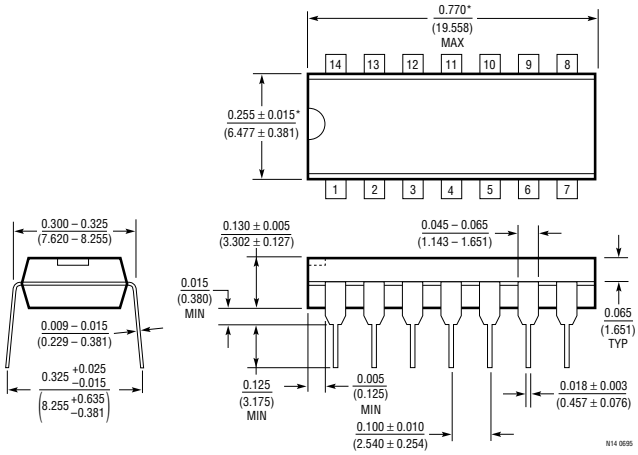
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

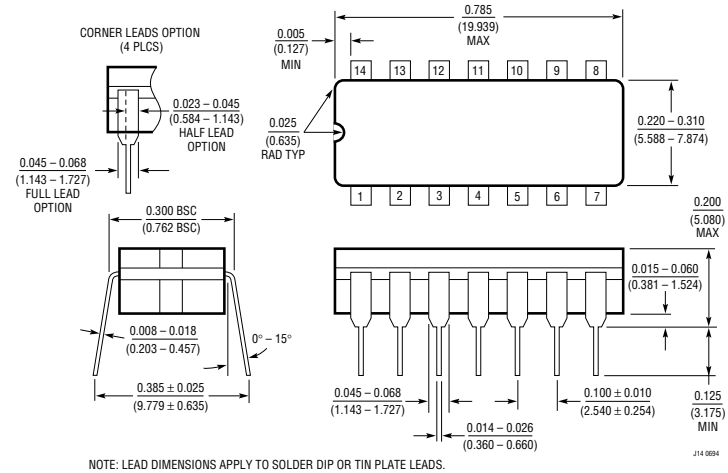
N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

	T_{JMAX}	θ_{JA}
LT1002ACN LT1002CN	125°C	100°C/W

J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

	T_{JMAX}	θ_{JA}
LT1002ACJ LT1002CJ	125°C	100°C/W
LT1002AMJ LT1002MJ	125°C	100°C/W

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