150MHz, 250V/μs, $A_V \geq 4$ Operational Amplifier

FEATURES

- **Gain-Bandwidth: 150MHz**
- **Gain of 4 Stable**
- **Slew Rate: 250V/μs**
- Input Noise Voltage: $6nV/\sqrt{Hz}$
- C-Load™ Op Amp Drives Capacitive Loads
- Maximum Input Offset Voltage: 600μV
- Maximum Input Bias Current: 300nA
- Maximum Input Offset Current: 300nA
- Minimum Output Swing Into 500Ω: ±12V
- Minimum DC Gain: 50V/mV, R_L = 500Ω
- Settling Time to 0.1%: 65ns, 10V Step
- Settling Time to 0.01%: 85ns, 10V Step
- Differential Gain: 0.08%, A_V = 4, R_L = 150Ω
- Differential Phase: 0.2°, A_V = 4, R_L = 150Ω

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- 8-, 10-, 12-Bit Data Acquisition Systems

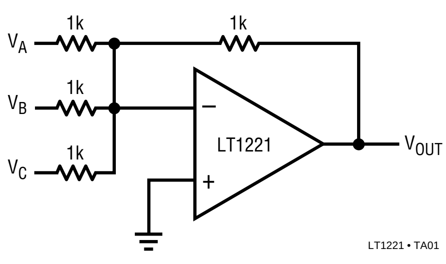
DESCRIPTION

The LT1221 is a very high speed operational amplifier with superior DC performance. The LT1221 is stable in a noise gain of 4 or greater. It features reduced input offset voltage, lower input bias currents and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage that includes proprietary DC gain enhancement circuitry to obtain precision with high speed. The high gain and fast settling time make the circuit an ideal choice for data acquisition systems. The circuit is also capable of driving capacitive loads which makes it useful in buffer or cable driver applications.

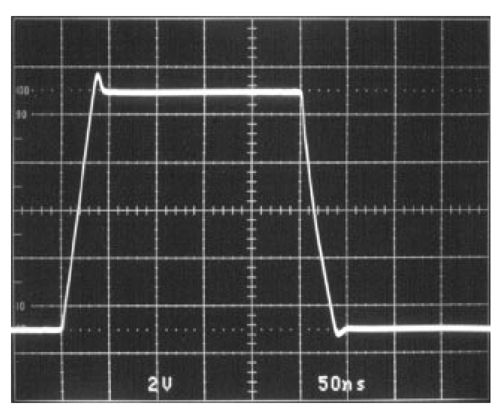
The LT1221 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced complementary bipolar processing. For unity-gain stable applications the LT1220 can be used, and for gains of 10 or greater the LT1222 can be used.

TYPICAL APPLICATION

Summing Amplifier



Summing Amplifier Large-Signal Response



V_S = ±15V f = 2MHz
V_{IN} = $10V_{P-P}$

LT1221 • TA02

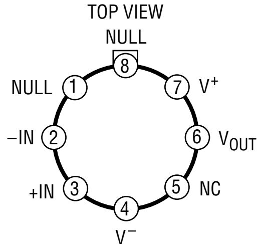
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 1) .... Indefinite
Specified Temperature Range
  LT1221C (Note 2) .... 0°C to 70°C
  LT1221M .... –55°C to 125°C

Operating Temperature Range
  LT1221C .... –40°C TO 85°C
  LT1221M .... –55°C to 125°C
Maximum Junction Temperature (See Below)
  Plastic Package .... 150°C
  Ceramic Package .... 175°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



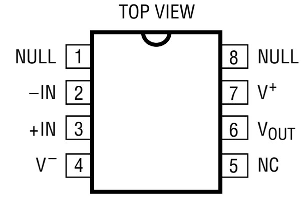
H PACKAGE
8-LEAD TO-5 METAL CAN

T_{JMAX} = 175°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

SPECIAL ORDER CONSULT FACTORY

TOP VIEW



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

ORDER PART NUMBER

LT1221CN8
LT1221MJ8
LT1221CS8

S8 PART MARKING

1221

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS V_S = ±15V, T_A = 25°C, V_{CM} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)		200	600	µV
I_{OS}	Input Offset Current			100	300	nA
I_B	Input Bias Current			100	300	nA
e_n	Input Noise Voltage	f = 10kHz		6		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		2		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	20	45 80		MΩ kΩ
C_{IN}	Inut Capacitance			2		pF
	Input Voltage Range (Positive) Input Voltage Range (Negative)		12	14 –13	 –12	V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	92	114		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	90	110		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±10V, R_L = 500Ω	50	100		V/mV
V_{OUT}	Output Swing	R_L = 500Ω	12	13		±V
I_{OUT}	Output Current	V_{OUT} = ±12V	24	26		mA
SR	Slew Rate	(Note 4)	200	250		V/µs
	Full Power Bandwidth	10V Peak (Note 5)		4		MHz
GBW	Gain-Bandwidth	f = 1MHz		150		MHz

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_r, t_f	Rise Time, Fall Time	$A_V = 4$, 10% to 90%, 0.1V			3.2		ns
	Overshoot	$A_V = 4$, 0.1V			10		%
	Propagation Delay	$A_V = 4$, 50% V_{IN} to 50% V_{OUT}, 0.1V			5.4		ns
t_s	Settling Time	10V Step, 0.1% 10V Step, 0.01%			65 85		ns ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$ (Note 6) f = 3.58MHz, R_L = 1k (Note 6)			0.08 0.02		% %
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$ (Note 6) f = 3.58MHz, R_L = 1k (Note 6)			0.20 0.05		DEG DEG
R_O	Output Resistance	$A_V = 4$, f = 1MHz			0.3		Ω
I_S	Supply Current				8	10.5	mA

$V_S = \pm15V$, $0°C \le T_A \le 70°C$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)	●		0.2	1.5	mV
	Input V_{OS} Drift				15		μV/°C
I_{OS}	Input Offset Current		●		100	400	nA
I_B	Input Bias Current		●		100	400	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	●	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	●	90	110		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	●	40	100		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$	●	12	13		±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	●	24	26		mA
SR	Slew Rate	(Note 4)	●	180	250		V/μs
I_S	Supply Current		●		8	11	mA

$V_S = \pm15V$, $-55°C \le T_A \le 125°C$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)	●		0.2	2	mV
	Input V_{OS} Drift				15		μV/°C
I_{OS}	Input Offset Current		●		100	800	nA
I_B	Input Bias Current		●		100	1000	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	●	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	●	90	110		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	●	12.5	100		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$ R_L = 1k	● ●	10 12	13 13		±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm10V$ $V_{OUT} = \pm12V$	● ●	20 12	26 13		mA mA
SR	Slew Rate	(Note 4)	●	130	250		V/μs
I_S	Supply Current		●		8	11	mA

The ● denotes specifications which apply over the full temperature range.

Note 1: A heat sink may be required when the output is shorted indefinitely.

Note 2: Commercial parts are designed to operate over −40°C to 85°C, but are not tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over −40°C to 85°C are available on special request. Consult factory.

Note 3: Input offset voltage is pulse tested and is exclusive of warm-up drift.

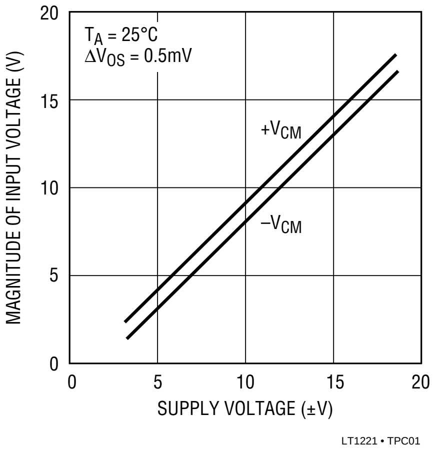
Note 4: Slew rate is measured between ±10V on an output swing of ±12V.

Note 5: $FPBW = SR/2\pi V_P$.

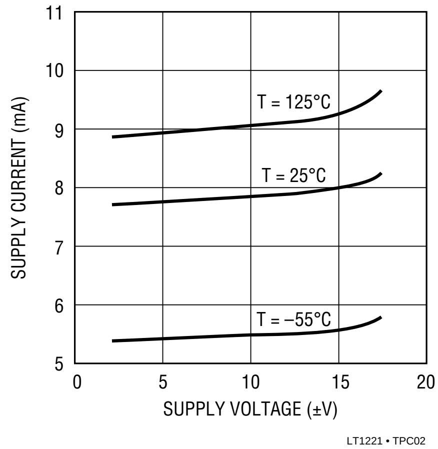
Note 6: Differential Gain and Phase are tested in $A_V = 4$ with five amps in series. Attenuators of 1/4 are used as loads (36.5Ω, 110Ω and 249Ω, 750Ω).

TYPICAL PERFORMANCE CHARACTERISTICS

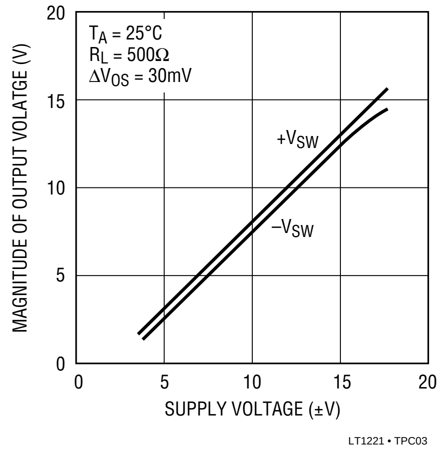
Input Common-Mode Range vs Supply Voltage



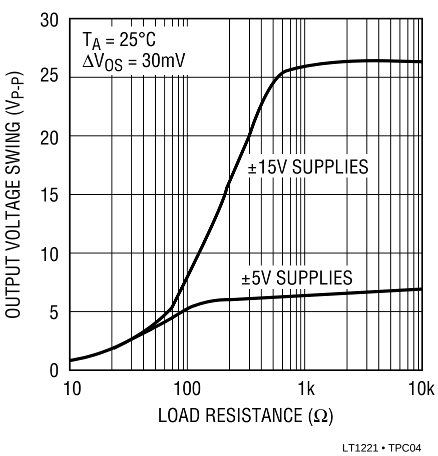
Supply Current vs Supply Voltage and Temperature



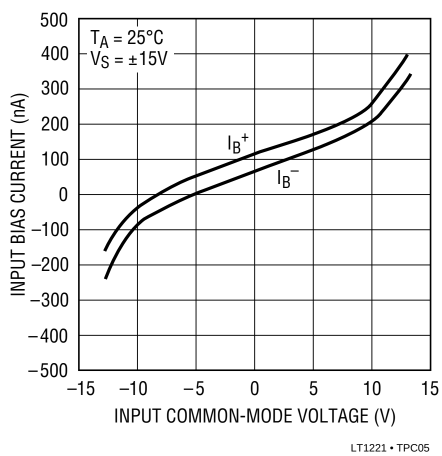
Output Voltage Swing vs Supply Voltage



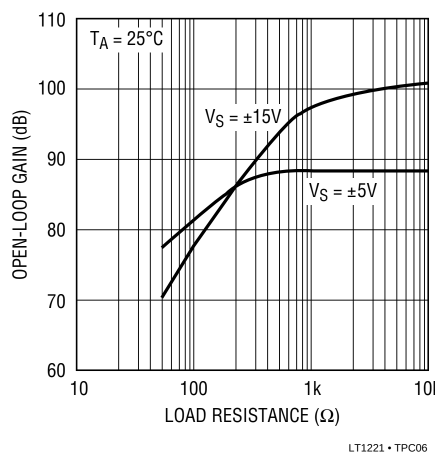
Output Voltage Swing vs Resistive Load



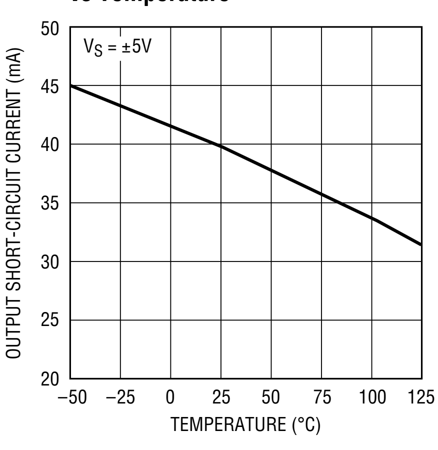
Input Bias Current vs Input Common-Mode Voltage



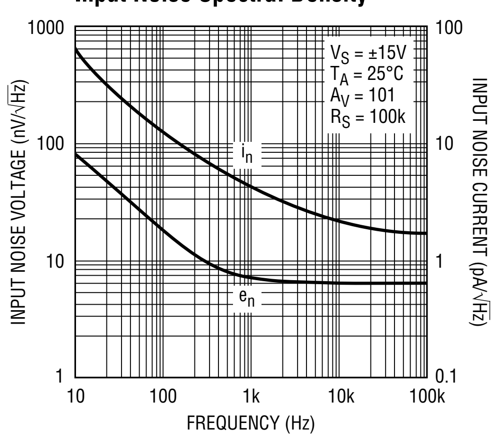
Open-Loop Gain vs Resistive Load



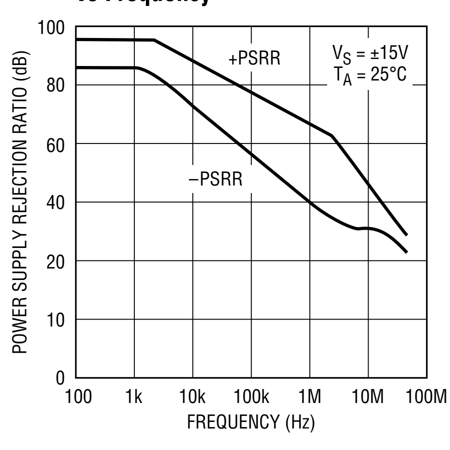
Output Short-Circuit Current vs Temperature



Input Noise Spectral Density

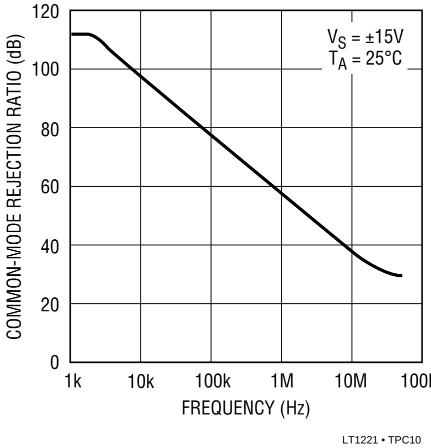


Power Supply Rejection Ratio vs Frequency

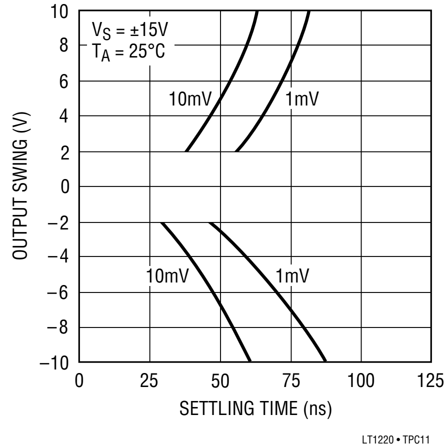


TYPICAL PERFORMANCE CHARACTERISTICS

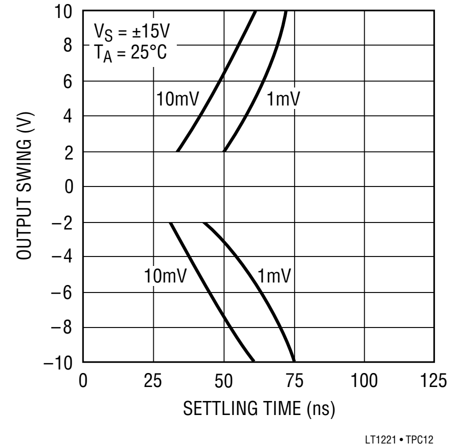
Common-Mode Rejection Ratio vs Frequency



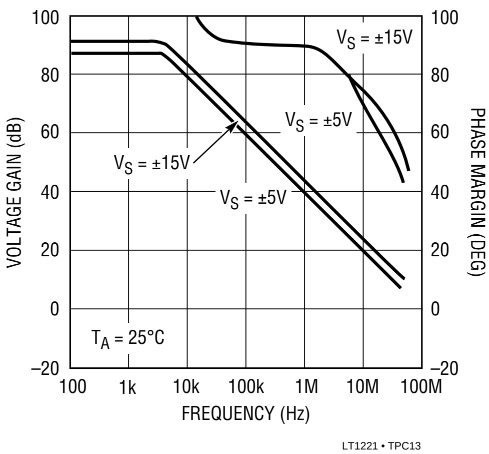
Output Swing and Error vs Settling Time (Noninverting)



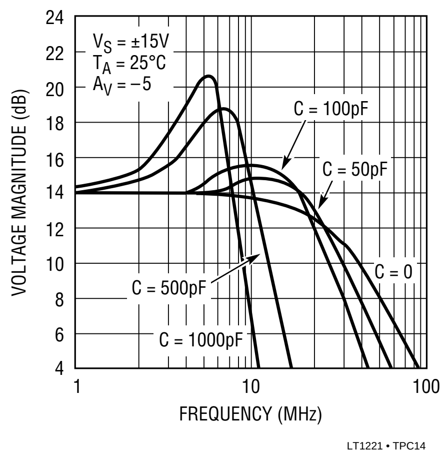
Output Swing and Error vs Settling Time (Inverting)



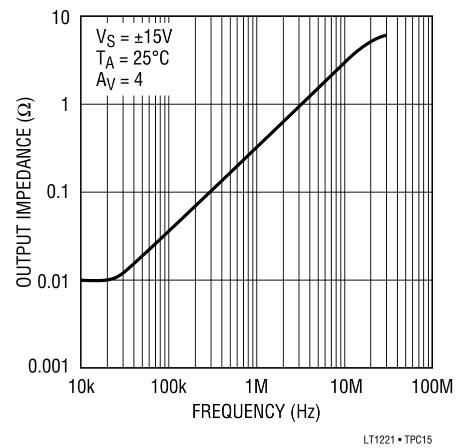
Voltage Gain and Phase vs Frequency



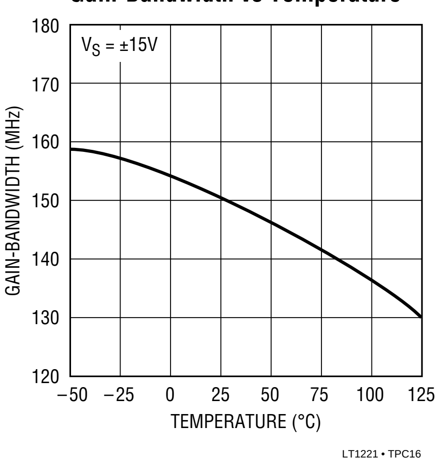
Frequency Response vs Capacitive Load



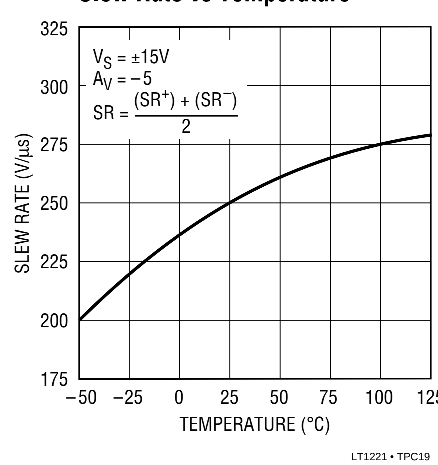
Closed-Loop Output Impedance vs Frequency



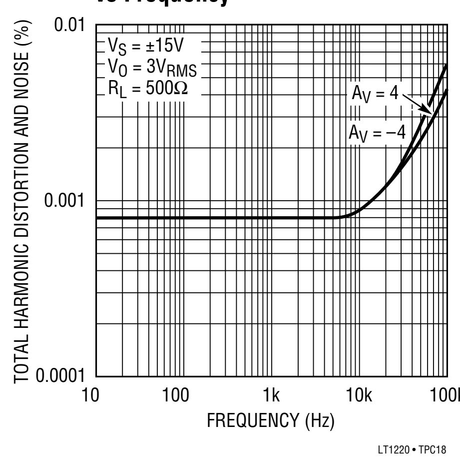
Gain-Bandwidth vs Temperature



Slew Rate vs Temperature

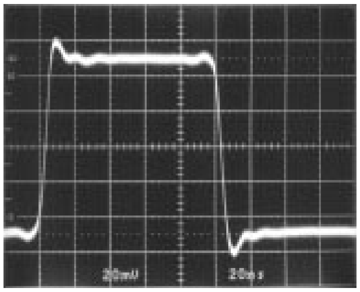


Total Harmonic Distortion vs Frequency



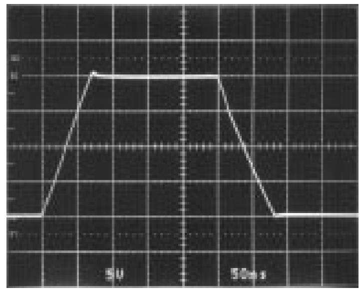
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal, A_V = 4



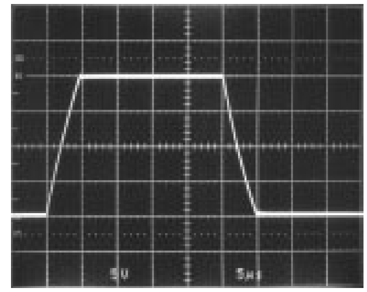
V_S = ±15V f = 5MHz LT1221 • TPC19
V_{IN} = 25mV

Large Signal, A_V = 4



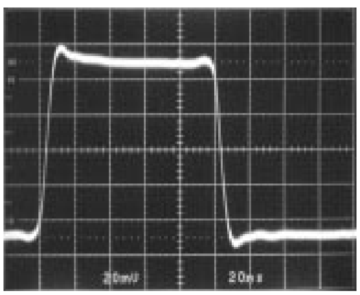
V_S = ±15V f = 2MHz LT1221 • TPC20
V_{IN} = $5V_{P-P}$

Large Signal, A_V = 4, C_L = 10,000pF



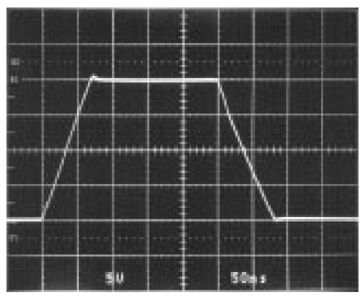
V_S = ±15V f = 20kHz LT1221 • TPC21
V_{IN} = $5V_{P-P}$

Small Signal, A_V = –4



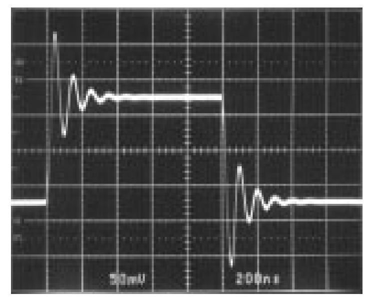
V_S = ±15V f = 5MHz LT1221 • TPC22
V_{IN} = 25mV

Large Signal, A_V = –4



V_S = ±15V f = 2MHz LT1221 • TPC23
V_{IN} = $5V_{P-P}$

Small Signal, A_V = –4, C_L = 1,000pF

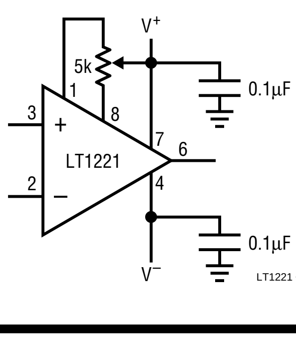


V_S = ±15V f = 500kHz LT1221 • TPC24
V_{IN} = 42mV

APPLICATIONS INFORMATION

The LT1221 is stable in noise gains of 4 or greater and may be inserted directly into HA2520/2/5, HA2541/2/4, AD817, AD847, EL2020, EL2044 and LM6361 applications, provided that the nulling circuitry is removed and the amplifier configuration has a high enough noise gain. The suggested nulling circuit for the LT1221 is shown in the following figure.

Offset Nulling



LT1221 • AI01

Layout and Passive Components

The LT1221 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example, fast settling time) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistors greater than 5k are not recommended because a pole is formed with the input capacitance which can cause peaking or oscillations.

Input Considerations

Bias current cancellation circuitry is employed on the inputs of the LT1221 so the input bias current and input

APPLICATIONS INFORMATION

offset current have identical specifications. For this reason, matching the impedance on the inputs to reduce bias current errors is not necessary.

Capacitive Loading

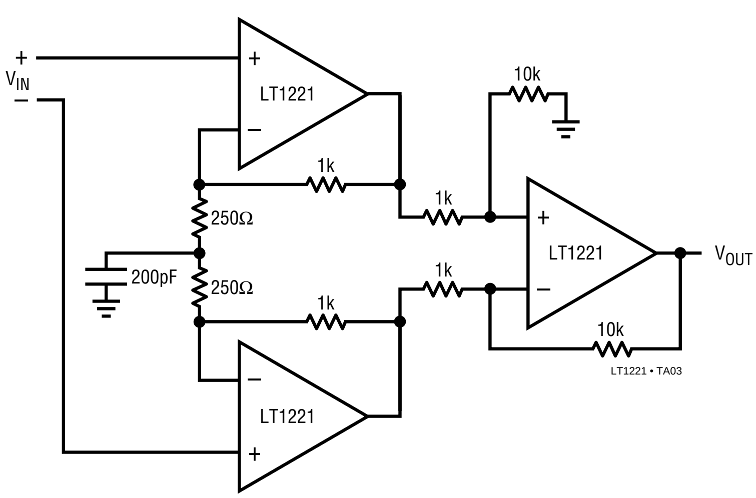
The LT1221 is stable with capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease. There will be peaking in the frequency domain as shown in the curve of Frequency Response vs Capacitive Load. The small-signal transient response will have more overshoot as shown in the photo of the small-signal response with 1000pF load. The large-signal response with a 10,000pF load shows the output slew rate being limited to 4V/µs by the short-circuit current. The LT1221 can drive coaxial cable directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Compensation

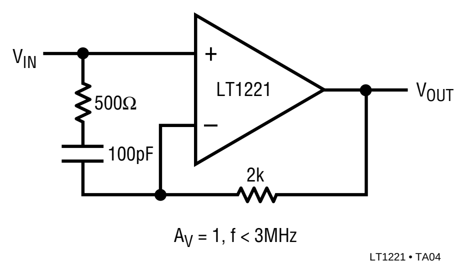
The LT1221 has a typical gain-bandwidth product of 150MHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 10, it will have a bandwidth of about 15MHz). The amplifier is stable in a noise gain of 4 so the ratio of the signal at the inverting input to the output must be 1/4 or less. Straightforward gain configurations of 4 or –3 are stable, but there are several others that allow the amplifier to be stable for lower signal gains (the noise gain, however, remains 4 or more). One example is the summing amplifier on the first page of this data sheet. Each input signal has a gain of –1 to the output, but it is easily seen that this configuration is equivalent to a gain of –3 as far as the amplifier is concerned. Another circuit is shown below with a DC gain of 1, but an AC gain of 5. The break frequency of the R-C combination across the amplifier inputs should be approximately a factor of 10 less than the gain-bandwidth of the amplifier divided by the high frequency gain (in this case 1/10 of 150MHz/5 or 3MHz).

TYPICAL APPLICATIONS

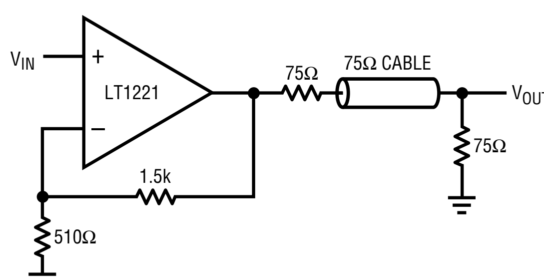
20MHz, A_V = 50 Instrumentation Amplifier



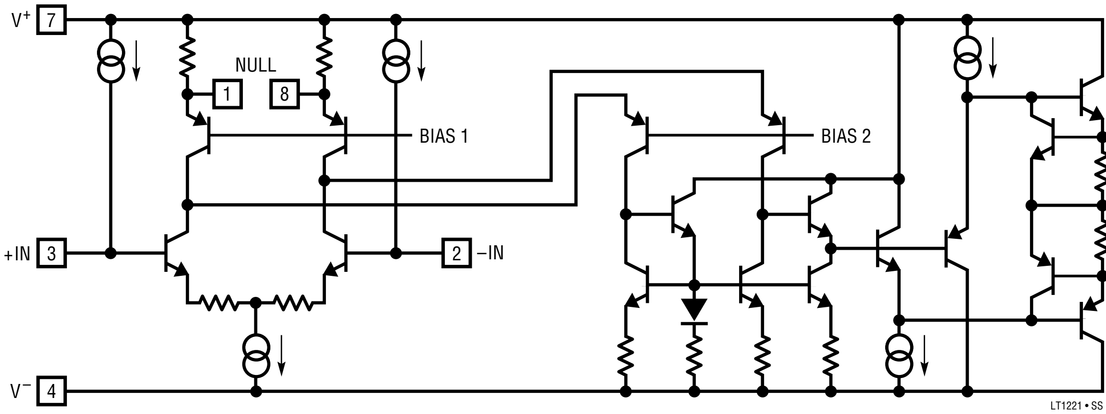
Lag Compensation



Cable Driver

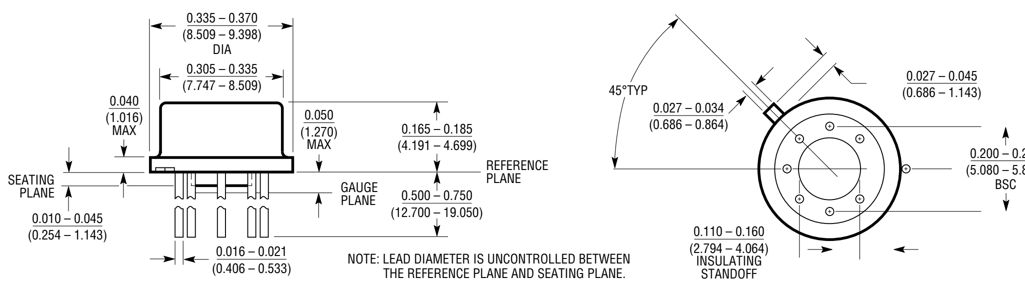


SIMPLIFIED SCHEMATIC

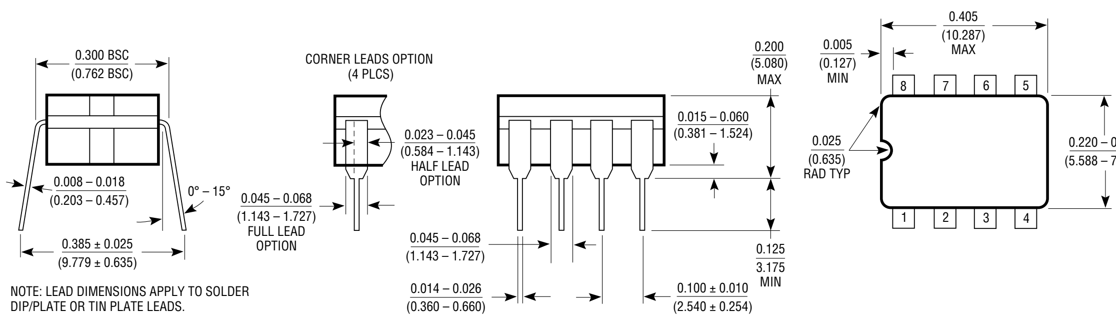


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

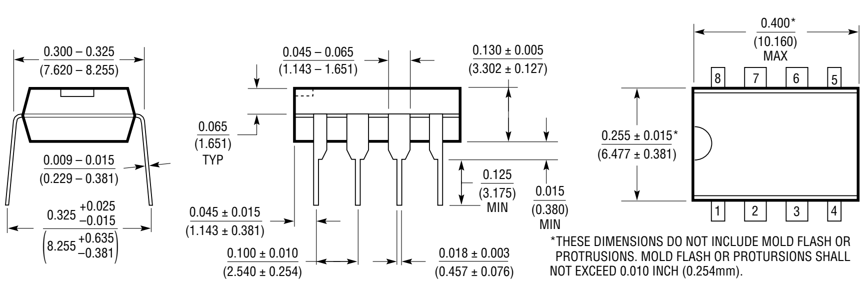
H8 Package
8-Lead TO-5
Metal Can



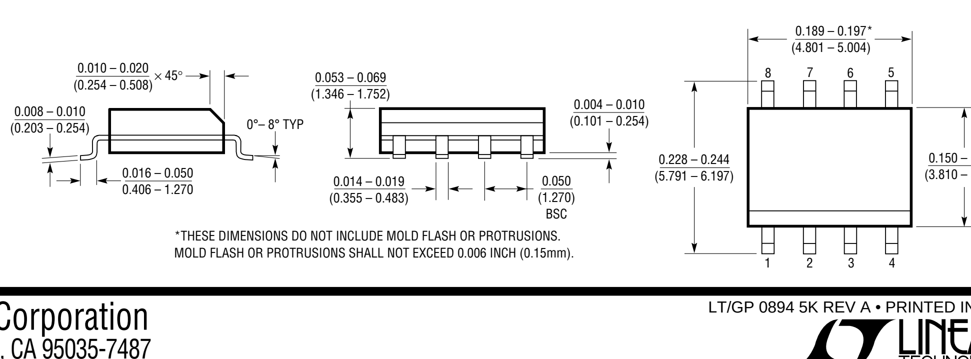
J8 Package
8-Lead Ceramic Dip



N8 Package
8-Lead Plastic Dip



S8 Package
8-Lead Plastic SOIC



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