LINEAR TECHNOLOGY

Multiple Modulation Standard Infrared Receiver

FEATURES

- **Receives Multiple IR Modulation Methods**
- **Low Noise, High Speed Preamp: 2pA/√Hz, 7MHz**
- **Low Frequency Ambient Rejection Loops**
- **Dual Gain Channels: 8MHz, 400V/V**
- 25ns and 60ns Comparators
- 16-Lead SO Package
- 5V Single Supply Operation
- Supply Current: 14mA
- Shutdown Supply Current: 500µA
- External Comparator Threshold Setting

MODULATION STANDARDS

- IRDA: SIR, FIR
- Sharp/Newton
- TV Remote
- High Data Rate Modulation Methods

DESCRIPTION

The LT®1319 is a general purpose building block that contains all the circuitry necessary to transform modulated photodiode signals back to digital signals. The circuit's flexibility permits it to receive multiple modulation methods. A low noise, high frequency preamplifier performs a current-to-voltage conversion while rejecting low frequency ambient interference with an AC coupling loop. Two separate high impedance filter buffer inputs are provided so that off-chip filtering can be tailored for specific modulation schemes. The filter buffers drive separate differential gain stages that end in comparators with internal hysteresis. The comparator thresholds are adjustable externally by the current into Pin 11. One channel has a high speed 25ns comparator required for high data rates. The second channel's comparator has a 60ns response time and is well suited to more modest data rates. A power saving shutdown feature is useful in portable applications.

For IRDA 4PPM contact the LTC Marketing Department.

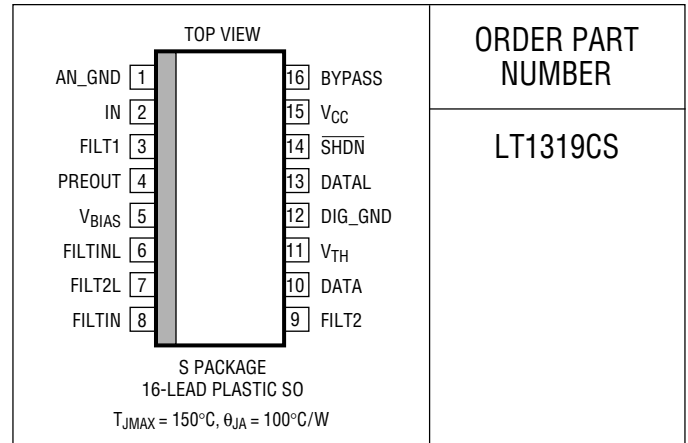$\mathcal{LT}$, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

IRDA and Sharp/Newton Data Receiver

LT1319 • TA01

LT1319
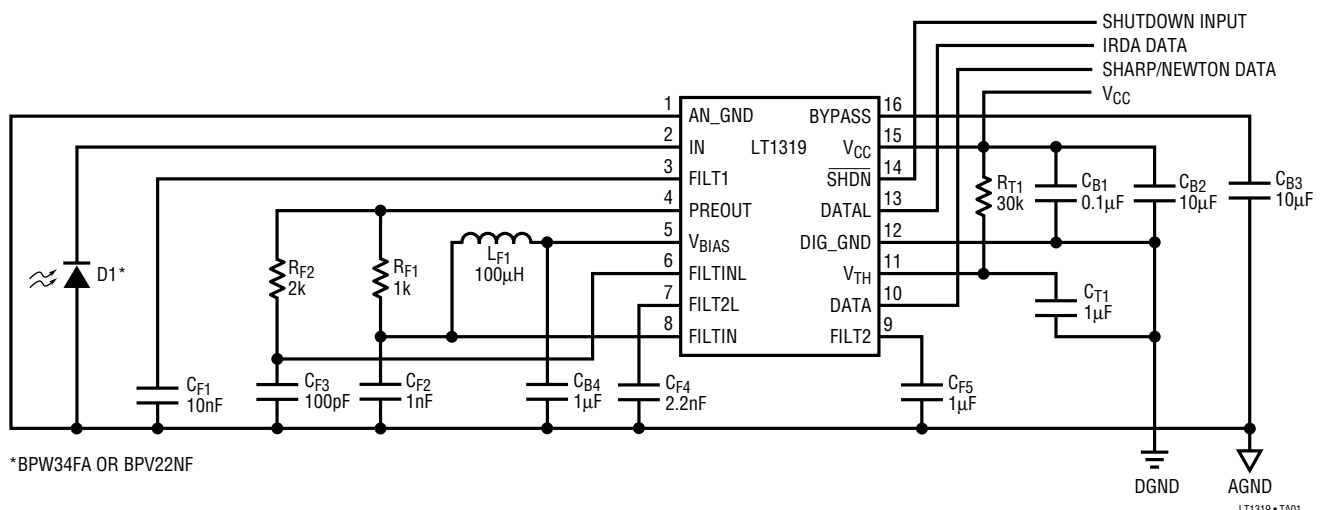
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{CC} to GND) 6V
Differential Voltage (Any Two Pins) 6V
Maximum Junction Temperature .... 150°C
Operating Temperature Range .... 0°C to 70°C
Specified Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

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                  TOP VIEW
      AN_GND  [1]              [16]  BYPASS
          IN  [2]              [15]  V_CC
       FILT1  [3]              [14]  SHDN
      PREOUT  [4]              [13]  DATAL
       V_BIAS [5]              [12]  DIG_GND
     FILTINL  [6]              [11]  V_TH
      FILT2L  [7]              [10]  DATA
      FILTIN  [8]              [9]   FILT2
```

S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1319CS

Consult factory for Industrial or Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{15} = 5V, V_1 = V_{12} = 0V, V_6 = V_8 = V_{14} = 2V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Preamp Input Offset Voltage	V (Pin 2) – V (Pin 5)		4	15	mV
	Preamp Output Offset Voltage	V (Pin 4) – V (Pin 5)		10	25	mV
	Preamp Loop Offset Voltage	V (Pin 3) – V (Pin 5)	50	150	250	mV
	High Gain Loop Offset Voltage	V (Pin 9) – V (Pin 5)	600	800	950	mV
	Low Gain Loop Offset Voltage	V (Pin 7) – V (Pin 5)	600	800	950	mV
A_{VP}	Preamp Transimpedance	±10µA Into Pin 2, Measure ΔV (Pin 4), Fix Pin 3	10	15	17	kΩ
	Preamp Output Swing, Positive	100µA Out of Pin 2, Measure ΔV (Pin 4), Fix Pin 3	0.25	0.4	0.55	V
	Preamp Output Swing, Negative	100µA Into Pin 2, Measure ΔV (Pin 4), Fix Pin 3	−0.55	−0.4	−0.25	V
BW_P	Preamp Bandwidth	C (Pin 3) = 1µF, Measure f_{-3dB}		7		MHz
i_n	Preamp Input Noise Current	C (Pin 3) = 1µF, f = 10kHz		2		pA/√Hz
	Preamp Loop Rejection, Positive	50µA Into Pin 2, Measure ΔV (Pin 4)	−3	−1	3	mV
	Preamp Loop Rejection, Negative	50µA Out of Pin 2, Measure ΔV (Pin 4)	−3	1	3	mV
	Preamp Loop Output Current, Positive	100µA Out of Pin 2, Measure I (Pin 3), (Note 1)	−150	−100	−50	µA
	Preamp Loop Output Current, Negative	100µA Into Pin 2, Measure I (Pin 3), (Note 1)	50	100	150	µA
V_{BIAS}	Bias Voltage	V (Pin 5)	1.7	1.9	2.1	V
V_{BYPASS}	Bypass Voltage	V (Pin 16)	4.75	4.9	4.95	V
I_B	Filter Buffer Input Bias Current	I (Pin 6), I (Pin 8)	0.1	0.5	1.4	µA
R_{IN}	Filter Buffer Input Resistance	ΔV = 0.1V, Measure ΔI_B Pin 6, Pin 8		40		MΩ
	Gain Stage Loop Rejection, Positive	ΔV = 50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	0.33	0.45	0.57	V
	Gain Stage Loop Rejection, Negative	ΔV = −50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	−0.57	−0.45	−0.33	V
A_{VG}	Gain Stages Voltage Gain	(Note 2)		400		V/V
BW_G	Gain Stages Bandwidth	C (Pin 7) = C (Pin 9) = 1µF		8		MHz
t_r	Fast Comparator Response Time	10mV Overdrive		25		ns
	Slow Comparator Response Time	10mV Overdrive		60		ns
V_{HYS}	Fast Comparator Hysteresis Voltage	(Note 3)		35		mV
	Slow Comparator Hysteresis Voltage	(Note 3)		40		mV
V_{OH}	Fast Comparator Output High Voltage	ΔV (Pin 9) = −200mV, 1mA Out of Pin 10 (Note 4)	2.4	3.5		V
	Slow Comparator Output High Voltage	ΔV (Pin 7) = −200mV, 0.1mA Out of Pin 13 (Note 4)	2.4	3.9		V
V_{OL}	Fast Comparator Output Low Voltage	ΔV (Pin 9) = 200mV, 800µA Into Pin 10		0.35	0.5	V
	Slow Comparator Output Low Voltage	ΔV (Pin 7) = 200mV, 800µA Into Pin 13		0.39	0.5	V

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{15} = 5V$, $V_1 = V_{12} = 0V$, $V_6 = V_8 = V_{14} = 2V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Threshold Transimpedance	100μA Into Pin 11 (Note 5)		2		kΩ
V_{TH}	Threshold External Voltage	100μA Into Pin 11, V (Pin 11)	0.8	0.9	1.2	V
V_{IH}	Shutdown Input High Voltage		2			V
V_{IL}	Shutdown Input Low Voltage				0.8	V
I_{IH}	Shutdown Input High Current	V (Pin 14) = 2.4V	−140	−60	−10	μA
I_{IL}	Shutdown Input Low Current	V (Pin 14) = 0.4V	−400	−260	−130	μA
I_S	Supply Current	V (Pin 14) = 2V	10	14	18	mA
I_{SHDN}	Supply Current in Shutdown	V (Pin 14) = 0.8V, V (Pin 6) = V (Pin 8) = 0V	300	500	800	μA

$0°C \leq T_A \leq 70°C$, $V_{15} = 5V$, $V_1 = V_{12} = 0V$, $V_6 = V_8 = V_{14} = 2V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Preamp Input Offset Voltage	V (Pin 2) − V (Pin 5)		4	17	mV
	Preamp Output Offset Voltage	V (Pin 4) − V (Pin 5)		10	27	mV
	Preamp Loop Offset Voltage	V (Pin 3) − V (Pin 5)	30	150	350	mV
	High Gain Loop Offset Voltage	V (Pin 9) − V (Pin 5)	400	800	1200	mV
	Low Gain Loop Offset Voltage	V (Pin 7) − V (Pin 5)	400	800	1200	mV
A_{VP}	Preamp Transimpedance	±10μA Into Pin 2, Measure ΔV (Pin 4)	8.5	15	18.5	kΩ
	Preamp Output Swing, Positive	100μA Out of Pin 2, Measure ΔV (Pin 4)	0.2	0.4	0.6	V
	Preamp Output Swing, Negative	100μA Into Pin 2, Measure ΔV (Pin 4)	−0.6	−0.4	−0.2	V
	Preamp Loop Rejection, Positive	50μA Into Pin 2, Measure ΔV (Pin 4)	−3.5	−1	3.5	mV
	Preamp Loop Rejection, Negative	50μA Out of Pin 2, Measure ΔV (Pin 4)	−3.5	1	3.5	mV
	Preamp Loop Output Current, Positive	100μA Out of Pin 2, Measure I (Pin 3), (Note 1)	−160	−100	−40	μA
	Preamp Loop Output Current, Negative	100μA Into Pin 2, Measure I (Pin 3), (Note 1)	40	100	160	μA
V_{BIAS}	Bias Voltage	V (Pin 5)	1.5	1.9	2.3	V
V_{BYPASS}	Bypass Voltage	V (Pin 16)	4.7	4.9	4.97	V
I_B	Filter Buffer Input Bias Current	I (Pin 6), I (Pin 8)	0.05	0.5	1.6	μA
	Gain Stage Loop Rejection, Positive	ΔV = 50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	0.3	0.45	0.6	V
	Gain Stage Loop Rejection, Negative	ΔV = −50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	−0.6	−0.45	−0.3	V
V_{OH}	Fast Comparator Output High Voltage	ΔV (Pin 9) = −200mV, 1mA Out of Pin 10 (Note 4)	2.4	3.5		V
	Slow Comparator Output High Voltage	ΔV (Pin 7) = −200mV, 0.1mA Out of Pin 13 (Note 4)	2.4	3.9		V
V_{OL}	Fast Comparator Output Low Voltage	ΔV (Pin 9) = 200mV, 800μA Into Pin 10		0.35	0.5	V
	Slow Comparator Output Low Voltage	ΔV (Pin 7) = 200mV, 800μA Into Pin 13		0.39	0.5	V
V_{TH}	Threshold External Voltage	100μA Into Pin 11, V (Pin 11)	0.7	0.9	1.3	V
V_{IH}	Shutdown Input High Voltage		2			V
V_{IL}	Shutdown Input Low Voltage				0.8	V
I_{IH}	Shutdown Input High Current	V (Pin 14) = 2.4V	−160	−60	0	μA
I_{IL}	Shutdown Input Low Current	V (Pin 14) = 0.4V	−450	−260	−80	μA
I_S	Supply Current	V (Pin 14) = 2V	9	14	20	mA
I_{SHDN}	Supply Current in Shutdown	V (Pin 14) = 0.8V, V (Pin 6) = V (Pin 8) = 0V	200	500	900	μA

Note 1: Measure V (Pin 3) without input current for Pin 2. Force Pin 3 to this measured voltage (which disables the preamp loop). Measure the current into and out of Pin 3 when Pin 2 is driven.

Note 2: The gain is the differential voltage at the comparator inputs divided by the differential voltage between the filter buffer output and V_{BIAS}. This parameter is not tested.

Note 3: Hysteresis is the difference in comparator trip point measured when the output is high and when the output is low. This parameter is not tested.

Note 4: Measure V (Pin 7) and V (Pin 9). Force these voltages to 200mV below their nominal value to switch the comparators high.

Note 5: The current into Pin 11 is multiplied by 4 and then applied to a 500Ω resistor on the positive comparator inputs. The threshold is I (Pin 11) • 4 • 500Ω.
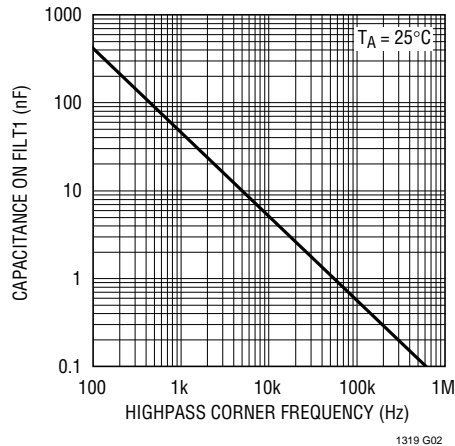
TYPICAL PERFORMANCE CHARACTERISTICS

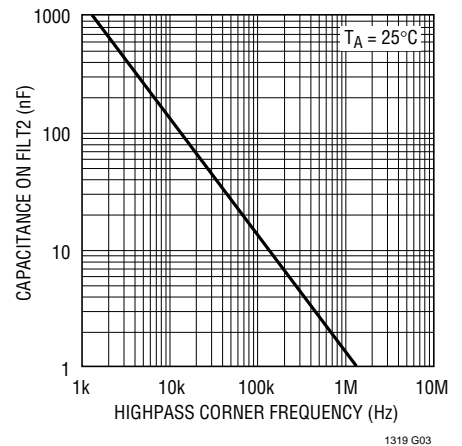**Preamp Frequency Response vs Input Capacitance**
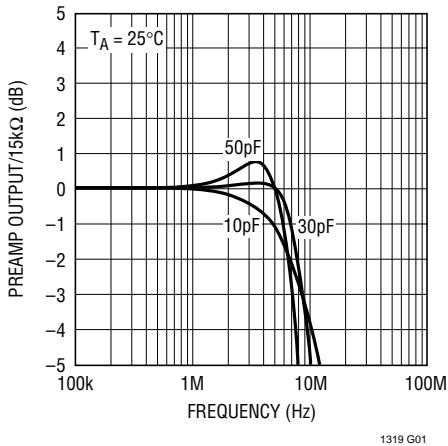
1319 G01

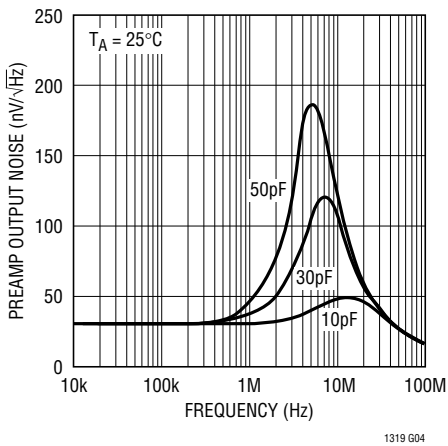**Preamp Highpass vs Capacitance on FILT1**

1319 G02

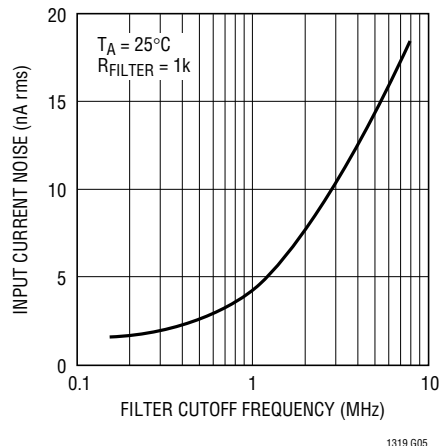**Gain Stage Highpass vs Capacitance on FILT2 or FILT2L**

1319 G03

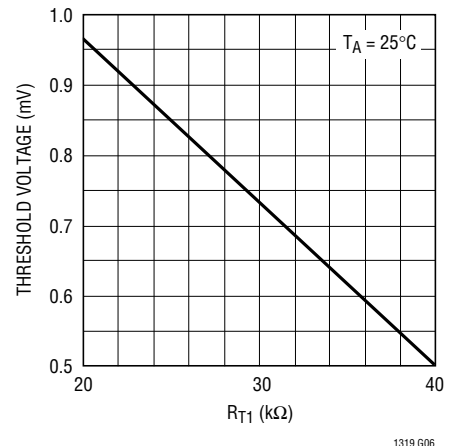**Preamp Output Noise vs Input Capacitance**

1319 G04

Input-Referred Noise vs Lowpass Filter on PREOUT

1319 G05

FILTIN- or FILTINL- Referred Threshold Voltage vs R_{T1}

1319 G06

CIRCUIT DESCRIPTION

The LT1319 is a general purpose low noise, high speed, high gain, infrared receiver designed to easily provide IR communications with portable computers, PDAs, desktop computers and peripherals. The receiver takes the photo-current from an infrared photodiode (Siemens BPW34FA or Temic BPV22NF) and performs a current-to-voltage conversion. After external filtering that is tailored for the desired communication standard, two filter buffers are provided. There are dual gain chains with nominal gain of 400V/V that feed internal comparators with hysteresis. The comparator thresholds are set externally with a current into the V_{TH} pin. The high frequency comparator has a response time of 25ns and is well-suited to high data rates.

The low frequency comparator responds in 60ns and is useful for more modest data rates such as Sharp/Newton and IRDA-SIR. The circuit also contains shutdown circuitry to reduce power consumption. Rejection of ambient interference is accomplished with AC coupling loops around the preamp and the two gain stages. The rejection frequency is set with an internal resistor and an external capacitor to ground. This feature allows changing of the break frequency by simply switching in additional capacitors. To aid in rejection of power supply noise there is internal supply regulation and a fully differential topology after the filter buffers.

LINEAR TECHNOLOGY

BLOCK DIAGRAM
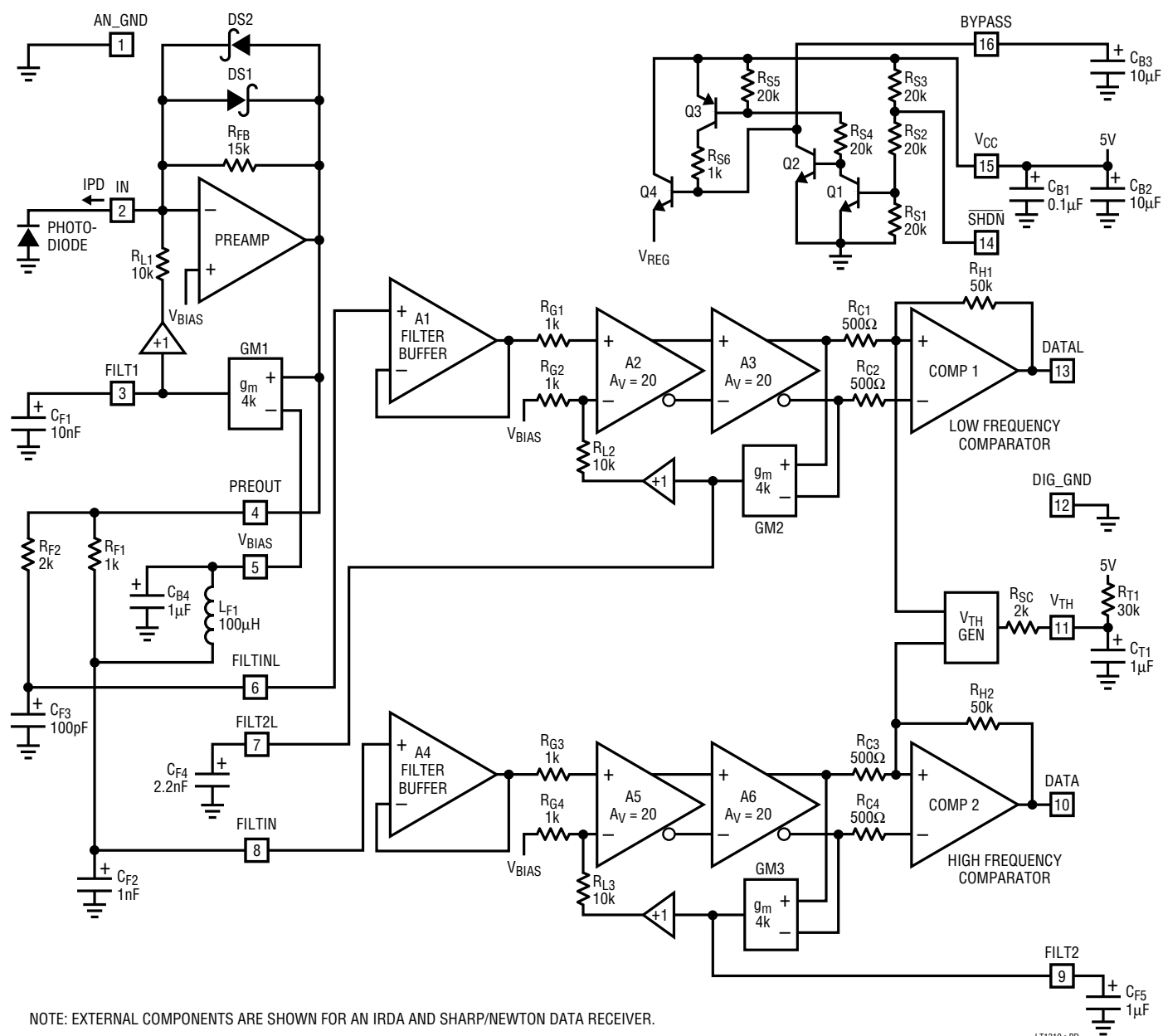
NOTE: EXTERNAL COMPONENTS ARE SHOWN FOR AN IRDA AND SHARP/NEWTON DATA RECEIVER.

LT1319 • BD

LT1319

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1319 requires careful layout techniques to minimize parasitic signal coupling to the preamp input. A sample board layout for the circuit on the first page is shown in the Typical Application section. The lead lengths on the photodiode must be as short as possible to Pin 2. Shielding is recommended over the entire circuit. A ground plane must be used and connected to Pin 1. The ground plane should extend under the package and surround Pins 1 to 9 and Pin 16. A single point connection should be made to the ground plane at Pin 12 (DIG_GND). The leads on Pins 6 and 8 should be short to prevent pickup into the gain stages. The comparator output leads (Pins 10 and 13) should be as short as possible to minimize coupling back to the input via parasitic capacitance.

Capacitance on Pin 10 should be minimized as the comparator output is pulled up by an internal 5k resistor. The associated digital circuitry should be located on the opposite side of the PC board from the LT1319 or separated as much as possible if on the same side of the board. Filter components should be located on the analog ground side of the package. Bypass capacitors should be used on Pins 5, 11, 15 and 16 for best supply rejection.

Preamp

The LT1319 preamp is a low noise, high speed current-to-voltage converter that has been optimized for an input capacitance of 30pF (which corresponds to the capacitance of the above-mentioned photodiodes with approximately 2V of back bias). A range of 0pF to 50pF is acceptable. The amplifier obtains high bandwidth by providing a low impedance input so that the input current is not filtered by the photodiode capacitance.

The dynamic range of the circuit will be limited at the low end by the input-referred current noise of the preamplifier and the desired signal-to-noise ratio. At the other extreme of the dynamic range for very large input signals, the output of the preamp is clamped by Schottky diodes across the feedback resistor.

The noise bandwidth is shaped by filtering at the output of the preamplifier and by the AC coupling loop. The input capacitance causes noise peaking for high bandwidth applications. Noise peaking can be explained by consider-

ing the voltage noise gain. Referring to the Block Diagram, at frequencies beyond the corner frequency of the AC coupling loop, the preamp is in a noise gain of 2.5 due to the ratio of $(R_{FB} + R_{L1})/R_{L1}$. At high frequencies the input capacitance approaches the same impedance as R_{L1} so the noise gain increases. For example, at 500kHz the 30pF input capacitance looks like 10.6kΩ which increases the noise gain to almost 4. The preamp is compensated to provide a flat current-to-voltage frequency response with a –3dB corner at 7MHz. The input current noise peaks up considerably if full bandwidth is used. To obtain best noise performance, the output of the preamp should be filtered to the minimum bandwidth required for the desired modulation scheme. The graph of input-referred noise versus lowpass filtering on the preamp output shows the noise penalty for higher bandwidths.

AC Coupling Loops

There are three AC loops in the circuit that reject low frequency inputs. The first loop is around the preamp and provides rejection of ambient light sources. The operation can be explained by looking at the Block Diagram. For low frequency signals the transconductance amplifier, GM1, compares the preamp output to the V_{BIAS} voltage. This differential voltage is transformed into a current that is fed into the high impedance node at Pin 3 and transformed back to a voltage. There is a voltage gain of approximately 60dB to this point which is then buffered to drive a 10k resistor that is connected back to the input of the preamp. This high gain loop attenuates the effect of low frequency signals by the amount of the loop gain times the ratio of R_{L1} to R_{FB} (i.e., 1000V/V • 15/10 = 1500). For higher frequencies the attenuation decreases due to the external capacitor on Pin 3. At frequencies beyond where the loop gain equals 10/15, signals are no longer attenuated. This high frequency cutoff is at:

$$f = (15/10)/(2\pi \bullet 4k\Omega \bullet C_{PIN3})$$

where $1/(4k\Omega)$ is the transconductance of the loop amplifier. For example, if $C_{PIN3} = 300pF$, the highpass frequency is 200kHz which can aid in rejection of a wide range of ambient interference.

The other two loops operate similarly around the gain stages and also provide low frequency rejection. In addi-

APPLICATIONS INFORMATION

tion, the loops around the gain stages provide an accurate DC threshold setting for the comparators. At DC, the loops force the differential voltages at the output of the gain stages to zero. The comparator threshold is set by the currents provided by the V_{TH} generator through the 500Ω resistors R_{C1} and R_{C3}. These currents are equal to 4 times the current into Pin 11. For 100μA into Pin 11, the comparator thresholds are nominally 200mV.

Power Supply Rejection and Biasing

The LT1319 has very high gain and bandwidth so great care is taken to reduce false output transitions due to power supply noise. As a first step the V_{CC} input is regulated down to approximately 4V to power all the analog sections of the circuit which are also tied to Analog Ground (Pin 1) as is the substrate of the die. Additionally, the internal 4V is bypassed at Pin 16. The digital circuitry (the comparators and shutdown logic) is powered directly off of V_{CC} and is returned to Digital Ground (Pin 12). To provide a clean bias point for the preamp, filter buffers and the gain stages, a 1.9V reference is generated from the 4V rail and is bypassed at Pin 5. The gain stages are pure differential designs which inherently reject supply variations.

Filtering

Filtering is needed for two main reasons: sensitivity and ambient rejection. Lowpass filtering is needed to limit the bandwidth in order to minimize the noise. Low noise permits reliable detection of smaller input signals over a larger distance. Highpass filtering is used to reject interfering ambient signals. Interference includes low frequency sources of infrared light such as sunlight, incandescent lights, and ordinary fluorescent lights, as well as high frequency sources such as TV remote controls (40kHz) and high frequency fluorescent lighting (40kHz to 80kHz).

The circuit topology allows for filtering between the preamplifier and the filter buffers as well as filtering with the three internal highpass loops. With two channels the filtering can be optimized for different modulation schemes. The high speed channel (with a 25ns comparator) is ideal for modulation schemes using frequencies above 1MHz. Carrier-based methods as well as narrow pulse schemes can have superior ambient rejection by adding in a dedicated high-

pass filter network. The application on the first page of the data sheet is repeated in the Block Diagram and can be used to illustrate the filtering for IRDA-SIR and Sharp/Newton. The preamp highpass zero is set by GM1 and C_{F1}. The break frequency is located at:

$$f = (15k\Omega/10k\Omega)/(2\pi \bullet 4k\Omega \bullet 10nF) = 6kHz$$

On the low speed channel there is a lowpass filter at 800kHz set by R_{F2} and C_{F3}. The gain stage has a highpass filter set by GM2 and C_{F4} at approximately 500kHz. The high speed channel has an LC tank circuit at 500kHz with Q = 3 set by R_{F1}. The high speed gain stage has a highpass characteristic set by GM3 and C_{F5} with a break frequency of 1.1kHz. These filters are suitable for the 1.6μs pulses and up to 115kBd data rates of IRDA-SIR on the slow channel. The fast channel is used for Sharp/Newton ASK Modulation with 500kHz bursts at data rates up to 38.4kBd.

A second circuit is shown in the Typical Applications section for IRDA SIR/FIR and Sharp. This circuit is Demo Board 54. The first filter is a preamp highpass loop set at 600Hz by C_{F7} for IRDA or 180kHz by C_{F1} for Sharp. Sharp modulation is run on the low speed channel and is next filtered by a tank circuit formed by R_{F2}, L_{F1} and C_{F3} and centered at 500kHz. L_{F1} also provides the DC bias for the filter buffer input. A final highpass for the lower speed channel is set by C_{F4} at 130kHz. The high speed channel is used by IRDA SIR and FIR which use 1.6μs and 220ns wide pulses. A lowpass formed by R_{F1} and C_{F2} limit the noise bandwidth. The final highpass is set by C_{F5} (2.5MHz for FIR) or C_{F6} (450kHz). The squelch circuit formed by Q1, Q2, Q3 and R_{C1} to R_{C6} extends the short range performance and will be discussed later.

In designing custom filters for different applications, the following guidelines should be used.

1. Limit the noise bandwidth with a lowpass filter that has a rise time equal to half the pulse width. For example, for 1μs pulses a 700kHz lowpass filter has a 10% to 90% rise time of 0.35/700kHz = 500ns.

2. Limit the maximum highpass to 1/(4 $\bullet$ pulse width). For 1μs pulses, 1/4μs = 250kHz.

3. In setting the highpass filters, space the filters apart by a factor of 5 to 10 to reduce overshoot due to filter

APPLICATIONS INFORMATION

interaction. Overshoot becomes especially important for high input levels because it can cause false pulses which may not be tolerated in certain modulation schemes. It is also more of a problem in modulation schemes such as IRDA-SIR and FIR where the duty cycle can get very low (i.e., transmitting data with lots of ones which are signaled with the absence of pulses). AC coupled receivers when faced with low duty cycle data set their thresholds close to the baseline DC level of the data stream which converts small overshoots into erroneously received pulses.

4. As a general rule, place the lowest frequency highpass around the preamp and the highest highpass around the gain stage or between the preamp and gain stage. The reason for this is again due to high signal levels where there can be slow photocurrent tails. The tail response can be filtered out by high enough frequency filters.

5. In all cases with custom filtering, or when modifying one of the applications presented in this data sheet, try the system over the full distance range with a full range of duty cycle data streams. Modulation methods with fixed or limited duty cycle are superior because they have little or no data dependent problems.

Dynamic Range

The calculation of dynamic range can only be made in the context of a specific modulation scheme and with the system variations taken into account. The required information includes: minimum signal-to-noise ratio (or BER, Bit Error Rate requirement), photodiode capacitance at 1.9V back bias, preamp noise spectrum, preamp output filtering, AC loop cutoff frequencies, modulation method, demodulation method including allowable pulse widths and the effect of missing or extra pulses, photodiode rise and fall times, and ambient interference. The best solution is to experimentally determine the maximum and minimum distances at which a desired BER is obtained. This measure of dynamic range is more meaningful in terms of the overall system than any analytic solution.

Using the IRDA-SIR modulation scheme as an example, however, we can illustrate how some limits on the required receiver/photodiode combination can be obtained. The minimum light intensity in the angular range is 40mW/sr

which translates to a photodiode current as follows (using the BPW34FA data sheet specs):

$$I_{PD(MIN)} = \left(40mW/sr\right)\left(\frac{7mm^2}{\left(1000mm\right)^2}\right) \bullet$$
$$\left(0.65A/W\right)\left(0.95\right)\left(0.95\right) = 164nA$$

The $7mm^2$ term is the photodiode area. The 1000mm is the distance from the light source. The 0.65A/W is the spectral sensitivity at 880nm wavelength. The first 0.95 term is the relative sensitivity at 850nm wavelength and the second term is the sensitivity at 15° off axis. Similar calculations are detailed in the Infrared Data Association Serial Infrared (SIR) Physical Layer Link Specification, version 1.0. This minimum photocurrent implies that the input-referred noise current of the receiver be less than 13.7nA rms for a bit error rate of 1E-9. With an 800kHz lowpass filter on the preamp output the LT1319 has approximately 3.6nA rms of input-referred current noise. The maximum photodiode current at 20mm, on-axis with 500mW/sr intensity:

$$I_{PD(MAX)} = \left(500mW/sr\right)\left(\frac{7mm^2}{\left(20mm\right)^2}\right) \bullet$$
$$\left(0.65A/W\right)\left(0.95\right) = 5.4mA$$

so we see that the dynamic range requirement is 90.4dB. What is not obvious, however, is that the photodiode output current is not simply a pulse of current, there is a significant tail at high current levels that has a time constant of more than 1μs which can cause distortion in the output pulse width of the LT1319. This tail can be shown in the following photograph which shows the voltage across a 5k resistor that is connected between the anode of a photodiode and ground. The cathode of the photodiode is connected to 2V. There is a 2pF Schottky diode across the resistor to clamp the voltage swing to less than 0.5V. With about 30pF photodiode capacitance and 10pF for an oscilloscope probe, any tail observed with a time constant greater than 210ns is due to decaying photocurrent. The

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first trace in the photograph shows the current with the photodiode 10cm from a source with 100mW/sr intensity. At 200mV/div, there is about 40µA of peak current and the decay is consistent with the 210ns time constant. The lower trace shows the current with the photodiode 2cm from the LEDs where the photodiode current is theoretically 25 times greater than at 10cm. The voltage is clamped by the photodiode to nearly 0.4V, but what is now noticeable is that there is a tail with a time constant a bit greater than 1µs. If the signal is AC coupled and has a low duty cycle, the waveform will be centered at the very bottom which can result in very wide output pulses. This issue will be discussed later in more detail and a method to circumvent it will be shown.

Photocurrent Waveforms

1319 AI01
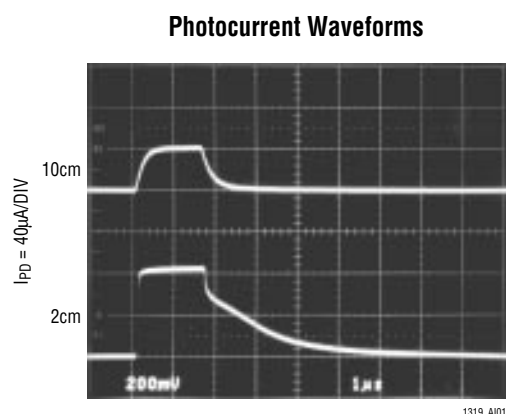
Threshold Adjustment

The comparator thresholds are set by the current into Pin 11. The simplest method of setting this current is by a resistor, R_{T1} tied between Pin 11 and Pin 15 (V_{CC}). Pin 11 should be bypassed. The current is given by:

$$I_{TH} = \frac{\left(V_{CC} - 0.9V\right)}{\left(R_{T1} + 2k\Omega\right)}$$

The threshold referred to the input of the filter buffer is:

$$V_{TH} = \frac{I_{TH} \cdot 4 \cdot 500\Omega}{400V/V}$$

or nominally 0.68mV for R_{T1} = 30k. The largest practical value of R_{T1} is 39k. The limitation tends to be switching transients at the comparator outputs parasitically coupling to the FILTIN or FILTINL inputs and is layout dependent.

Extending Short Range Performance

The short range performance of the LT1319 is normally limited by the photocurrent tail, but in some instances the peak current level cannot be supported by the output of the preamplifier and the input will sag at Pin 2. Typically the maximum input current is 6mA. To increase this current to 20mA or more, place an NPN transistor with its emitter tied to Pin 2, the base to Pin 4 and collector to the 5V supply. The choice of transistor is dependent on the bandwidth required for the preamp. The base-emitter capacitance of the transistor (C_{JE}), is in parallel with the 15k feedback resistor of the preamplifier and performs a lowpass filtering function. For modest data rates such as IRDA-SIR and Sharp/Newton a 2N3904 limits the bandwidth to 2MHz which is ample. For the highest data rates, a transistor with f_T greater than 1GHz is needed such as MMBR941LT1.

Another issue with large input signals is the photocurrent tail. When this tail is AC coupled and the data has a low duty cycle, the output pulse width can become so wide that it extends into the next bit interval. A highpass filter can reject this tail, but for the case of IRDA-SIR, rejecting the 1µs time constant can cause rejection of the 1.6µs pulse which leads to a loss of sensitivity and reduced maximum link distance. The circuit on the front page of the data sheet uses a 500kHz highpass that trades off some sensitivity for rejection of this tail. Unfortunately both maximum and minimum distance are compromised. An alternative is shown in the IRDA-SIR/FIR application. In this instance the final highpass filter for SIR is moved into 450kHz, but a clamp/squelch circuit consisting of Q1, Q2, D3 and R_{C1} to R_{C6} is added. Q1 is used as described above to clamp the input, but the input current level at which the clamp engages has been modified by R_{C1} and R_{C2}.

Without the resistors, Q1 would turn on when the voltage across the 15k resistor in the preamp reaches about 0.7V (a current of 0.7V/15kΩ = 47µA). The drop across R_{C1} reduces this voltage by about 365mV. The drop is set by the

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current through R_{C2} which is $[V_{CC} - (V_{BIAS} + 0.365V)]/15k\Omega = 182\mu A$ where $V_{BIAS} = 1.9V$. At this new level $(0.335V/15k\Omega = 22.3\mu A)$, Q1 turns on which clamps the preamp output. The collector current of Q1 provides base drive for Q2 which saturates and pulls its collector close to 5V. The FILT1, FILT2L and FILT2 inputs are now pulled positive by R_{C3}, R_{C4} and R_{C6} which forces an offset at the inputs to the gain stages and preamp. Referring to the Block Diagram, pulling FILT2L or FILT2 positive a voltage ΔV provides a voltage of $\Delta V/11$ at the inverting input of the first gain stage. This offset effectively cuts off a portion of the tail at high input levels. The magnitude of ΔV is set by the value of R_{C3}, the current sinking capability of the transconductance stages (100μA), the value of C_{F4},C_{F5} and the duty cycle of the data pulses. Likewise an offset of $\Delta V/10k\Omega$ is created at the preamp input to reduce tail current contributions.

LED Drive Circuits

There are several simple circuits for driving LEDs. For low speed modulation methods such as IRDA-SIR and Sharp/Newton with pulses over 1μs, a 2N3904 in a SOT-23 package can be used as a switch with a series resistor in the collector to limit the current drive. This circuit is shown below with a suggested limiting resistor of 16Ω which typically sets the current at 200mA. The supply voltage must be well bypassed at the connection to the LED in order for the supply not to sag when hit with a fast current pulse. A 10μF low ESR capacitor should be used as well as a 0.1μF

RF quality capacitor to reduce the high frequency spikes. The current must be selected to achieve the minimum output light intensity at a given angle and must be lower than the manufacturer's maximum current rating at the maximum duty cycle of the modulation method. The optimum current is a function of the LED output, the LED forward voltage, the drop across the transistor and the minimum supply voltage.

$$I_{LED} = \frac{\left(V_{CC} - V_{LED} - V_{SW}\right)}{R_{SERIES}}$$

The minimum light output then can be obtained from the LED data sheet. For IRDA-SIR the minimum intensity at 15° off axis is 40mW/sr. For IRDA-FIR the spec rises to 100mW/sr. To increase light output and distance of the link, a second LED can be inserted in series with the first to obtain twice the light output without consuming additional supply current. The current variation will now be greater because two LED forward drops must be accounted for and the drop across the series resistor is greatly reduced.

For pulse widths less than 500ns the NPN should be replaced by an N-channel MOSFET with on-resistance of less than 1Ω with 5V on the gate. The FET can turn off much more quickly than the saturated NPN and provides a lower effective on-resistance. A suggested circuit is shown below and includes three devices available in the SOT-23 package.
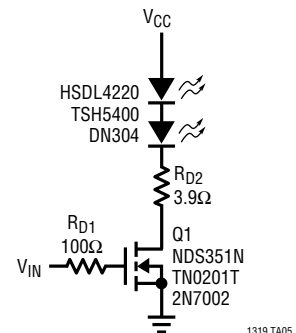
TYPICAL APPLICATIONS

Optional Clamp Circuit
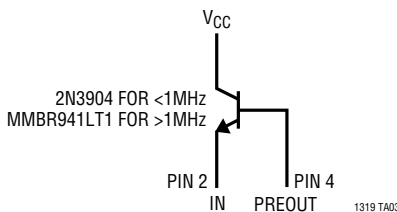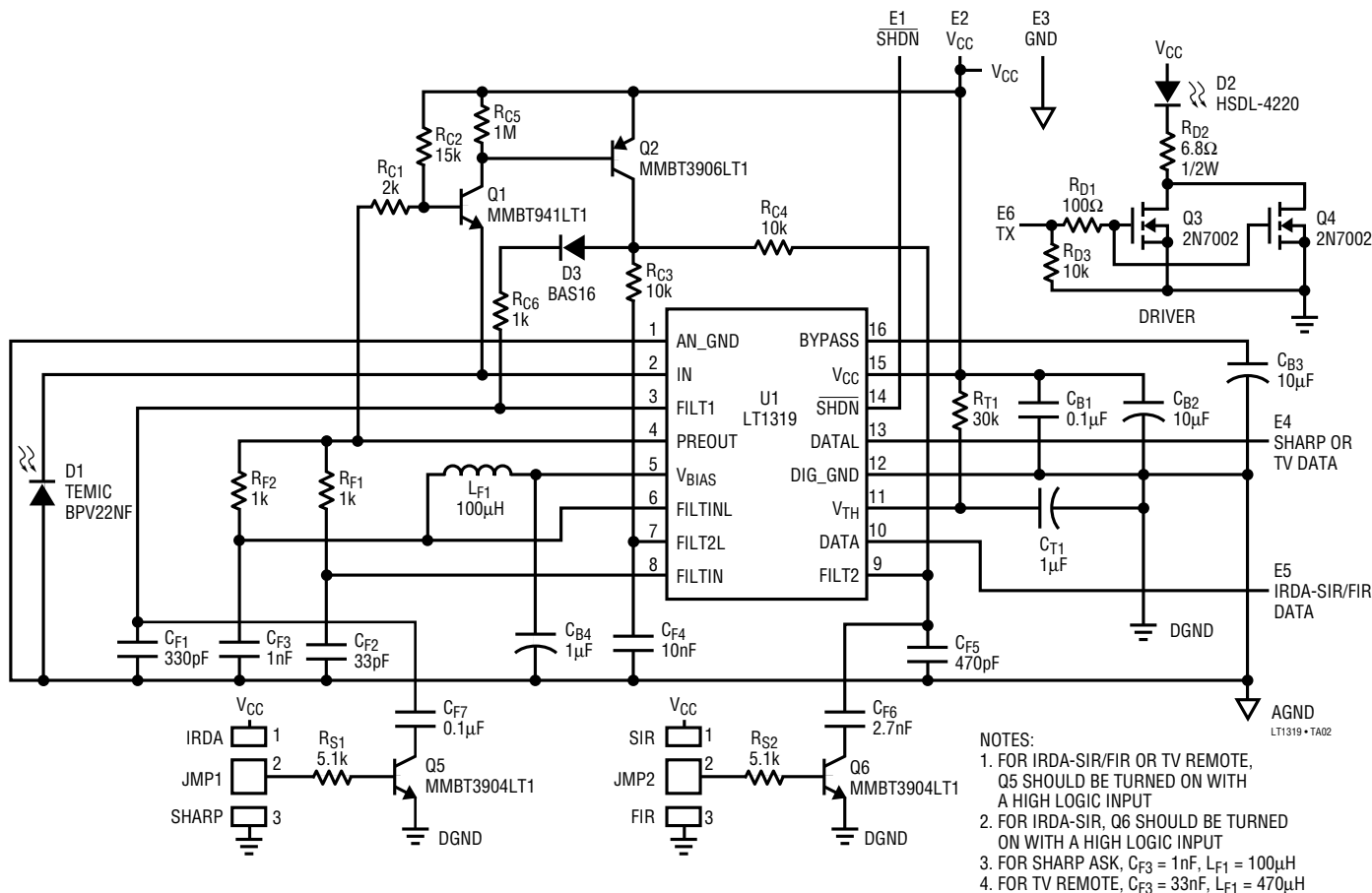

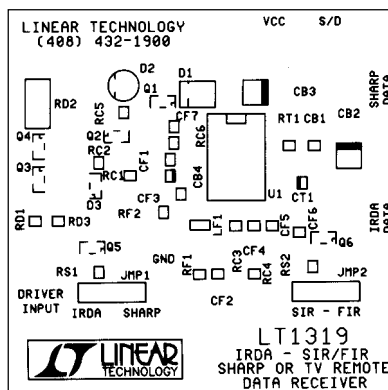**LED Drive Circuit for IRDA-SIR and Sharp/Newton**
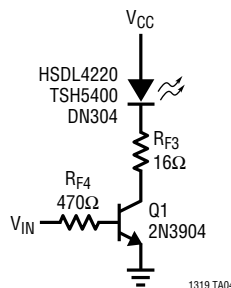
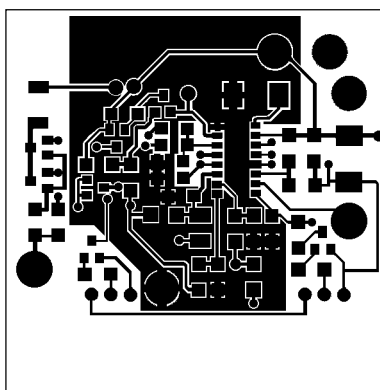**2 LED Drive Circuit for IRDA-FIR**

TYPICAL APPLICATIONS

IRDA-SIR/FIR and Sharp or TV Remote Data Receiver

NOTES:
1. FOR IRDA-SIR/FIR OR TV REMOTE, Q5 SHOULD BE TURNED ON WITH A HIGH LOGIC INPUT
2. FOR IRDA-SIR, Q6 SHOULD BE TURNED ON WITH A HIGH LOGIC INPUT
3. FOR SHARP ASK, C_{F3} = 1nF, L_{F1} = 100µH
4. FOR TV REMOTE, C_{F3} = 33nF, L_{F1} = 470µH
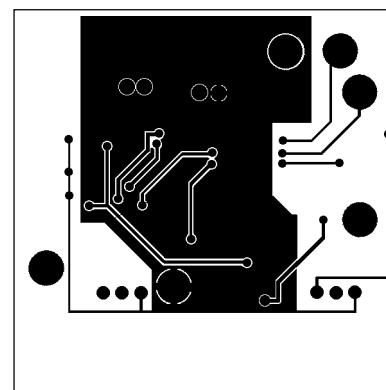
LT1319 • TA02

PC Board Layout for IRDA-SIR/FIR and Sharp or TV Remote Data Receiver
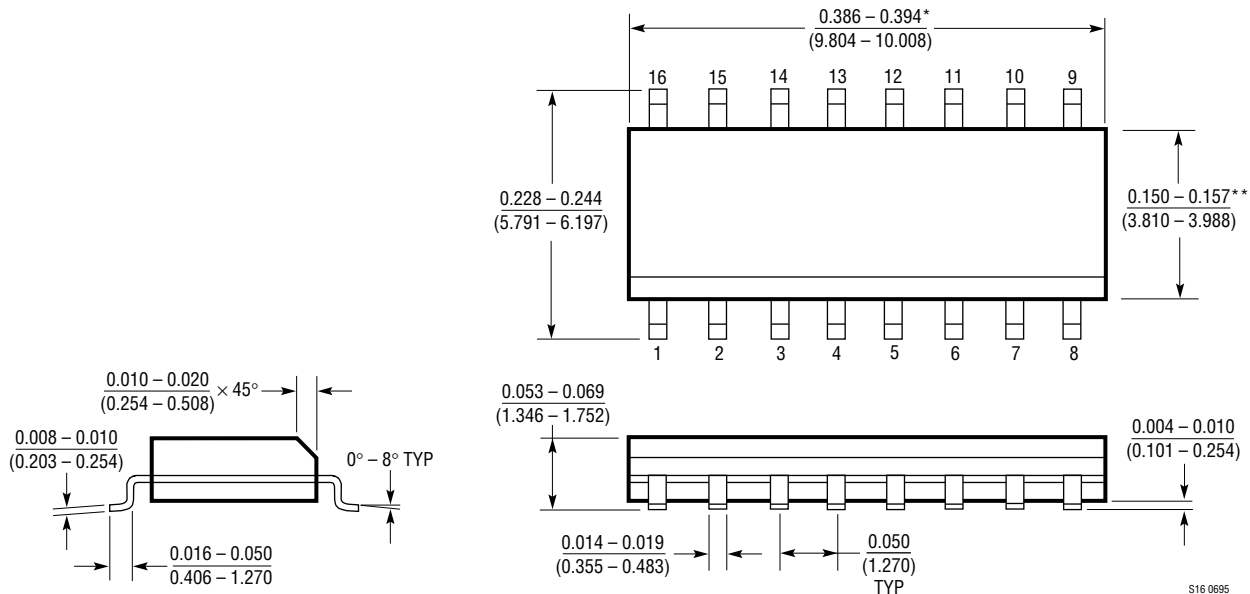
COMPONENT   TOP   BOTTOM

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

0.386 – 0.394*
(9.804 – 10.008)

16 15 14 13 12 11 10 9

0.228 – 0.244
(5.791 – 6.197)

0.150 – 0.157**
(3.810 – 3.988)

1 2 3 4 5 6 7 8

0.010 – 0.020
(0.254 – 0.508) × 45°

0.008 – 0.010
(0.203 – 0.254)

0° – 8° TYP

0.016 – 0.050
0.406 – 1.270

0.053 – 0.069
(1.346 – 1.752)

0.004 – 0.010
(0.101 – 0.254)

0.014 – 0.019
(0.355 – 0.483)

0.050
(1.270)
TYP

S16 0695

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1113	Dual, Low Noise Precision JFET Input Op Amp	4.5nV/$\sqrt{Hz}$ Input Voltage Noise
LT1169	Dual, Low Noise Picoampere Bias Current Op Amp	JFET Input, 10pA Max
LT1222	Low Noise, High Speed Op Amp ($A_V \geq 10$)	500MHz Gain Bandwidth, External Comp Pin