Single Chip 12-Bit Data Acquisition Systems

FEATURES

- Built-In Sample-and-Hold
- **Single Supply 5V Operation**
- 60kHz Maximum Throughput Rate (LTC1292)
- **Power Shutdown After Each Conversion (LTC1297)**
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- Analog Inputs Common Mode to Supply Rails

KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 12µs Max Over Temp
- Low Supply Current: 6.0mA
- Shutdown Supply Current: 5µA (LTC1297)

DESCRIPTION

The LTC1292/LTC1297 are data acquisition systems that contain a 12-bit, switched-capacitor successive approximation A/D, a differential input, sample-and-hold on the (+) input, and serial I/O. When the LTC1297 is idle between conversions it automatically powers down reducing the supply current to 5µA, typically. The LTC1292 is capable of digitizing signals at a 60kHz rate and with the device's excellent AC characteristics, it can be used for DSP applications. All these features are packaged in an 8-pin DIP and are made possible using LTCMOS™ switched-capacitor technology.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three wires. Because of their accuracy, ease of use and small package size these devices are well suited for digitizing analog signals in remote applications where minimum number of interconnects and power consumption are important.

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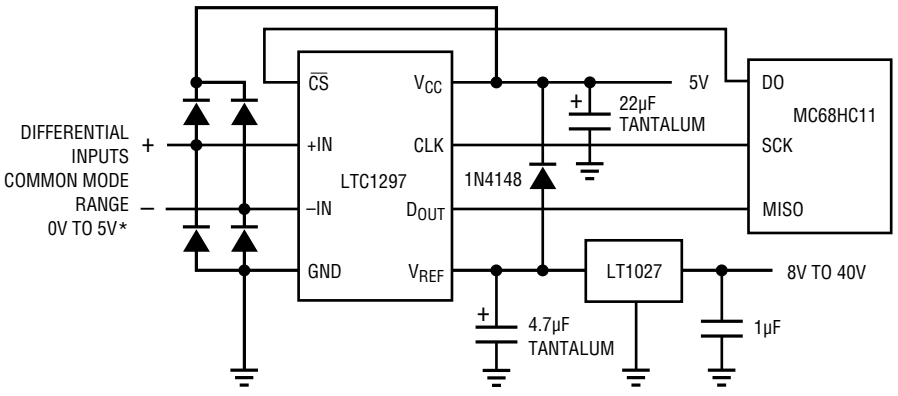
TYPICAL APPLICATION

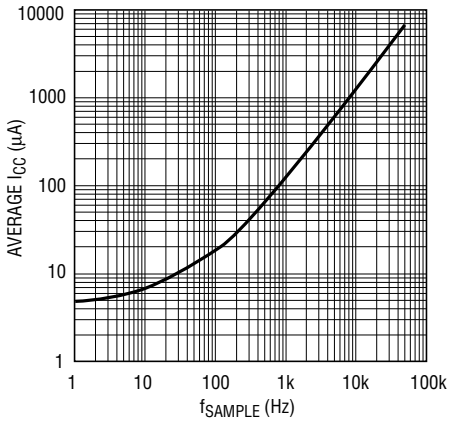
12-Bit Differential Input Data Acquisition System



*FOR OVERVOLTAGE PROTECTION LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN ANY INPUT IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

LTC1292/7 TA01

Power Supply Current vs Sampling Frequency



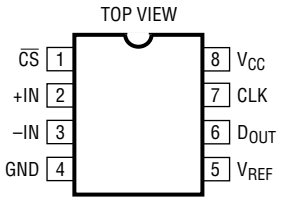
LTC1297• TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference
    Inputs ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1292/LTC1297BC, LTC1292/LTC1297CC,
  LTC1292/LTC1297DC ..... 0°C to 70°C
  LTC1292/LTC1297BI, LTC1292/LTC1297CI,
  LTC1292/LTC1297DI ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} =100°C/W (J8)
T_{JMAX} = 100°C, θ_{JA} =130°C/W (N8)

ORDER PART NUMBER	
LTC1292BIN8	LTC1297BIN8
LTC1292CIN8	LTC1297CIN8
LTC1292DIN8	LTC1297DIN8
LTC1292BCJ8	LTC1297BCJ8
LTC1292CCJ8	LTC1297CCJ8
LTC1292DCJ8	LTC1297DCJ8
LTC1292BCN8	LTC1297BCN8
LTC1292CCN8	LTC1297CCN8
LTC1292DCN8	LTC1297DCN8

For Military Temperature Ranges please contact factory.

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1292B LTC1297B MIN	TYP	MAX	LTC1292C LTC1297C MIN	TYP	MAX	LTC1292D LTC1297D MIN	TYP	MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Note 4 & 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±0.5			±1.0			±4.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed					12			12			12	Bits
Analog and REF Input Range	(Note 7)	●			−0.05V to V_{CC} + 0.05V							V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		(Note 9)		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence LTC1292 LTC1297			1.5CLK 0.5CLK+5.5µs		
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6) LTC1292 LTC1297			 14CLK+2.5µs 14CLK+6µs		
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓				130		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before CLK↑ (LTC1297 Wakeup Time)	V_{CC} = 5V (Note 6) LTC1292 LTC1297		50 5.5			ns µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V (Note 6) LTC1292 LTC1297		2.5 0.5			µs µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6) LTC1292 LTC1297		14CLK 14CLK+5.5µs			
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA I_O = 360µA	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			20		mA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1292B/LTC1297B LTC1292C/LTC1297C LTC1292D/LTC1297D MIN	TYP	MAX	UNITS
I_{CC}	Positive Supply Current	$\overline{CS}$ High	LTC1292	●		6	12	mA
		$\overline{CS}$ Low	LTC1297	●		6	12	mA
		$\overline{CS}$ High Power Shutdown CLK Off	LTC1297BC, LTC1297CC, LTC1297DC	●		5	10	µA
			LTC1297BI, LTC1297CI, LTC1297DI LTC1297BM, LTC1297CM, LTC1297DM	●		5	15	µA
I_{REF}	Reference Current	$\overline{CS}$ High		●		10	50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, V_{REF} = 5V, CLK = 1.0MHz unless otherwise specified.

Note 4: One LSB is equal to V_{REF} divided by 4096. For example, when V_{REF} = 5V, 1LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

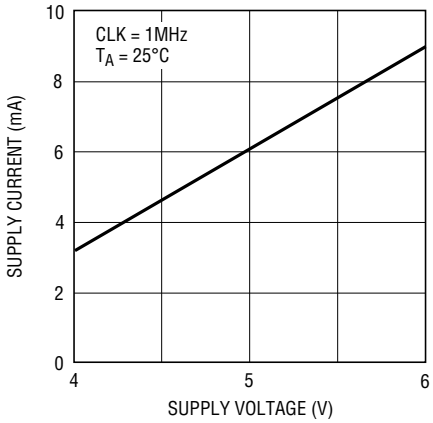
Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 125kHz$ at 125°C, $f_{CLK} \geq 31kHz$ at 85°C, and $f_{CLK} \geq 3kHz$ at 25°C.

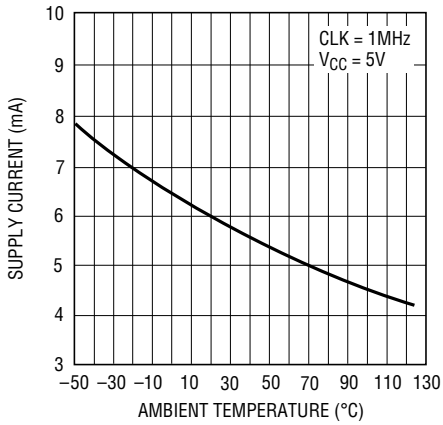
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



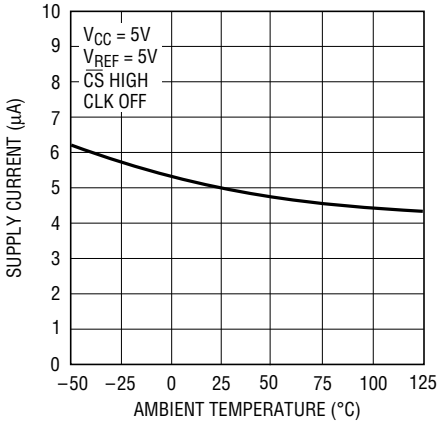
LTC1292/7 G01

Supply Current vs Temperature



LTC1292/7 G02

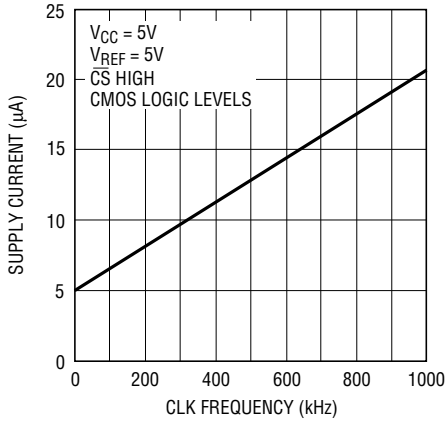
LTC1297 Supply Current (Power Shutdown) vs Temperature



LTC1292/7 G03

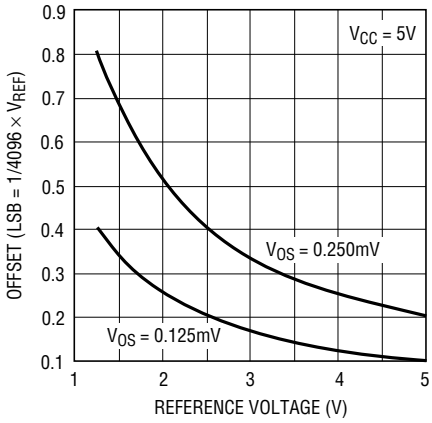
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1297 Supply Current (Power Shutdown) vs CLK Frequency



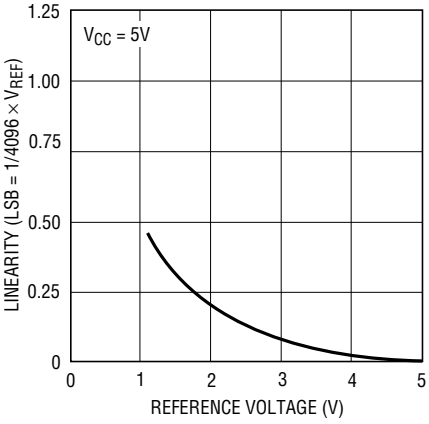
LTC1292/7 G04

Unadjusted Offset Voltage vs Reference Voltage



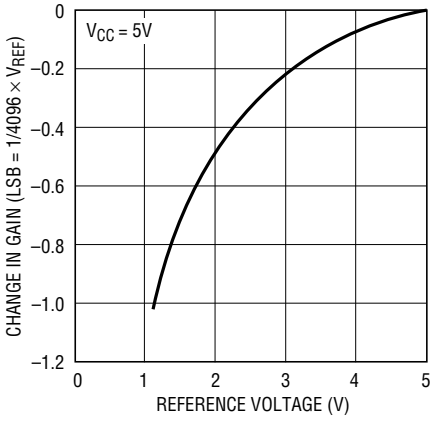
LTC1292/7 G05

Change in Linearity vs Reference Voltage



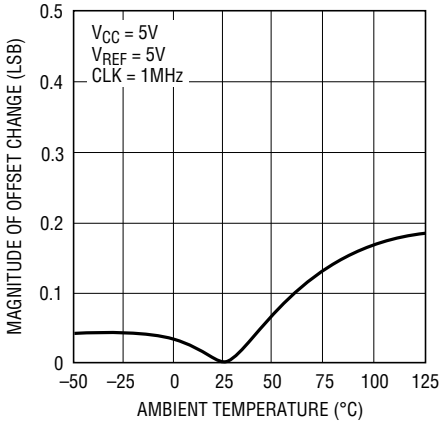
LTC1292/7 G06

Change in Gain vs Reference Voltage



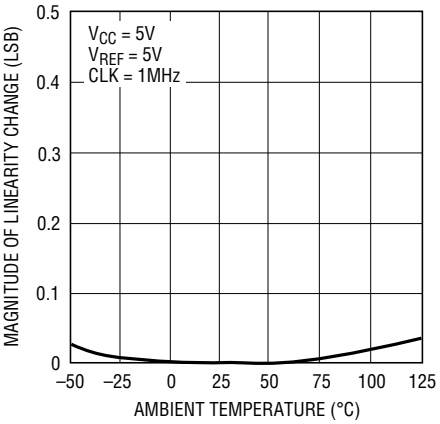
LTC1292/7 G07

Change in Offset vs Temperature



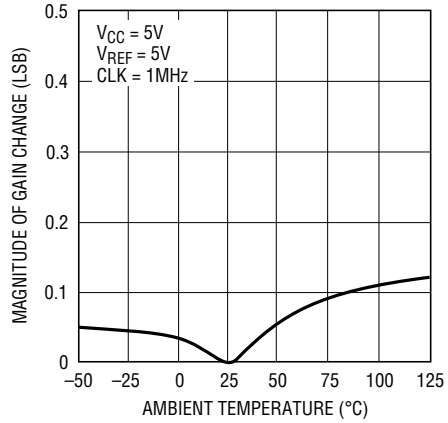
LTC1292/7 G08

Change in Linearity vs Temperature



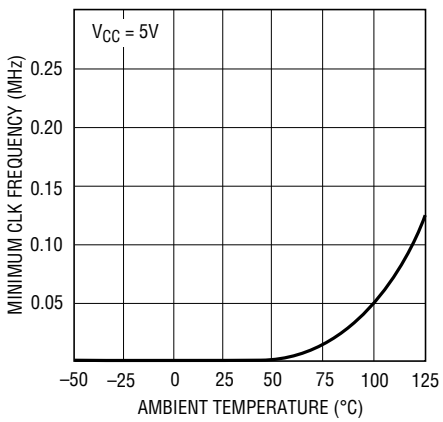
LTC1292/7 G09

Change in Gain vs Temperature



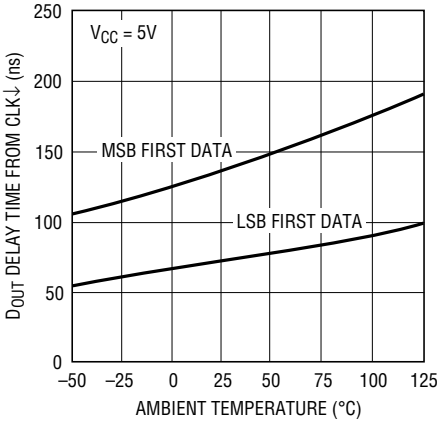
LTC1292/7 G10

Minimum Clock Rate for 0.1 LSB Error*



LTC1292/7 G11

D_{OUT} Delay Time vs Temperature

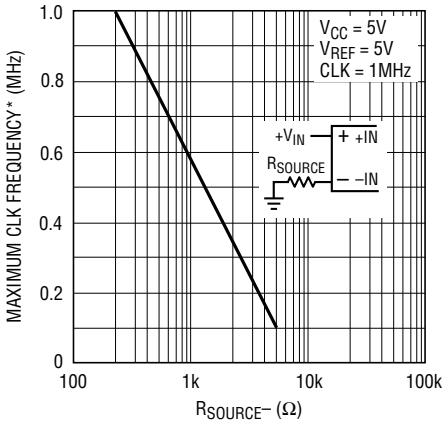


LTC1292/7 G12

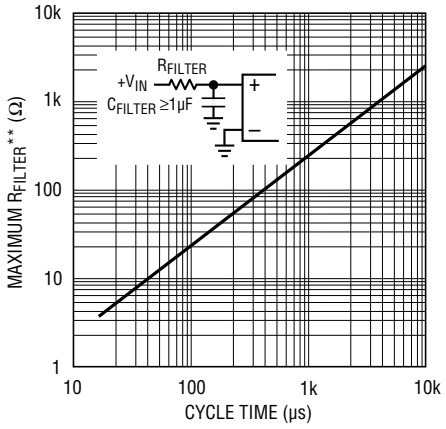
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED (NOTE 9).

TYPICAL PERFORMANCE CHARACTERISTICS

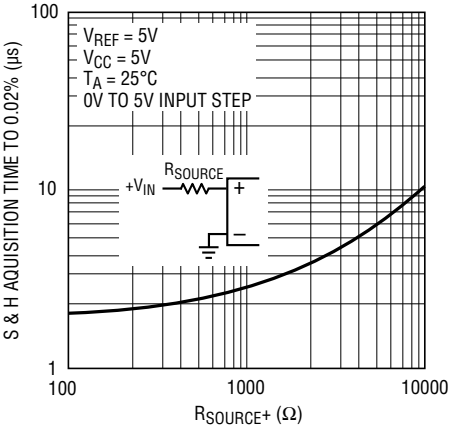
Maximum Clock Rate vs Source Resistance



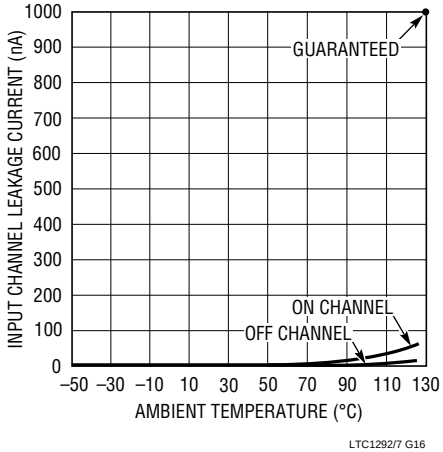
Maximum Filter Resistor vs Cycle Time



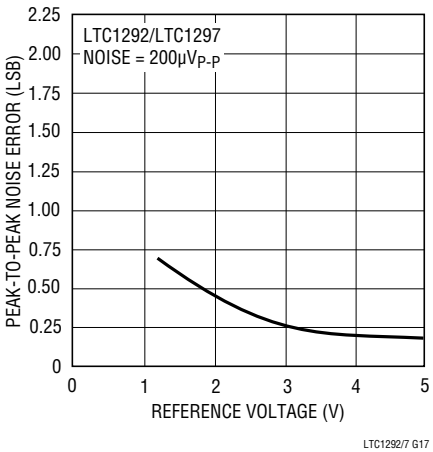
Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



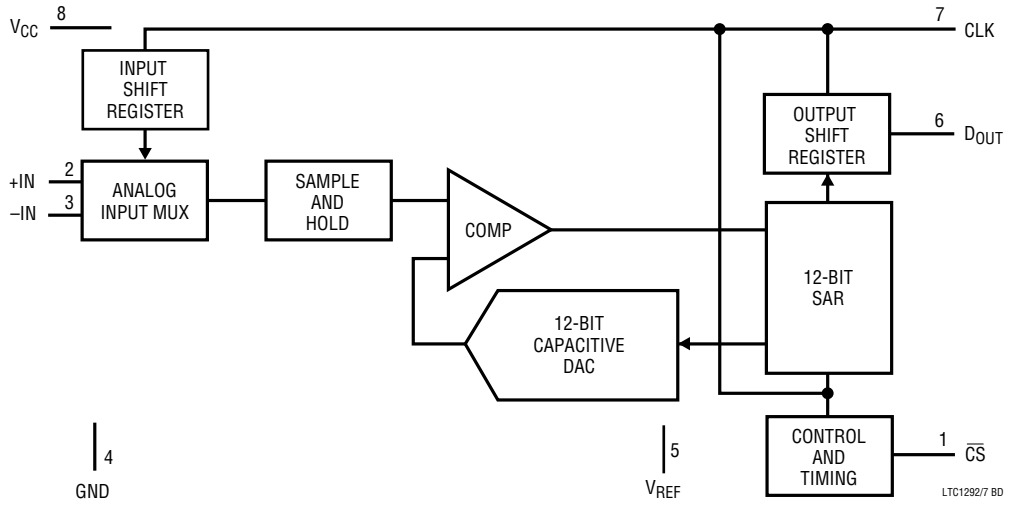
* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT $R_{FILTER} = 0\Omega$ IS FIRST DETECTED.

PIN FUNCTIONS

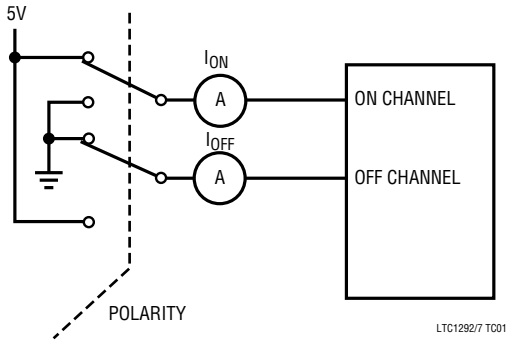
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1292/LTC1297. Power shutdown is activated on the LTC1297 when $\overline{CS}$ is brought high.
2, 3	+IN, –IN	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	V_{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

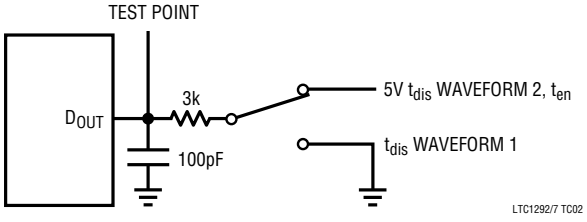


TEST CIRCUITS

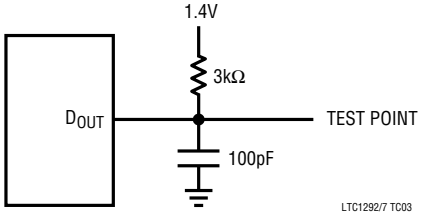
On and Off Channel Leakage Current



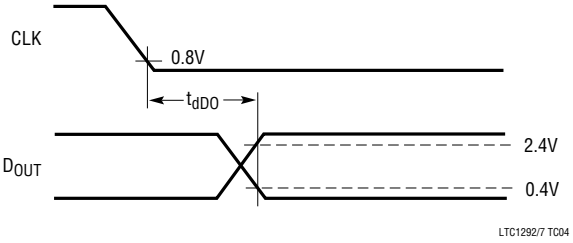
Load Circuit for t_{dis} and t_{en}



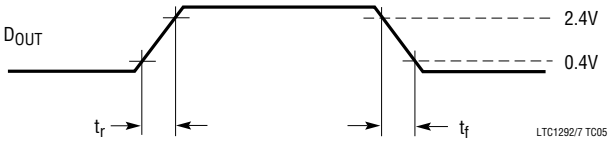
Load Circuit for t_{dDO}, t_r and t_f



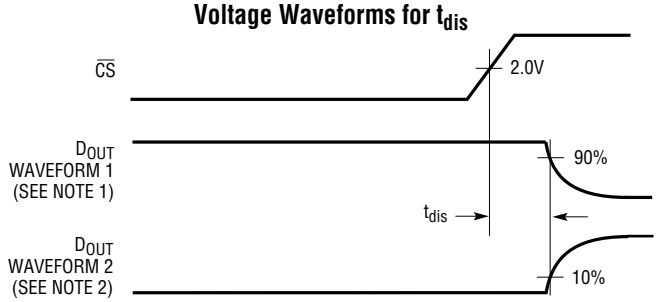
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

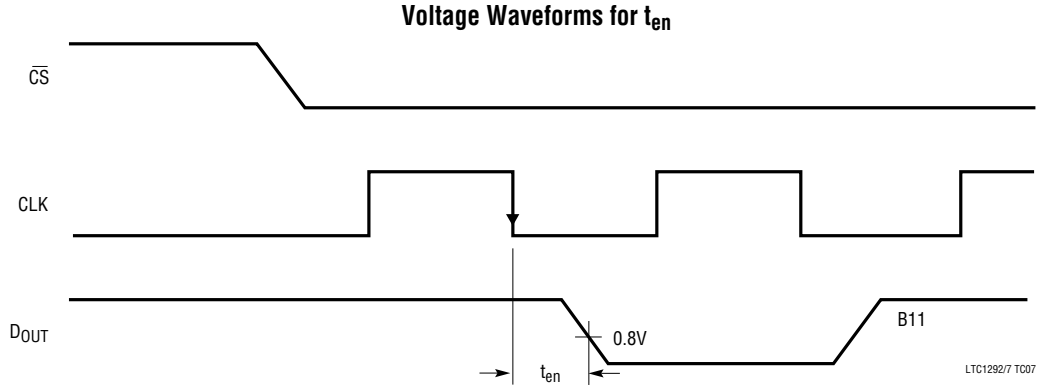


Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS



APPLICATIONS INFORMATION

The LTC1292/LTC1297 are data acquisition components which contain the following functional blocks:

1. 12-Bit Succesive Approximation Capacitive A/D Converter
2. Differential Input
3. Sample-and-Hold (S/H)
4. Synchronous, Half-Duplex Serial Interface
5. Control and Timing Logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1292/LTC1297 communicate with microprocessors and other external circuitry via a synchronous, half-duplex, three-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge. The LTC1292/LTC1297 do not require a configuration input word and have no D_{IN} pin. They are permanently configured to have a single differential input and to perform a unipolar conversion. A falling $\overline{CS}$ initiates data transfer. To allow the LTC1297 to recover from the power shutdown mode, $t_{su\overline{CS}}$ has to be met. Then the first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line with a MSB-first sequence followed by a LSB-first sequence. With the half-duplex serial interface the D_{OUT} data is from the current conversion. This provides easy interface to MSB-first or LSB-first serial ports. Bringing $\overline{CS}$ high resets the LTC1292/LTC1297 for the next data exchange and puts the LTC1297 into its power shutdown mode.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1292/LTC1297**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

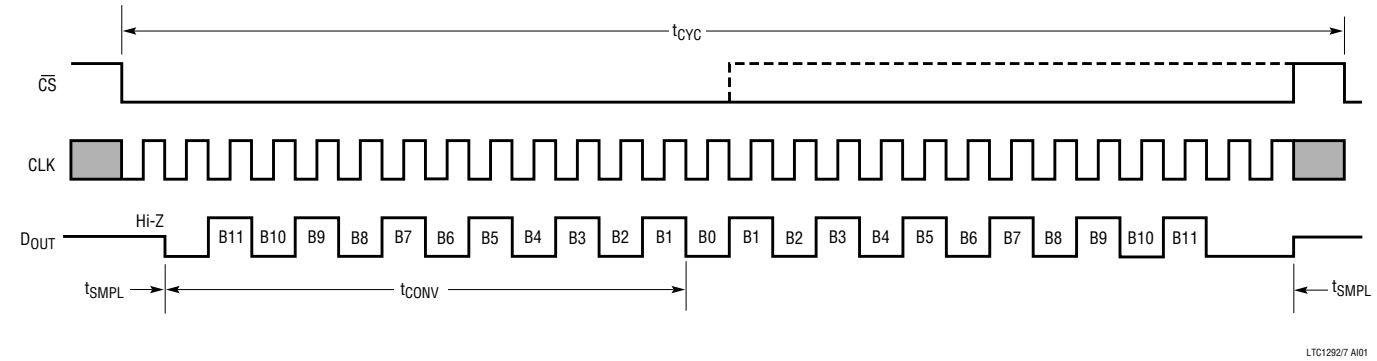
* Requires external hardware

** Contact factory for interface information for processors not on this list

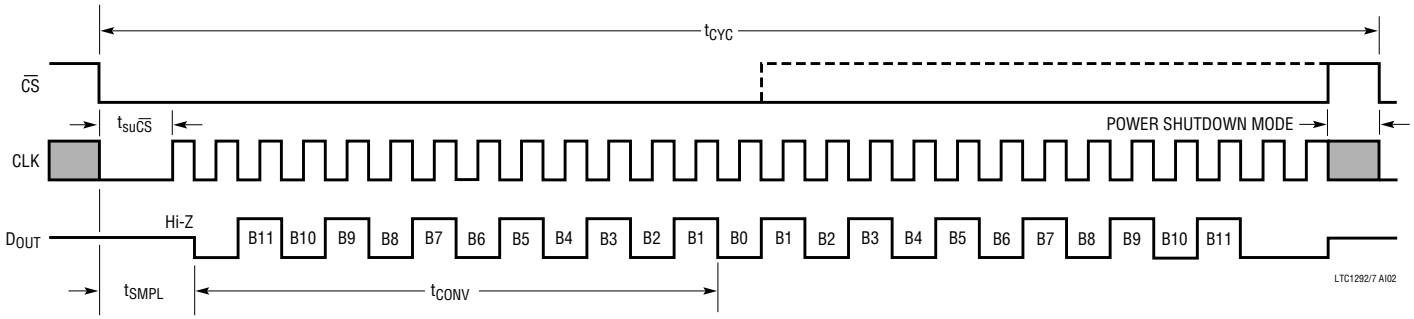
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

LTC1292 Operating Sequence



LTC1297 Operating Sequence



Microprocessor Interfaces

The LTC1292/LTC1297 can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1292/LTC1297. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. A dummy D_{IN} word sent to the data register starts the SPI process. With two 8-bit transfers, the A/D result is read into the MPU (Figure 1). For the LTC1292 the first 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits B7 through B0 into

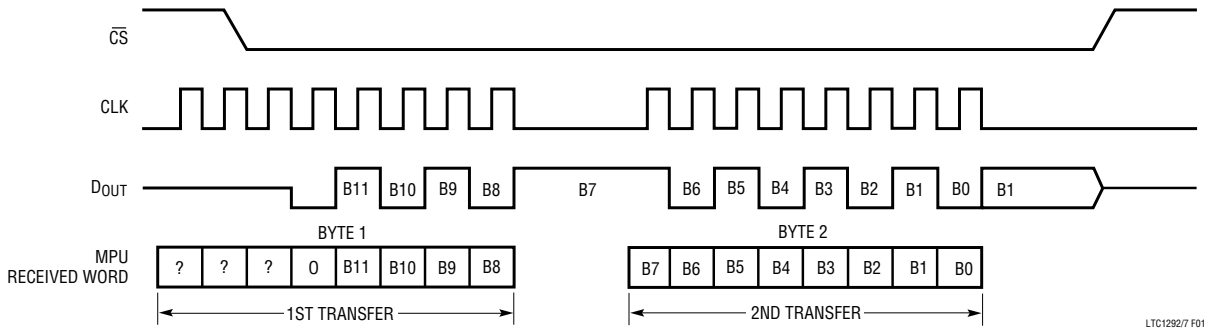


Figure 1. Data Exchange Between LTC1292 and MC68HC11

APPLICATIONS INFORMATION

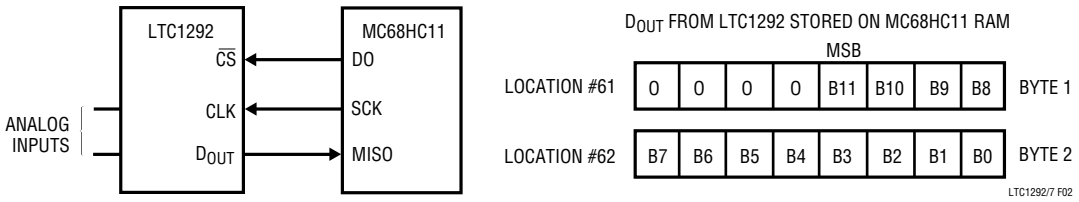


Figure 2. Hardware and Software Interface to Motorola MC68HC11 Microcontroller

MC68HC11 CODE for LTC1292 Interface

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR		STAB	$08, X	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		NOP		6 NOPS FOR TIMING
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR				
	STAA	$1009	LOAD DATA INTO PORT D DDR		LDAA	$1029	CHECK SPI STATUS REG
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A		LDAA	$102A	LOAD LTC1292 MSBs INTO ACC A
					STAA	$61	STORE MSBs IN $61
	STAA	$50	LOAD DUMMY DIN DATA INTO $50		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
LOOP	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000		NOPS		6 NOPS FOR TIMING
	LDAB	#$00	LOAD ACC B WITH $00		BSET	$08,X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAA	$50	LOAD DUMMY DIN INTO ACC A FROM $50		LDAA	$1029	CHECK SPI STATUS REGISTER
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK		LDAA	$102A	LOAD LTC1292 LSBs IN ACC
					STAA	$62	STORE LSBs IN $62
	NOP		DELAY $\overline{CS}$ FALL TIME TO RIGHT JUSTIFY DATA		JMP	LOOP	START NEXT CONVERSION

the MPU. The data is right-justified in the two memory locations (Figure 2). This was made possible by delaying the falling edge of $\overline{CS}$ till after the second CLK. ANDing the first byte with $0F_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

For the LTC1297 (Figure 3) a delay must be introduced to accommodate the setup time, $t_{su\overline{CS}}$, before the dummy D_{IN} word is sent to the data register. The first 8-bit transfer clocks B11 through B6 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits B5 through B0 into the MPU. Note B1 and B2 from the LSB-first data word have also been clocked in.

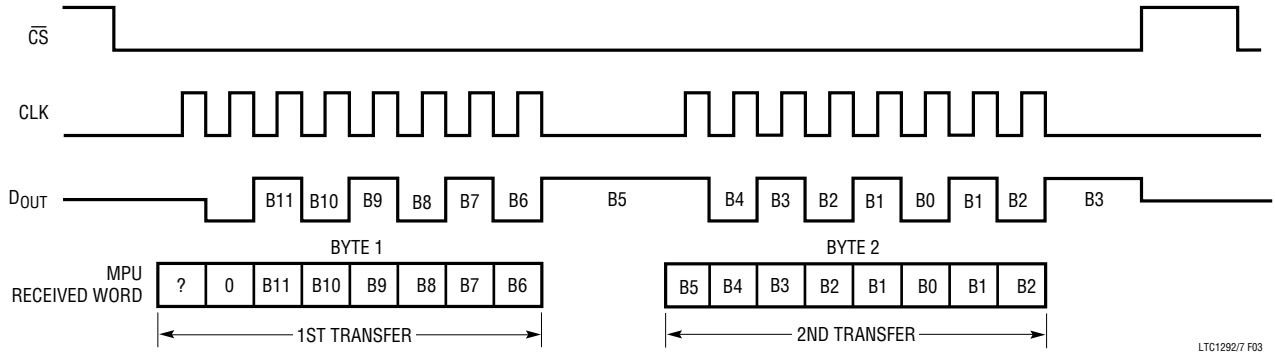


Figure 3. Data Exchange Between LTC1297 and MC68HC11

APPLICATIONS INFORMATION

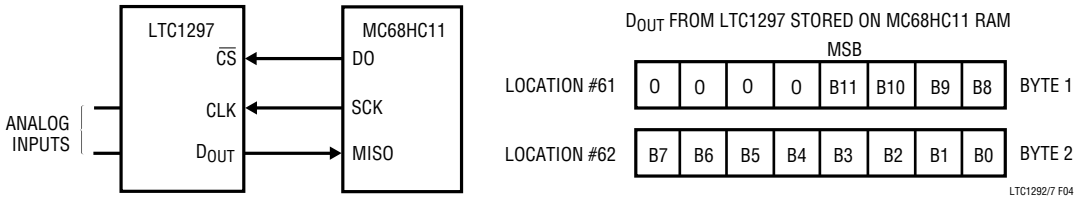


Figure 4. Hardware and Software Interface to Motorola MC68HC11 Microcontroller

MC68HC11 CODE for LTC1297 Interface

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR	LOOP1	LDAA	$1029	CHECK SPI STATUS REG
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		BPL	LOOP1	CHECK IF TRANSFER IS DONE
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		LDAA	$102A	LOAD LTC1297 MSBs INTO ACC A
	STAA	$1009	LOAD DATA INTO PORT D DDR		STAA	$61	STORE MSBs IN $61
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	STAA	$50	LOAD DUMMY DIN DATA INTO $0	LOOP2	LDAA	$1029	CHECK SPI STATUS RES
LOOP	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000		BPL	LOOP2	CHECK IF TRANSFER IS DONE
					BSET	$08X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAB	#$00	LOAD ACC B WITH $00		LDAA	$102A	LOAD LTC1297 LSBs INTO ACC A
	LDAA	$50	LOAD DIN INTO ACC FROM $50		STAA	$62	STORE LSBs IN $62
	BCLR	$08,X,$01	D0 GOES LOW ($\overline{CS}$ GOES LOW)		ROR	$61	ROTATE RIGHT WITH CARRY
	NOP		3 NOP FOR $t_{su\overline{CS}}$ TIMING		ROR	$62	NEEDED TO RIGHT JUSTIFY
	NOP				ROR	$61	THE DATA IN $61 AND $62
	NOP				ROR	$62	
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START CLK		JMP	LOOP	START NEXT CONVERSION

The data is right- justified in the two memory locations by rotating right twice (Figure 4). ANDing the first byte with $0F_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1292/LTC1297 and parallel port microprocessors. The signals $\overline{CS}$ and CLK are generated on two port lines and the D_{OUT} signal is read on a third port line. After a falling CLK edge each data bit is loaded into the carry bit and then rotated into the accumulator. Once the first 8 MSBs have been shifted into the accumulator they are loaded into register R2. The last four bits are shifted in the same way and loaded into register R3. The output data is left-justified in registers R2 and R3 (Figure 5).

For the LTC1297 four NOPs need to be inserted in the 8051 code after $\overline{CS}$ goes low to allow the LTC1297 to wake up from power shutdown ($t_{su\overline{CS}}$).

APPLICATIONS INFORMATION

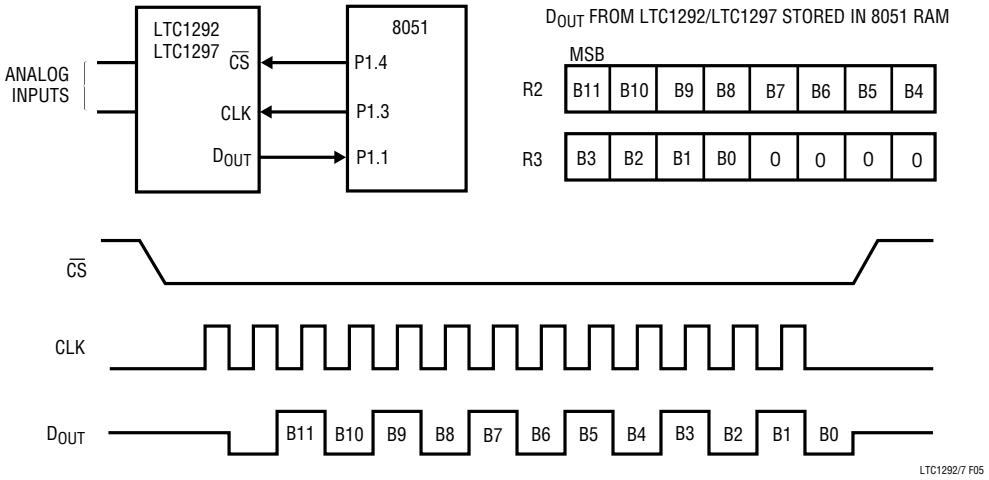


Figure 5. Hardware and Software Interface to Intel 8051 Processor

8051 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	P1,#02h	BIT 1 PORT 1 SET AS INPUT		CLR	A	CLEAR ACC
	CLR	P1.3	CLK GOES LOW		RLC	A	ROTATE DATA BIT (B3) INTO ACC
	SETB	P1.4	$\overline{CS}$ GOES HIGH			SETB P1.3	CLK GOES HIGH
CONT	CLR	P1.4	$\overline{CS}$ GOES LO		CLR	P1.3	CLK GOES LOW
	NOP		4 NOP FOR LTC1297 $t_{su\overline{CS}}$ (Wakeup		MOV	C,P1.1	READ DATA BIT INTO CARRY
	NOP		Time) (Not Needed for LTC1292)		RLC	A	ROTATE DATA BIT (B2) INTO ACC
	NOP				SETB	P1.3	CLK GOES HIGH
	NOP				CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH		MOV	C,P1.1	READ DATA BIT INTO CARRY
	CLR	P1.3	CLK GOES LOW		RLC	A	ROTATE DATA BIT (B1) INTO ACC
	SETB	P1.3	CLK GOES HIGH		SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW		CLR	P1.3	CLK GOES LOW
	MOV	R4,#08H	LOAD COUNTER		MOV	C,P1.1	READ DATA BIT INTO CARRY
LOOP	MOV	C,P1.1	READ DATA BIT INTO CARRY		SETB	P1.4	$\overline{CS}$ GOES HIGH
	RLC	A	ROTATE DATA BIT INTO ACC		RRC	A	ROTATE DATA BIT (B0) INTO ACC
	SETB	P1.3	CLK GOES HIGH		RRC	A	ROTATE RIGHT INTO ACC
	CLR	P1.3	CLK GOES LOW		RRC	A	ROTATE RIGHT INTO ACC
	DJNZ	R4,LOOP	NEXT BIT		RRC	A	ROTATE RIGHT INTO ACC
	MOV	R2,A	STORE MSBs IN R2		MOV	R3,A	STORE LSBs IN R3
	MOV	C,P1.1	READ DATA BIT INTO CARRY		AJMP	CONT	START NEXT CONVERSION

Sharing the Serial Interface

The LTC1292/LTC1297 can share the same two-wire serial interface with other peripheral components or other LTC1292/LTC1297s (Figure 6). In this case, the $\overline{CS}$ signals decide which LTC1292 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1292/LTC1297 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance

APPLICATIONS INFORMATION

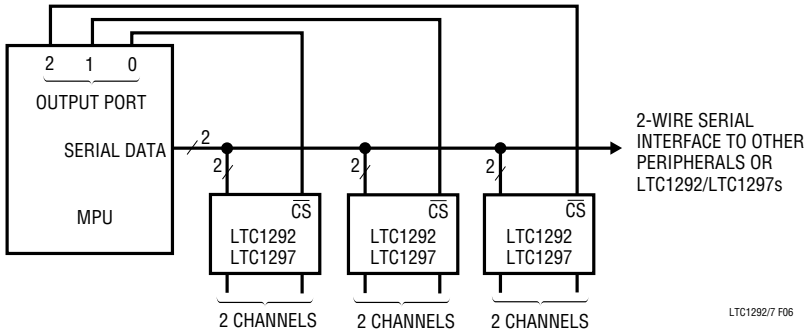


Figure 6. Several LTC1292/LTC1297s Sharing One 2-Wire Serial Interface

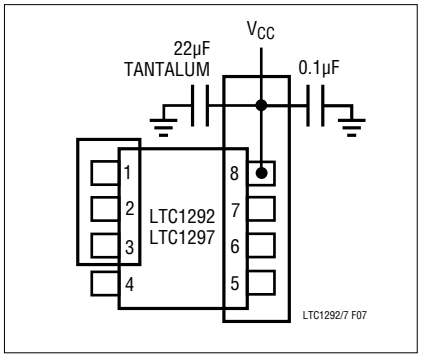


Figure 7. Example Ground Plane for the LTC1292/LTC1297

use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). Figure 7 shows an example of an ideal LTC1292/LTC1297 ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance such as obtained from a voltage regulator (e.g., LT323A). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Figures 8 and 9 show the effects of good and poor V_{CC} bypassing.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1292/LTC1297 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure that the transients caused by the current spikes settle completely before the conversion begins.

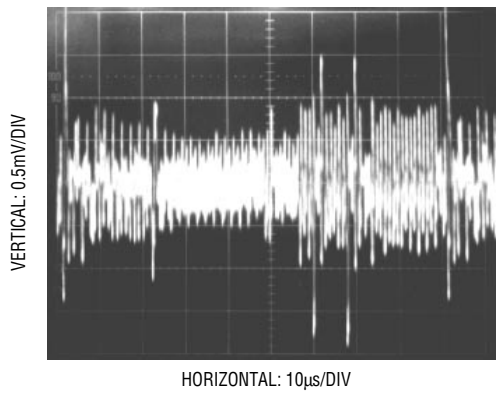


Figure 8. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

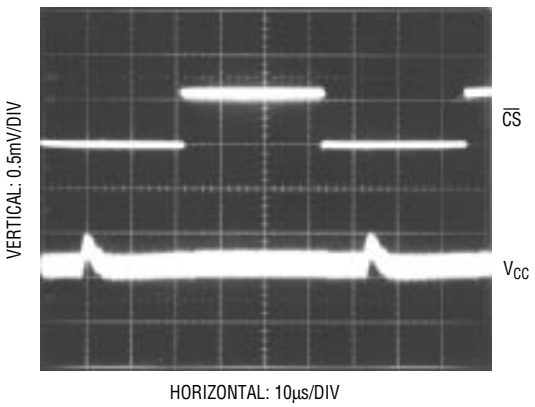


Figure 9. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

APPLICATIONS INFORMATION

Source Resistance

The analog inputs of the LTC1292/LTC1297 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) (Figures 10a and 10b). C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

"+" Input Settling

The input capacitor for the LTC1292 is switched onto the "+" input during the sample phase (t_{SMPL}, see Figures 11a, 11b and 11c). The sample period can be as short as $t_{WH\overline{CS}}$ + 1/2 CLK cycle or as long as $t_{WH\overline{CS}}$ + 1 1/2 CLK cycles before a conversion starts. This variability depends on where $\overline{CS}$ falls relative to CLK. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3.0µs, **R_{SOURCE}+ < 2.0k and C1 < 20pF will provide adequate settling time.**

The sample period for the LTC1297 starts on the falling edge of $\overline{CS}$ and ends on the falling edge of the first CLK

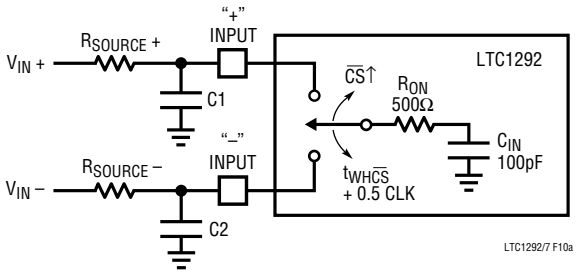


Figure 10a. Analog Input Equivalent Circuit for the LTC1292

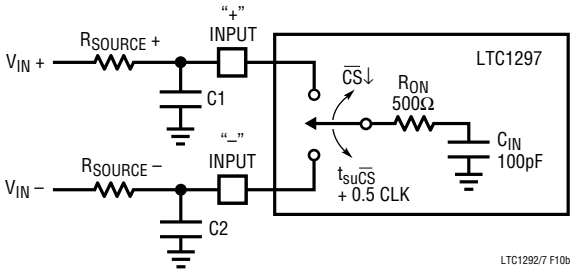


Figure 10b. Analog Input Equivalent Circuit for the LTC1297

(Figure 12). The length of the sample period is $t_{su\overline{CS}}$ +0.5 CLK cycles. Again, the voltage on the "+" input must settle completely within the sample period. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency or by increasing

"+" and "–" Input Settling Windows

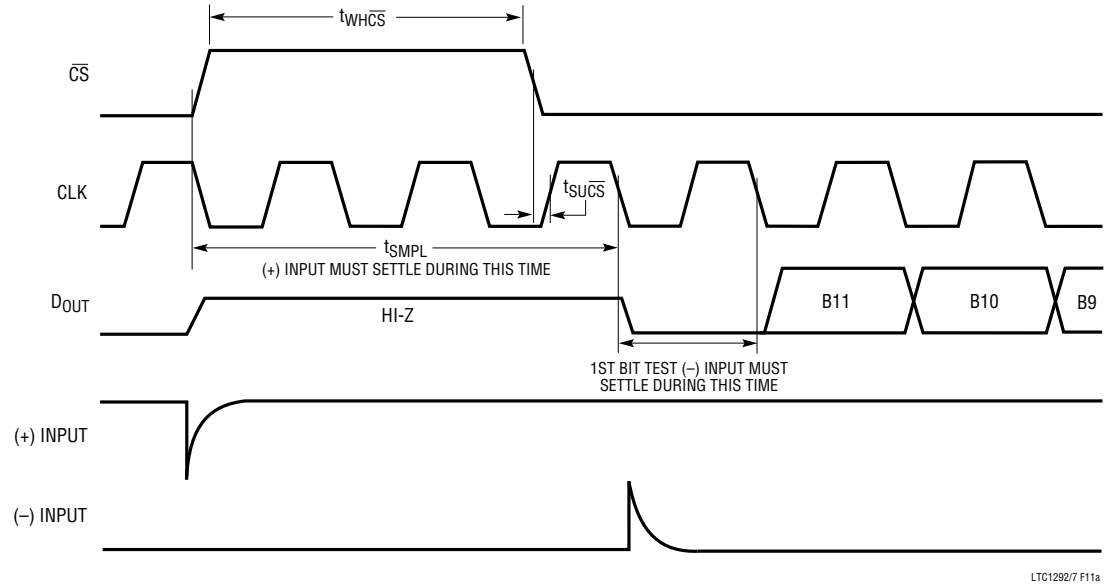


Figure 11a. Setup Time ($t_{su\overline{CS}}$) Is Met for the LTC1292

APPLICATIONS INFORMATION

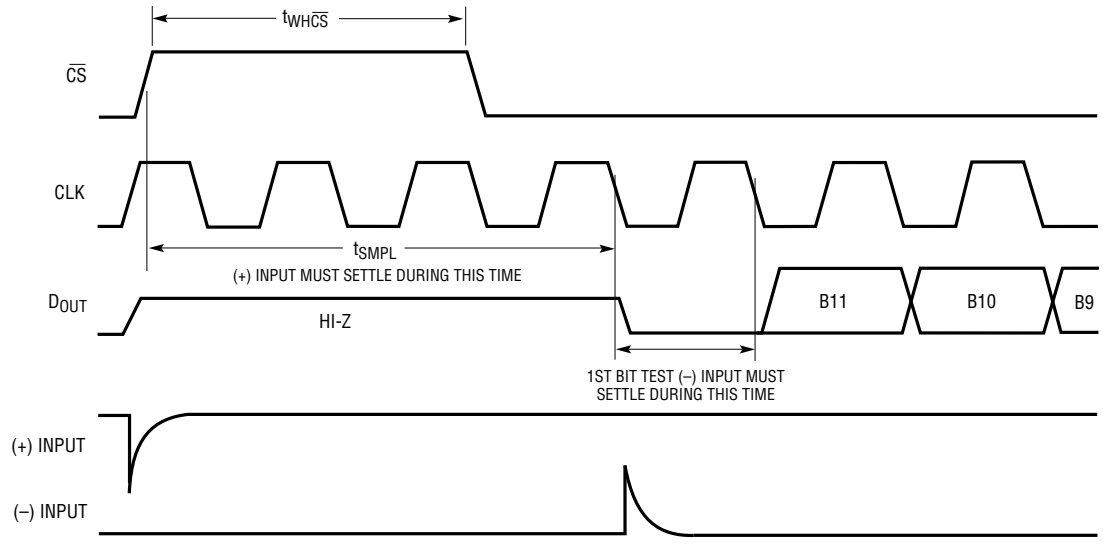


Figure 11b. Setup Time ($t_{su\overline{CS}}$) Is Met for the LTC1292

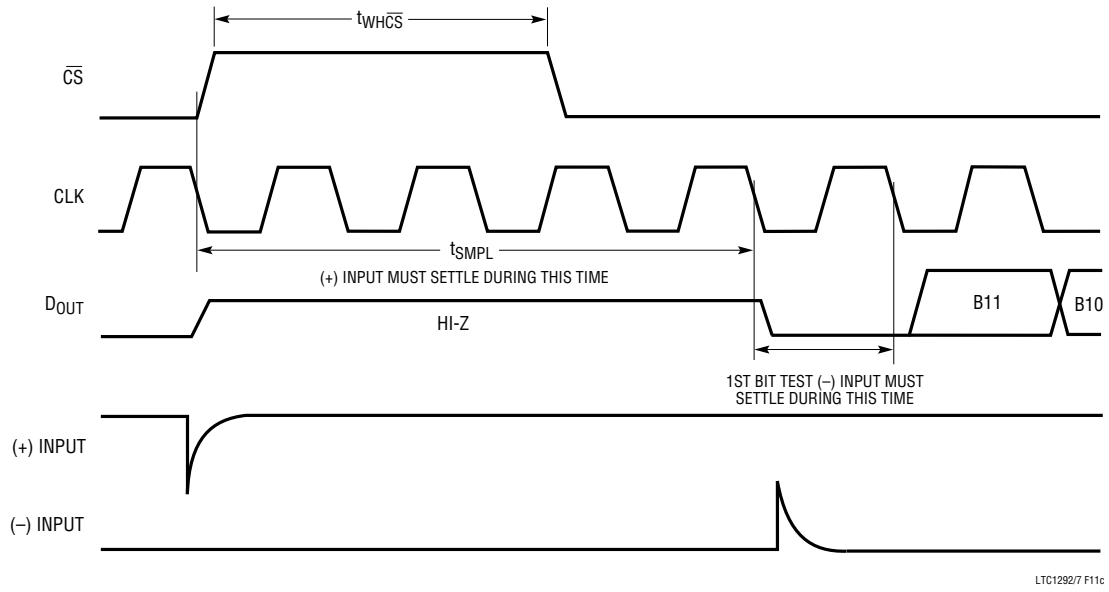


Figure 11c. Setup Time ($t_{su\overline{CS}}$) Is Not Met for the LTC1292

$t_{su\overline{CS}}$. With the minimum possible sample time of 6µs, **R_{SOURCE}+ < 5k and C1 < 20pF will provide adequate settling time**. In general for both the LTC1292 and LTC1297 keep the product of the total resistance and the total capacitance less than $t_{SMPL}/9$. If this condition can not be met, then make C1 > 0.47µF (see RC Input Filtering section).

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figures 11a, 11b, 11c and 12). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the

APPLICATIONS INFORMATION

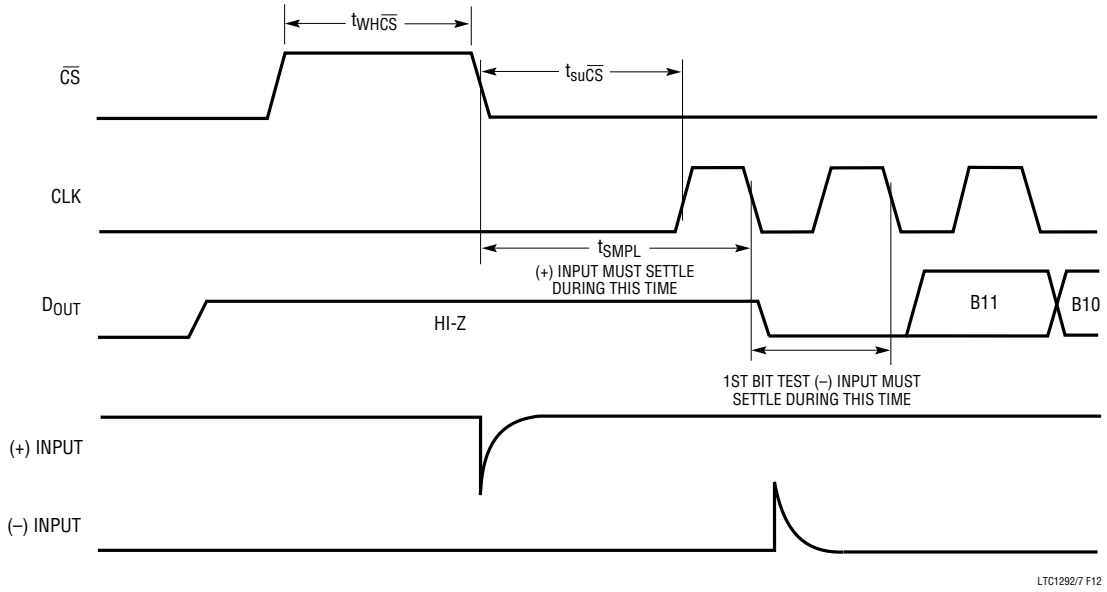


Figure 12. "+" and "–" Input Settling Windows for the LTC1297

"–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **R_{SOURCE}– < 250Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figures 11a, 11b, 11c and 12). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 3.0µs for the LTC1292 or 6.0µs for the LTC1297 ("+" input) and 1µs ("–" input) that occurs at the maximum clock rate of 1MHz. Figures 13 and 14 show examples of both adequate and poor op amp settling.

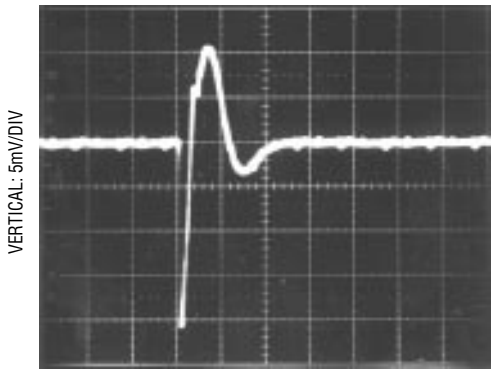


Figure 13. Adequate Settling of Op Amp Driving Analog Input

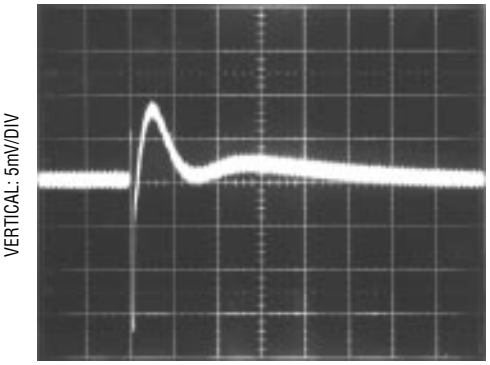


Figure 14. Poor Op Amp Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 15. For large values of C_F (e.g., 1μF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running the LTC1292(LTC1297) at the minimum cycle time of 16.5μs (20μs), the input current equals 30μA (25μA) at V_{IN} = 5V. Here a filter resistor of 4Ω (5Ω) will cause 0.1LSB of full scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristics curve Maximum Filter Resistor vs Cycle Time.

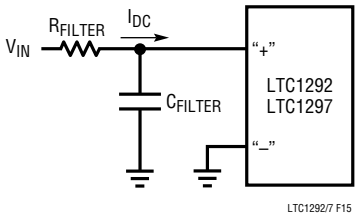


Figure 15. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1292/LTC1297 provide a built-in sample-and-hold (S&H) function on the +IN input for signals acquired in the single-ended mode (–IN pin grounded). The sample-and-hold allows the LTC1292/LTC1297 to convert rapidly varying signals (see typical performance characteristics curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 11. The sampling interval begins at the rising edge of $\overline{CS}$ for the LTC1292, and at the falling edge of $\overline{CS}$ for the LTC1297, and continues until the falling edge of the CLK before the conversion begins. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time-varying as in single-ended mode. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right) \quad \text{1292/7 E1}$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (300μV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right) \quad \text{1292/7 E2}$$

For 0.25LSB error (300μV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz.

Reference Input

The voltage on the reference input of the LTC1292/LTC1297 determine the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched-capacitor con-

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version technique (see Figure 16). During each bit test of the conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

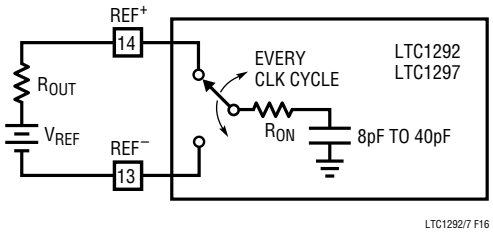

Figure 16. Reference Input Equivalent Circuit

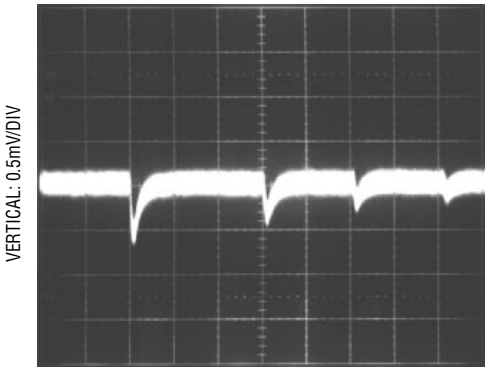

Figure 17. Adequate Reference Settling (LT1027)

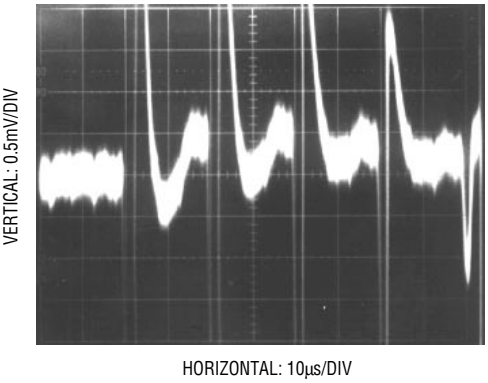

Figure 18. Poor Reference Settling Can Cause A/D Errors

Figures 17 and 18 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 1MHz most references and op amps can be made to settle within the 1µs bit time. For example the LT1027 will settle adequately. With a 10µF bypass capacitor at V_{REF} the LT1021 can also be used.

Reduced Reference Operation

The effective resolution of the LTC1292/LTC1297 can be increased by reducing the input span of the converter. The LTC1292/LTC1297 exhibit good linearity over a range of reference voltages (see typical performance characteristics curves of Change in Linearity vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and noise are factors that must be considered when operating at low V_{REF} values. The internal reference for V_{REF} has been tied to the GND pin. Any voltage drop from the GND pin to the ground plane will cause a gain error.

Offset with Reduced V_{REF}

The offset of the LTC1292/LTC1297 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.1LSB with a 5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the –IN input to the LTC1292/LTC1297.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1292/LTC1297 can be reduced to approximately 200µV_{P-P} using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference input but will

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become a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

For operation with a 5V reference, the 200μV noise is only 0.16LSB peak-to-peak. Here the LTC1292/LTC1297 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200μV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now, averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Gain Error Due to Reduced V_{REF}

The gain error of the LTC1292/LTC1297 is very good over a wide range of reference voltages. The error component that is seen in the typical performance characteristics curve Change in Gain Error vs Reference Voltage is due to the voltage drop on the GND pin from the device to the ground plane. To minimize this error the LTC1292/LTC1297 should be soldered directly onto the PC board. The internal reference point for V_{REF} is tied to GND. Any voltage drop in the GND pin will make the reference voltage, internal to the device, less than what is applied externally (Figure 19). This drop is typically 420μV due to the product of the pin resistance (R_{PIN}) and the LTC1292/LTC1297 supply current. For example, with V_{REF} = 1.25V this will result in a gain error change of –1.0LSB from the gain error measured with V_{REF} = 5V.

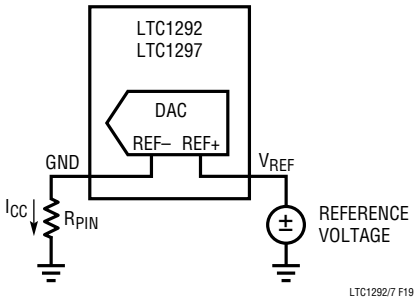

Figure 19. Parasitic Resistance in GND Pin

LTC1292 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/Ds in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "Effective Number of Bits (ENOB)." SNR is the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the non-fundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

SNR = (6.02N + 1.76dB)

where N is the number of bits. Thus the SNR depends on the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. Fast Fourier Transform (FFT) plots of the output spectrum of the LTC1292 are shown in Figures 20a and 20b. The input (f_{IN}) frequencies are 1kHz and 28kHz with the sampling frequency (f_S) at 58.8 kHz. The SNRs obtained from the plots are 73.0dB and 61.5dB.

By rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \left(\frac{SNR - 1.76dB}{6.02} \right)$$

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This is the effective number of bits (ENOB). For the example shown in Figures 20a and 20b, N = 11.8 bits and 9.9 bits, respectively. Figure 21 shows a plot of ENOB as a function of input frequency. The 2nd harmonic distortion term accounts for the degradation of the ENOB as f_{IN} approaches $f_S/2$.

Figure 22 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

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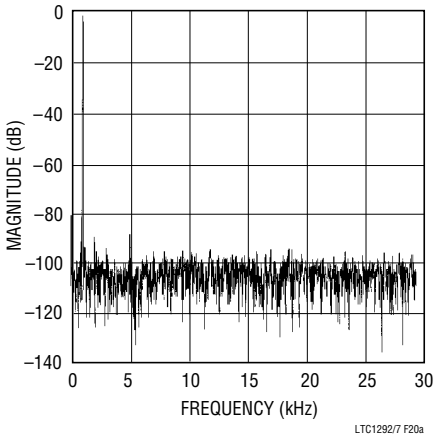

Figure 20a. f_{IN} = 1kHz, f_S = 58.8kHz, SNR = 73.0dB

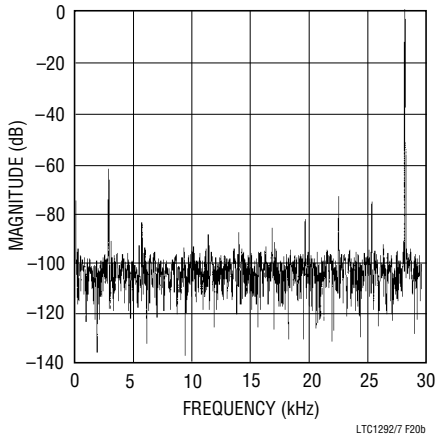

Figure 20b. f_{IN} = 28kHz, f_S = 58.8kHz, SNR = 61.5dB

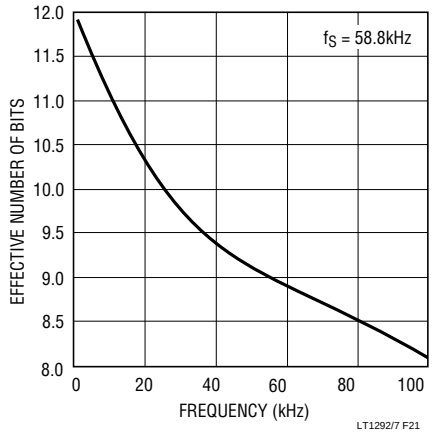

Figure 21. LTC1292 ENOB vs Input Frequency

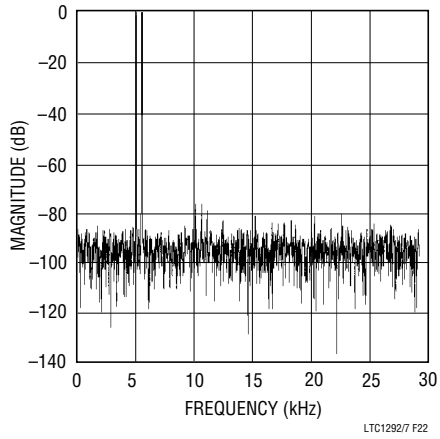

Figure 22. f_{IN1} = 5.1kHz, f_{IN2} = 5.6kHz, f_S = 58.8kHz

Overvoltage Protection

Applying signals to the LTC1292/LTC1297's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the devices. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1292/LTC1297. Another example is the input source is operating from different supplies of larger value than the LTC1292/LTC1297. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 23 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 250Ω when clocked at its maximum clock frequency of 1MHz. If the LTC1292/LTC1297 are clocked at the maximum clock frequency and 250Ω is not enough to current limit the input source, then the clamp diodes are recommended (Figures 24a and 24b). The reason for the limit on the resistor value is that the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the typical performance characteristics Maximum CLK Frequency vs Source Resistance).

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If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met, connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 25).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

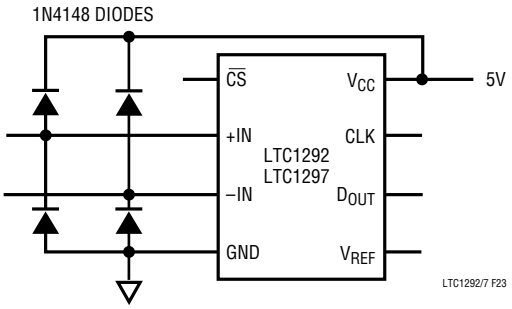

Figure 23. Overvoltage Protection with Clamp Diodes

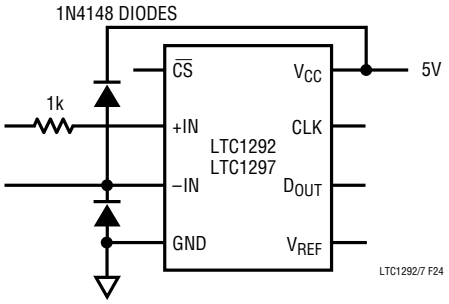

Figure 24b. Overvoltage Protection with Diode Clamps and Current Limiting Resistor

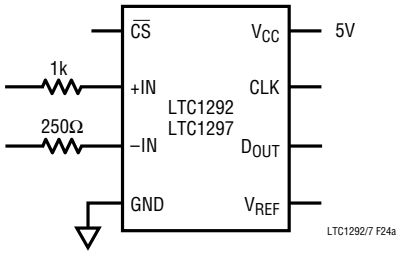

Figure 24a. Overvoltage Protection with Current Limiting Resistors

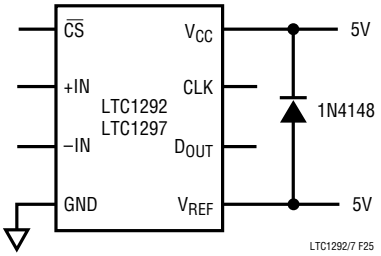

Figure 25. Separate V_{CC} and V_{REF} Supplies

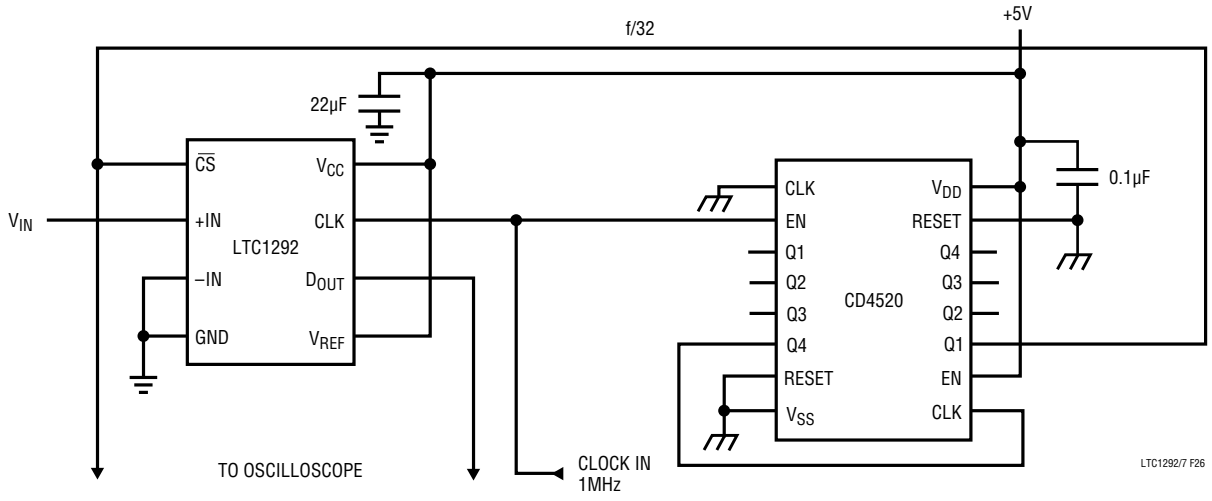

Figure 26. "Quick Look" Circuit for the LTC1292

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A "Quick Look" Circuit for the LTC1292

Users can get a quick look at the function and timing of the LTC1292 by using the "Quick Look" circuit in Figure 26. V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground plane. $\overline{CS}$ is driven at 1/32 the clock rate by the CD4520 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 27). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

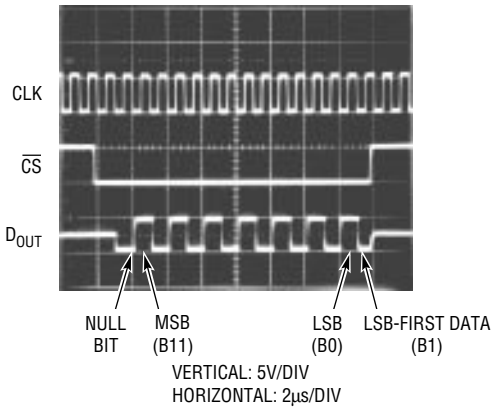

Figure 27. Scope Trace of the LTC1292 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

A "Quick Look" Circuit for the LTC1297

A circuit similar to the one used for the LTC1292 can be used for the LTC1297(Figure 28). A one shot has been generated with NAND gates, a resistor and capacitor to satisfy the setup time $t_{su\overline{CS}}$. This can be eliminated if a slower clock is used. When $\overline{CS}$ goes low the one shot is triggered. This turns off the clock to the LTC1297 for a fixed time to meet $t_{su\overline{CS}}$. Once the clock starts D_{OUT} is shifted out one bit at a time. $\overline{CS}$ is driven at 1/64 the clock rate by the 74HC393. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set to trigger on the falling edge of $\overline{CS}$. See Figure 29.

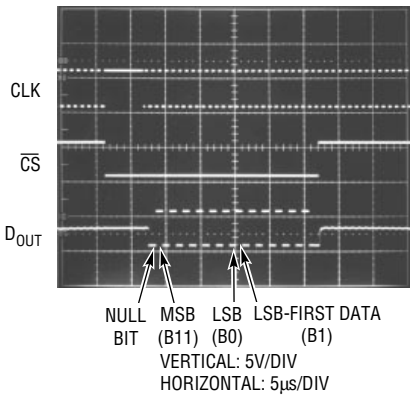

Figure 29. Scope Trace of the LTC1297 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

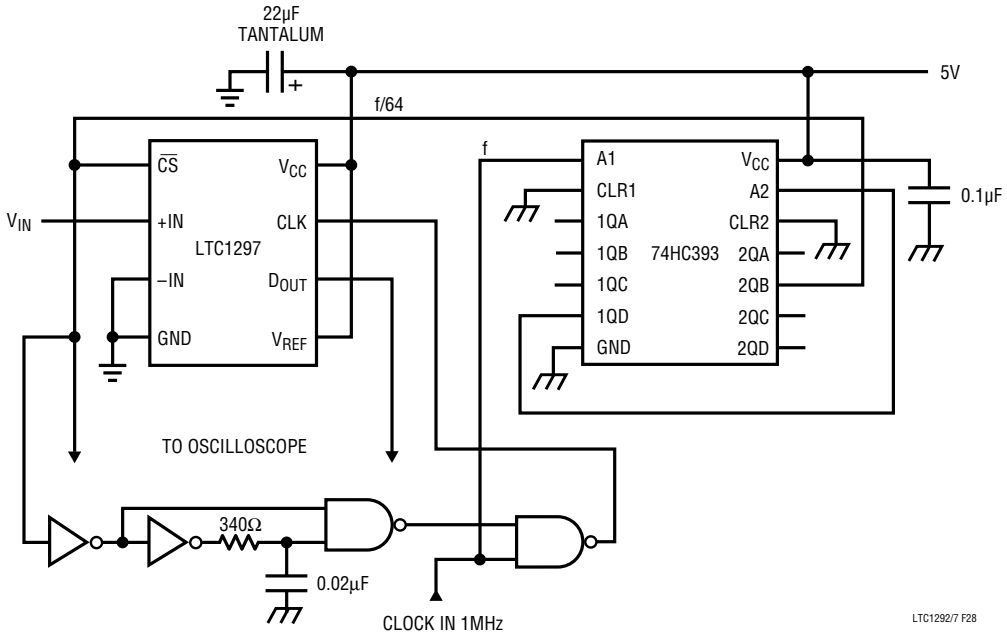

Figure 28. "Quick Look" Circuit for the LTC1297

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Opto-Isolated Temperature Monitor

Amplification of sensor outputs is often required to generate a signal large enough to be properly digitized. For example, a J-type thermocouple provides only 52µV/°C. The 5µV offset of the LTC1050 chopper op amp generates less than 0.1°C error (Figure 31). Cold junction compensation is provided by the LT1025A. (For more detail see LTC Design Note 5).

In the opto-isolated interface two signals are generated from one. This allows a two-wire interface to the LTC1292. A long high signal (>1ms) on the CLK IN input allows the 0.1µF capacitor to discharge taking $\overline{CS}$ high. This resets the A/D for the next conversion. When CLK IN starts toggling, $\overline{CS}$ goes low and stays there until the next extended CLK IN high time. See Figure 30.

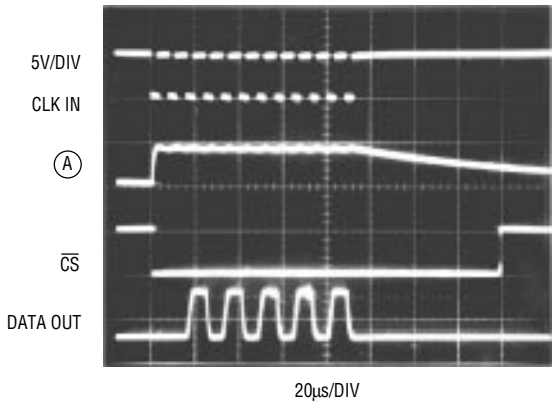


Figure 30. Opto-Isolated Temperature Monitor Digital Waveforms

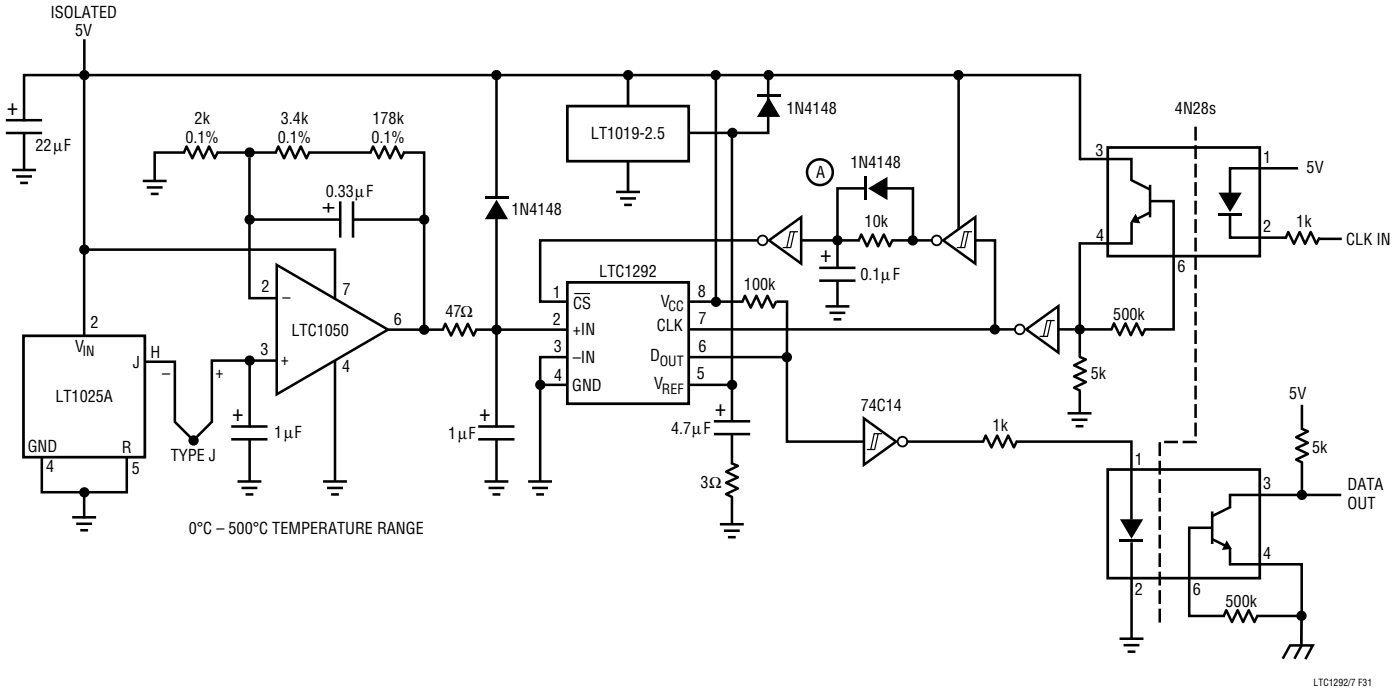
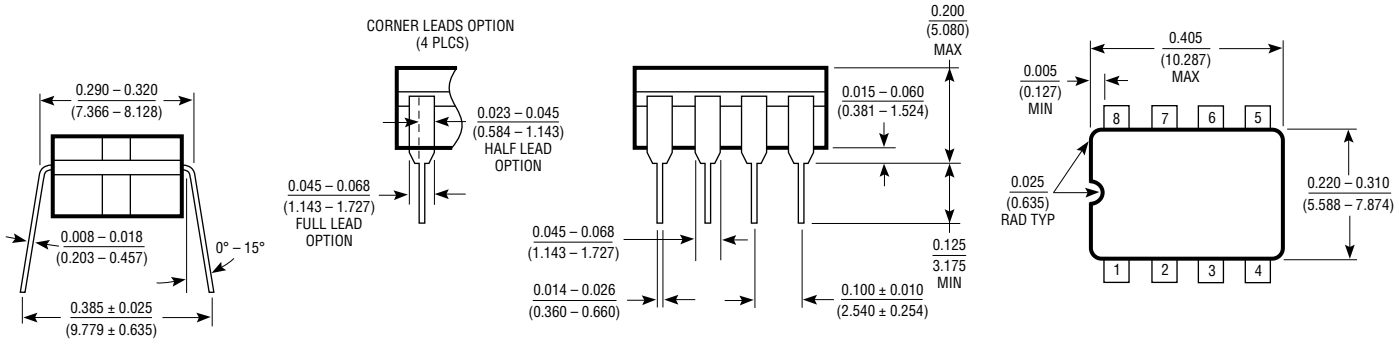


Figure 31. Opto-Isolated Temperature Monitor

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

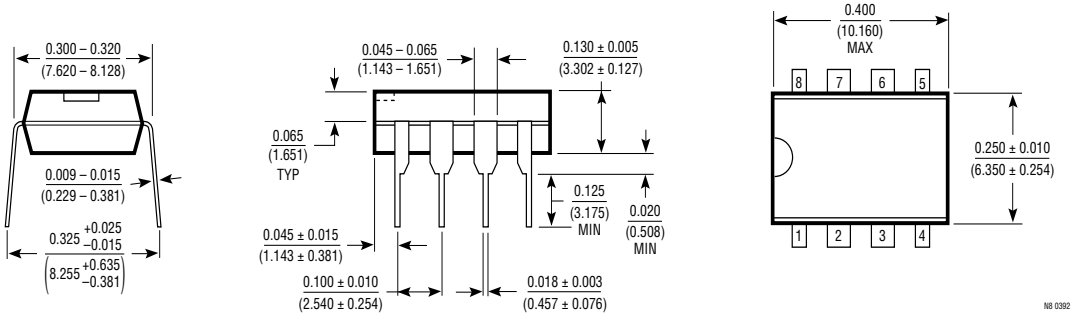
J8 Package
8-Lead Ceramic DIP



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J8 0293

N8 Package
8-Lead Plastic DIP



N8 0392

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