LTC1642

Hot Swap Controller

May 1999

FEATURES

- Single Channel Positive NFET Driver
- Programmable Undervoltage and Overvoltage Protection
- Foldback Current Limit
- Adjustable Current Limit Time-Out
- Latch Off or Automatic Retry on Current Fault
- Driver for SCR Crowbar on Overvoltage
- Programmable Reset Timer
- Reference Output with Uncommitted Comparator
- V_{CC}: 2.97V to 16.5V Normal Operation, Protected Against Surges to 33V.
- 16-Pin SSOP Package

APPLICATIONS

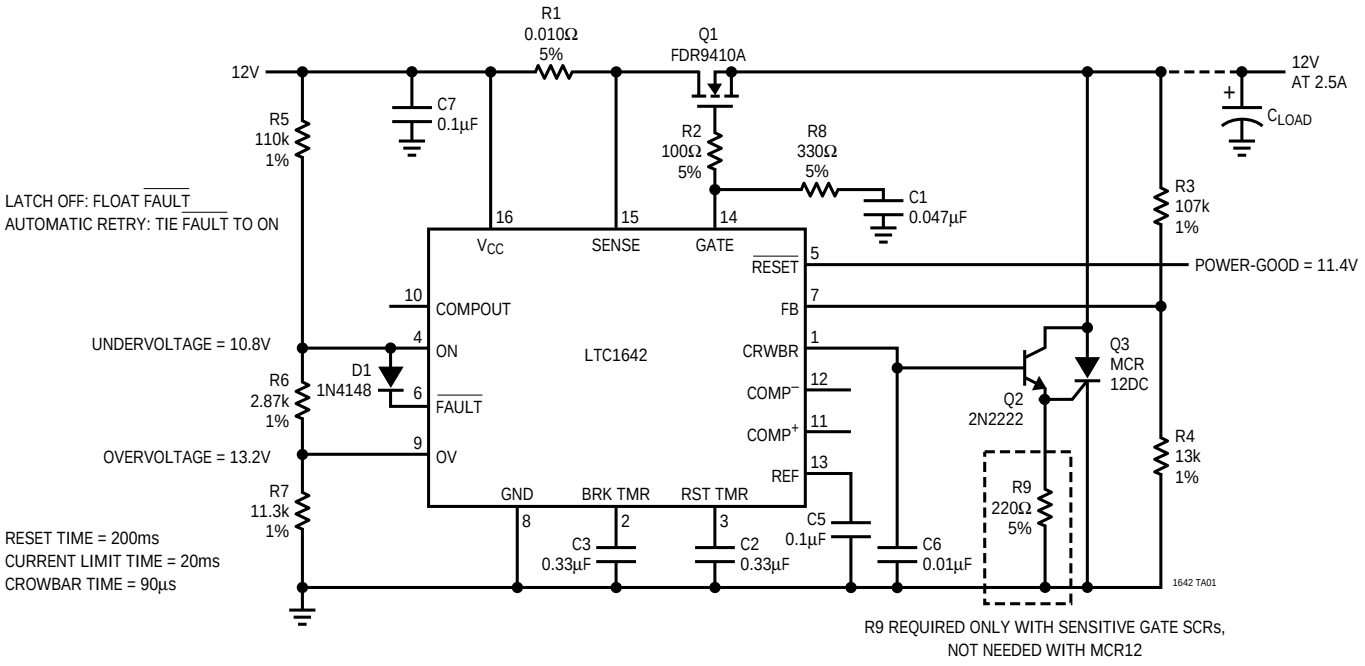
- Hot Board Insertion
- Electronic Circuit Breaker

DESCRIPTION

The LTC®1642 is a 16-pin Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, the board supply voltage can be ramped up at a programmable rate. A high side switch driver controls the N-channel gate for supply voltages ranging from 2.97V to 16.5V.

The SENSE pin allows foldback limiting of the load current, with circuit breaker action after a programmable delay time. The delay allows the part to power-up in current limit. The CRWBR output can be used to trigger an SCR for crowbar load protection after a programmable delay if the input supply exceeds a programmable voltage. The $\overline{\text{RESET}}$ output can be used to generate a system reset with programmable delay when the supply voltage falls below a programmable voltage. The ON pin can be used to cycle the board power. The LTC1642 is available in the 16-pin SSOP package.

TYPICAL APPLICATION

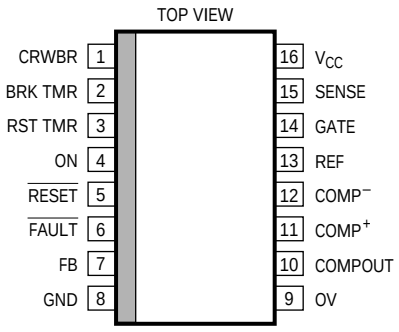


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) .....–0.3V to 33V
SENSE Pin ..... –0.3V to (V_{CC} + 0.3V)
GATE Pin .....–0.3V to 27V
All Other Pins.....–0.3V to 16.5V
Operating Temperature Range
LTC1642C ..... 0°C to 70°C
LTC1642I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1642CGN LTC1642IGN

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current	ON = V_{CC}	●		1.25	3.0	mA
V_{LKHI}	V_{CC} Undervoltage Lockout (Low to High)		●	2.55	2.73	2.95	V
V_{LKLO}	V_{CC} Undervoltage Lockout (High to Low)		●	2.35	2.50	2.80	V
V_{LKHYST}	V_{CC} Undervoltage Lockout Hysteresis				230		mV
V_{CC}	Operating Voltage Range			2.97		16.5	V
V_{FB}	FB Pin Voltage Threshold (FB Falling)		●	1.208	1.220	1.232	V
ΔV_{FB}	FB Pin Threshold Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
V_{FBHST}	FB Pin Voltage Threshold Hysteresis				3		mV
V_{OV}	OV Pin Voltage Threshold (OV Rising)		●	1.208	1.220	1.232	V
ΔV_{OV}	OV Pin Threshold Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
V_{OVHYST}	OV Pin Voltage Theshold Hysteresis				3		mV
V_{RST}	RST TMR Pin Voltage Threshold (RST TMR Rising)		●	1.200	1.220	1.250	V
ΔV_{RST}	RST TMR Pin Threshold Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
I_{RST}	RST TMR Pin Current	Timer On Timer Off, V_{RSTTMR} = 1.5V	●	–2.5	–2.0 10	–1.5	µA mA
V_{BRK}	BRK TMR Pin Voltage Threshold (BRK TMR Rising)		●	1.200	1.220	1.250	V
ΔV_{BRK}	BRK TMR Pin Threshold Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
I_{BRK}	BRK TMR Pin Current	Timer On Timer Off, V_{BRKTMR} = 1.5V	●	–30	–20 10	–15	µA mA
V_{CR}	CRWBR Pin Voltage Theshold		●	375	410	425	mV
ΔV_{CR}	CRWBR Pin Threshold Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V	●		4	15	mV
I_{CR}	CRWBR Pin Current	CRWBR On, V_{CRWBR} = 0V CRWBR On, V_{CRWBR} = 2.1V CRWBR Off, V_{CRWBR} = 1.5V	● ●	–60	–45 –1500 2.3	–30 –1000	µA µA mA

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CB}	Circuit Breaker Trip Voltage	$V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = GND $V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = 1V	● ●	15 45	25 52.5	36 60	mV mV
I_{CP}	GATE Pin Output Current	Charge Pump On, V_{GATE} = GND Charge Pump Off, V_{GATE} = 5V	●	–30	–25 10	–20	µA mA
ΔV_{GATE}	External N-Channel Gate Drive	$V_{GATE} - V_{CC}$, V_{CC} = 3V $V_{GATE} - V_{CC}$, V_{CC} = 5V $V_{GATE} - V_{CC}$, V_{CC} = 15V	● ● ●	4.5 10 4.5	5.9 11.5 8.5	8.0 14 18	V V V
V_{ONHI}	ON Pin Threshold (Low to High)			1.30	1.34	1.38	V
V_{ONLO}	ON Pin Threshold (High to Low)		●	1.20	1.22	1.26	V
V_{ONHYST}	ON Pin Hysteresis				110		mV
V_{OL}	Output Low Voltage	$\overline{RESET}$, $\overline{FAULT}$, COMPOUT I_O = 1.5mA	●			0.4	V
I_{PU}	Logic Output Pull-Up Current	$\overline{RESET}$, $\overline{FAULT}$ = GND			–15		µA
V_{REF}	Reference Output Voltage	No Load	●	1.208	1.220	1.232	V
ΔV_{LNR}	Reference Line Regulation	2.97V ≤ V_{CC} ≤ 16.5V, No Load	●		5	15	mV
ΔV_{LDR}	Reference Load Regulation	I_O = 0mA to –1mA, Sourcing Only	●		2.5	7.5	mV
I_{RSC}	Reference Short-Circuit Current	V_{REF} = 0V			4.5		mA
V_{COS}	Comparator Offset Voltage	$V_{CM} = V_{REF}$	●			±10	mV
V_{CHYST}	Comparator Hysteresis	$V_{CM} = V_{REF}$			3		mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

PIN FUNCTIONS

CRWBR (Pin 1): Combination Overvoltage Timer and Crowbar Circuit Trigger. The timer sets the overvoltage time needed to trigger the crowbar circuit. To use the timer connect a capacitor C to ground; the trigger time is 9ms•C(µF). When the timer is off an internal N-channel pulls the pin to ground. The timer is started when the OV comparator trips. A 45µA current source is connected from V_{CC} to the CRWBR pin, and the voltage increases at a rate of 45/C(µF) Volts/second. When the voltage reaches 410mV the current sourced by the pin increases to 1.5mA. Boost this current with an NPN emitter follower to trigger a crowbar SCR.

BRK TMR (Pin 2): Analog Timer which Limits the Time the Part Remains In Current Limit. To use the timer connect a capacitor from BRK TMR to ground. BRK TMR is pulled to ground until the sense resistor current reaches its limit, when the pin begins sourcing 20µA and the pin voltage increases at a rate of 20/C(µF) Volts/second. When the pin reaches 1.23V the GATE pin is pulled to ground and the $\overline{FAULT}$ output is asserted until the chip is reset. To allow the part to remain in current limit indefinitely ground BRK TMR.

RST TMR (Pin 3): Analog System Timer. To use the timer connect a capacitor from RST TMR to ground. This timer sets the delay from the ON pin going high to the start of the GATE pin's ramp; it also sets the delay from output voltage good, as sensed by the FB pin, to $\overline{RESET}$ going high. When the timer is off, an internal N-channel shorts RST TMR to ground. When the timer is turned on a 2µA current from V_{CC} is connected and the RST TMR pin voltage starts to ramp up at a rate of 2/C(µF) Volts/second. The timer trips when the voltage reaches 1.23V.

PIN FUNCTIONS

ON (Pin 4): Control. When ON is low the GATE pin is grounded and FAULT goes high. The GATE pin voltage starts ramping up one RST TMR timing cycle after ON goes high. Pulsing the ON pin low for at least 2µs also resets the chip when it latches off after a sustained overvoltage or current limit. The threshold on a low to high transition is 1.34V with 110mV of hysteresis.

RESET (Pin 5): Open Drain Output. RESET is pulled low if the voltage at the FB pin is below its trip point and goes high one timing cycle after the FB voltage exceeds its trip point plus 3mV of hysteresis. RESET has a weak pull-up to one diode drop below V_{CC}; an external resistor can pull the pin above V_{CC}.

FAULT (Pin 6): Open Drain Output. FAULT is pulled low when the part latches itself off following a sustained overvoltage or current limit. It goes high 2µs after the ON pin goes low. FAULT has a weak pull-up to one diode drop below V_{CC}; an external resistor can pull the pin above V_{CC}.

FB (Pin 7): Noninverting Input to An Analog Comparator; the inverting input is tied to the 1.23V internal reference. The FB comparator can be used with an external resistive divider to monitor the output supply voltage. When the FB voltage is lower than 1.23V the RESET pin is pulled low. RESET goes high one system timing cycle after the voltage at FB exceeds its threshold by 3mV of hysteresis. A low pass filter at the comparator's output prevents negative voltage glitches from triggering a false reset.

GND (Pin 8): Chip Ground.

OV (Pin 9): Analog Input Used to Monitor Overvoltages. When the voltage on OV exceeds its trip point the GATE pin is pulled low immediately and the CRWBR timer starts. If OV remains above its trip point (minus 3mV of hysteresis) long enough for CRWBR to reach its trip point the part latches off until reset by pulsing the ON pin low; otherwise, the GATE pin begins ramping up one RST TMR timing cycle after OV goes below its trip point.

COMPOUT (Pin 10): Uncommitted Comparator's Open Drain Output.

$COMP^+$ (Pin 11): Uncommitted Comparator's Noninverting Input.

$COMP^-$ (Pin 12): Uncommitted Comparator's Inverting Input.

REF (Pin 13): The Reference Voltage Output, 1.232V ±2%. To ensure stability the pin should be bypassed with a 0.1µF compensation capacitor. For V_{CC} = 5V it can source 1mA.

GATE (Pin 14): High Side Gate Drive for the External N-Channel. An internal charge pump provides at least 4.5V of gate drive, but can only source 25µA. The pin requires an external series RC network to ground to compensate the current limit loop, and to limit the maximum voltage ramp which is dV/dt (V/s) = 25/C(µF). GATE is immediately pulled to ground when the overvoltage comparator trips or the input supply is below the undervoltage lockout trip point. During current limit the GATE voltage is adjusted to maintain constant load current until the BRK TMR pin trips, when the pin is pulled to ground until the chip is reset.

SENSE (Pin 15): Current Limit Set. To use the current limit place a sense resistor in the supply path between V_{CC} and SENSE. Should the drop across the resistor exceed a threshold voltage the GATE pin is adjusted to maintain a constant load current and the timer at the BRK TMR pin is started. To protect the external FET from thermal damage the circuit breaker trips after the BRK TMR timing cycle. A foldback feature makes the current limit decrease as the voltage at FB approaches ground. Figure 3 quantifies the relationship. To disable the current limit short SENSE to V_{CC}.

V_{CC} (Pin 16): Positive Supply Voltage; between 2.97V and 16.5V in normal operation. An internal undervoltage lockout circuit holds the GATE pin at ground until V_{CC} exceeds 2.73V. If V_{CC} exceeds 16.5V an internal shunt regulator protects the chip from V_{CC} and SENSE pin voltages up to 33V. When the internal shunt regulator is active and the charge pump is on the GATE pin voltage will usually be low but this is not guaranteed; use the OV pin to ensure that the pass device is off. The V_{CC} pin also provides a Kelvin connection to the high side of the SENSE resistor.

APPLICATIONS INFORMATION

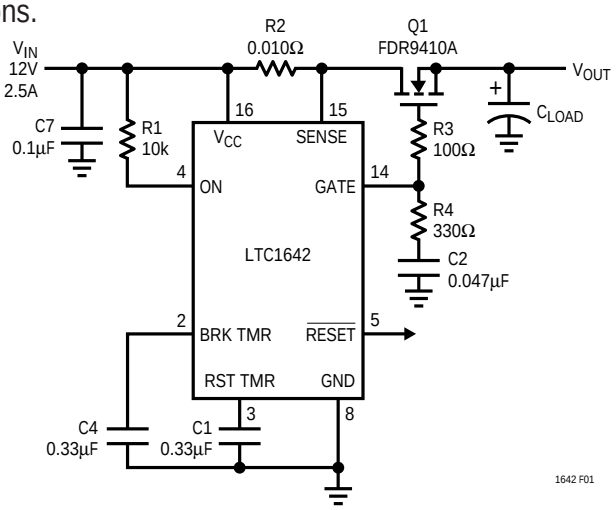
Hot Circuit Insertion

When a circuit board is inserted into a live backplane its supply bypass capacitors can draw large currents from the backplane power bus as they charge. These currents can permanently damage connector pins and can glitch the backplane supply, resetting other boards in the system. The LTC1642 limits the charging currents drawn by a board's capacitors, allowing safe insertion in a live backplane.

Power Supply Ramping

In the circuit shown in Figure 1 the LTC1642 and the external N-channel pass transistor Q1 work together to limit charging currents. When power is first applied to V_{CC} the chip holds Q1's gate at ground. After a programmable delay a 25µA current source begins to charge the external capacitor C2, generating a voltage ramp of 25µA/C2 V/s at the GATE pin. Because Q1 acts as a source follower while its gate ramps, the current charging the board's bypass capacitance C_{LOAD} is limited to 25µA•C_{LOAD}/C2.

An internal charge pump supplies the 25µA gate current, ensuring sufficient gate drive to Q1. At 3V V_{CC} the minimum gate drive is 4.5V; at 5V V_{CC} the minimum is 10V; at 15V V_{CC} the minimum is again 4.5V, due to a Zener clamp from the GATE pin to ground. Resistor R3 limits this Zener's transient current during board insertion and removal and protects against high frequency FET oscillations.



ALL RESISTORS ±5% UNLESS NOTED
RESET DELAY = 200ms
SHORT-CIRCUIT DURATION = 20ms

Figure 1. Supply Control Circuitry

The delay before the GATE pin voltage begins ramping is determined by the system timer. It comprises an external capacitor C1 from the RST TMR pin to ground; an internal 2µA current source feeding RST TMR from V_{CC}; an internal comparator, with the positive input tied to RST TMR and the negative input tied to the 1.23V reference; and an NMOS pull-down. In standby, the NMOS holds RST TMR at ground; when the timer starts the NMOS turns off and the RST TMR voltage ramps up as the current source charges the capacitor. When RST TMR reaches 1.23V the timer comparator trips; the GATE voltage begins ramping and RST TMR returns to ground. The ramp time Δt needed to trip the comparator is : $\Delta t(ms) = 615 \bullet C1(\mu F)$.

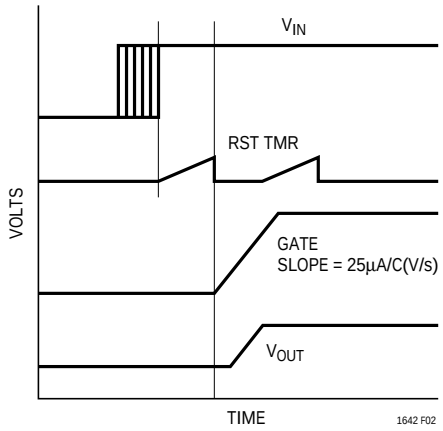


Figure 2. Supply Control Timing

Powering-Up In Current Limit

Ramping the GATE pin voltage *indirectly* limits the charging current to I = 25µA•C_{LOAD}/C2, where C2 is the external capacitor connected to the GATE and C_{LOAD} is the load capacitance. If the value of C_{LOAD} is uncertain, then a worst-case design can often result in needlessly long ramp times, and it may be better to limit the charging current directly.

Current Limiting and Solid-State Circuit Breaker

The board current can be limited by connecting a sense resistor between the LTC1642's V_{CC} and SENSE pins. An internal servo loop adjusts the GATE pin voltage such that Q1 acts as a constant current source if the voltage drop across the sense resistor reaches a limit. The voltage limit across the sense resistor increases as the output charges

APPLICATIONS INFORMATION

up; this "foldback" limiting tends to keep the power dissipation in the N-channel pass transistor constant. The output voltage is sensed at the FB pin. The limiting sense resistor voltage is 23mV when FB is grounded, but increases gradually to 53mV when FB exceeds 1V; Figure 3 shows the full dependence.

When the sense resistor voltage reaches its limit, a circuit breaker timer starts. This timer uses the BRK TMR pin and has a 1.23V threshold. If BRK TMR reaches 1.23V the timer comparator trips, tripping the circuit breaker; if the sense resistor voltage falls below its limit before the comparator trips the GATE voltage begins ramping back up immediately. The ramp time Δt needed to trip the comparator is $\Delta t(ms) = 62 \bullet C(\mu F)$, where C is the external capacitance.

Once the circuit breaker trips, GATE and $\overline{FAULT}$ remain at ground until the chip is restarted. To restart, hold the ON pin low for at least 2µs and $\overline{FAULT}$ will go high. Then take ON high again and the GATE will ramp up after a system timing cycle. Or, configure the LTC1642 to restart itself after the circuit breaker trips by connecting $\overline{FAULT}$ to the ON pin.

The servo loop controlling Q1 during current limit has a unity-gain frequency of about 125kHz; in Figure 1 R4, together with C2, provide compensation. To ensure stability the product $1/(2 \bullet \pi \bullet R4 \bullet C2)$ should be kept below the unity-gain frequency, and C2 should be more than Q1's gate-source capacitance. The values shown in Figure 1, 0.047µF and 330Ω, are a starting point.

Typical waveforms during a load short to ground are shown in Figure 4. The load is shorted to ground at time 1. The GATE voltage drops until the load current equals its maximum limit, and the circuit breaker timer starts. The short is cleared at time 2, before the timer trips. The BRK TMR pin returns to ground, and the GATE voltage begins ramping up. At time 3 the load is shorted again and at time 4 the timer trips, pulling the GATE to ground and asserting $\overline{FAULT}$. Although the short is cleared at time 5, $\overline{FAULT}$ doesn't go high until the ON pin is pulled low at time 6. At time 7 ON goes high and the system timer starts. When it trips at time 8 the GATE voltage begins ramping.

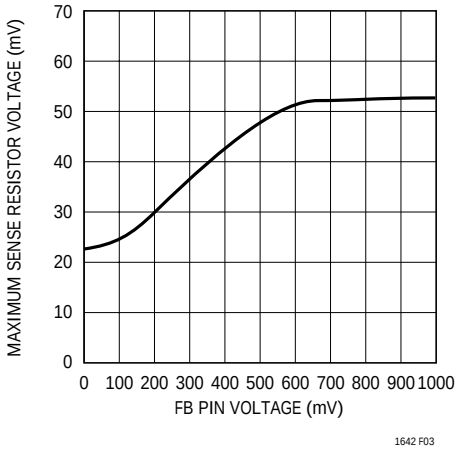


Figure 3. Maximum Sense Resistor Voltage vs FB Voltage

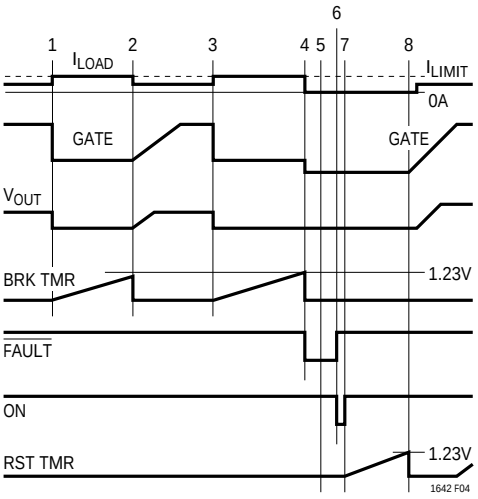


Figure 4. Current Limit and Circuit Breaker Timing

APPLICATIONS INFORMATION

Automatic Restart After a Current Fault

The LTC1642 will automatically attempt to restart itself after the circuit breaker opens if the $\overline{\text{FAULT}}$ output is tied to the ON pin. The circuit is shown in Figure 5, and the waveforms during a load short in Figure 6.

During a continuous current limit such as a load short, the N-channel pass transistor's duty cycle is equal to the circuit breaker timer period, divided by the sum of the circuit breaker and system timer periods. If $\overline{\text{FAULT}}$ is tied to ON then open drain logic should be used to drive the node. The external pull-up resistor at the ON pin may be omitted because $\overline{\text{FAULT}}$ provides a weak pull-up.

Undervoltage Lockout

An internal undervoltage lockout circuit holds the charge pump off until V_{CC} exceeds 2.73V. If V_{CC} falls below 2.5V, it turns off the charge pump and clears overvoltage and current limit faults.

For higher lockout thresholds tie the ON pin to a resistor divider driven from V_{CC}, as shown in Figure 7. This circuit keeps the charge pump off until V_{CC} exceeds (1+R1/R5)•1.34V, and also turns it off if V_{CC} falls below (1+R1/R5)•1.23V.

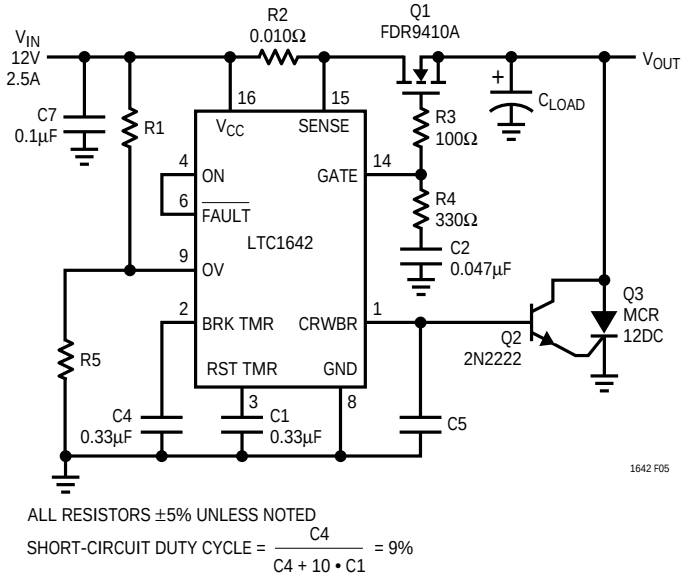


Figure 5. Automatic Restart Circuit

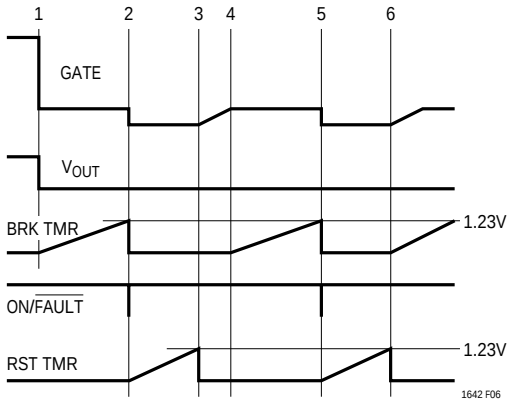


Figure 6. Automatic Retry Following a Load Short

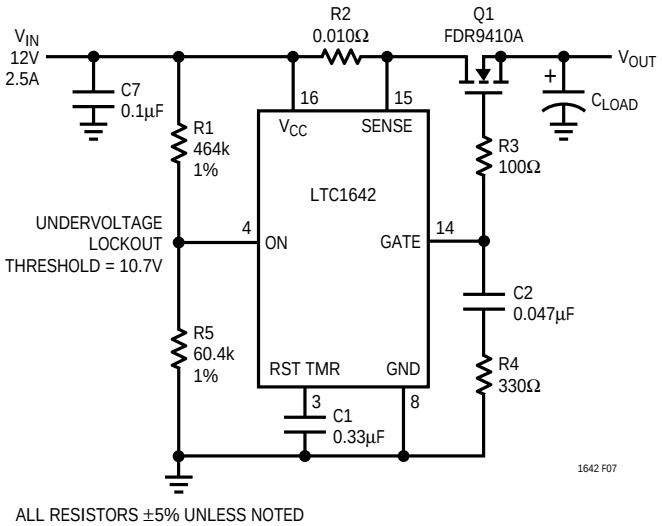


Figure 7. Setting a Higher Undervoltage Lockout

APPLICATIONS INFORMATION

Overvoltage Protection

The LTC1642 can protect a load from overvoltages by turning off the pass transistor if the supply voltage exceeds a programmable limit, and by triggering a crowbar SCR if the overvoltage lasts longer than a programmable time. The part can also be configured to automatically restart when the overvoltage clears.

The overvoltage protection circuitry is shown in Figure 8. The external components comprise a resistor divider driving the OV pin, timing capacitor C5, NPN emitter follower Q2, and crowbar SCR Q3. Because the MCR12DC is not a sensitive-gate device, the optional resistor shunting the SCR gate to ground is omitted. The internal components comprise a comparator, 1.23V bandgap reference, two current sources, and a timer at the CRWBR pin. When V_{CC} exceeds (1+R1/R5)•1.23V the comparator's output is high and internal logic pulls the GATE down and starts the timer. This timer has a 0.410V threshold and uses the CRWBR pin; when CRWBR reaches 0.410V the timer comparator trips, and the current sourced from V_{CC} increases to 1.5mA. Emitter follower Q2 boosts this current to trigger crowbar SCR Q3. The ramp time Δt needed to trip the comparator is : $\Delta t(ms) = 9.1 \bullet C5(\mu F)$.

Once the CRWBR timer trips the LTC1642 latches off: after the overvoltage clears GATE and $\overline{FAULT}$ remain at ground and CRWBR continues sourcing 1.5mA. To restart the part after the overvoltage clears, hold the ON pin low for at least 2µs and then bring it high. The GATE voltage will begin ramping up one system timing cycle later. The part will restart itself if $\overline{FAULT}$ and ON are connected: GATE begins ramping up one system timing cycle after the overvoltage clears.

Figure 9 shows typical waveforms when the divider is driven from V_{CC}. The OV comparator goes high at time 1, causing the chip to pull the GATE pin to ground and start the CRWBR timer. At time 2, before the timer's comparator trips, OV falls below its threshold; the timer resets and GATE begins charging one system timing cycle later at time 3. Another overvoltage begins at time 4, and at time 5 the CRWBR timer trips; $\overline{FAULT}$ goes low and the CRWBR pin begins sourcing 1.5mA. Even after OV falls below 1.23V at time 6, GATE and $\overline{FAULT}$ stay low, and CRWBR continues to source 1.5mA. $\overline{FAULT}$ goes high when ON

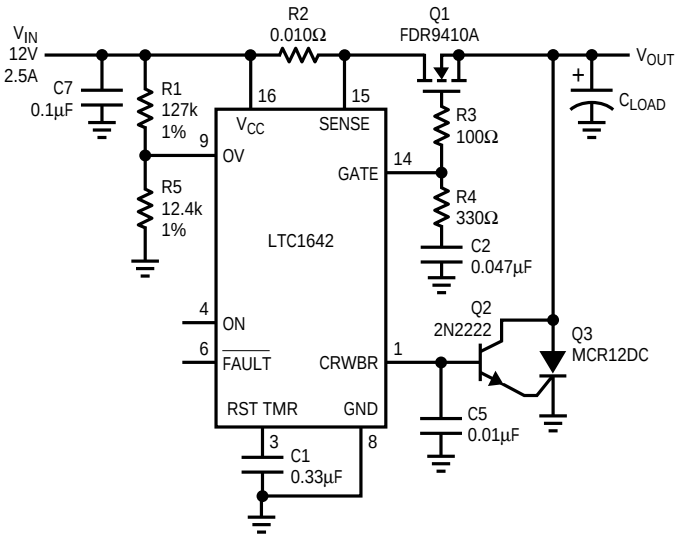


Figure 8. Overvoltage Protection Circuitry

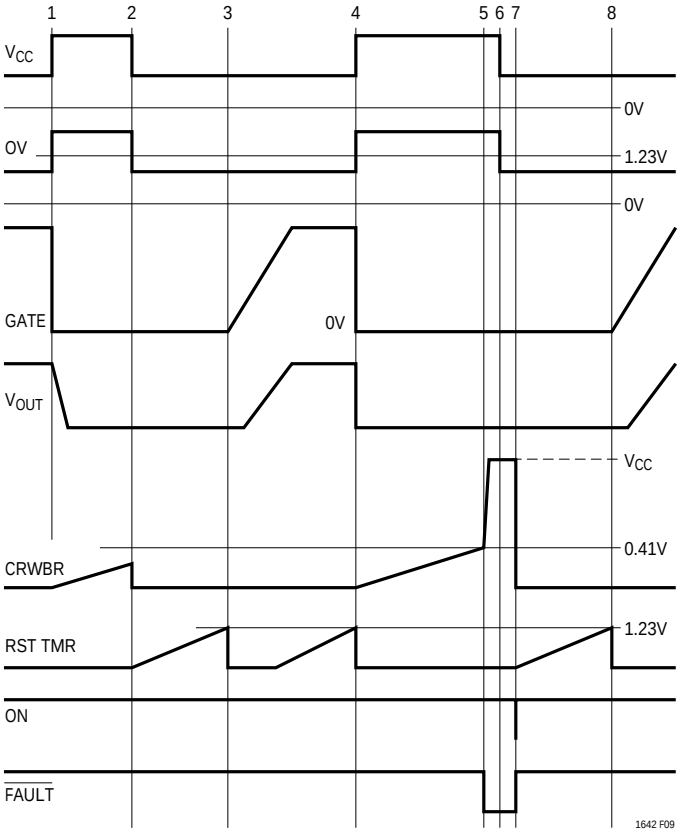


Figure 9. Overvoltage Timing (High Side)

APPLICATIONS INFORMATION

goes low at time 7, and GATE begins charging at time 8, one RST TMR cycle after FAULT goes high.

Figure 10 shows typical waveforms when the OV divider is driven from the N-channel's low side. Because the voltage driving the divider collapses after the OV comparator trips, FAULT stays high and CRWBR stays near ground, which prevents the pin from triggering an SCR. The GATE voltage begins ramping up after a RST TMR timing cycle.

Automatic Restart

If there is an overvoltage, and the resistor divider feeding OV is connected to the output of the N-channel pass transistor, the LTC1642 will automatically restart even if FAULT is not tied to ON. If the divider is connected to the input side, the LTC1642 will restart itself only if FAULT is tied to ON, and only after the overvoltage clears.

The OV and FB Comparators

The propagation delay through the OV and FB comparators on low to high transitions depends strongly on the differential input voltage. The relationship is shown in Figure 11. The minimum propagation delay for large overdrives is about 20µs. In addition the comparators have 3mV of hysteresis.

Internal Voltage Clamp Protection

The LTC1642 includes a shunt regulator to protect itself from V_{CC} and SENSE pin voltages up to 33V. The regulator turns on when V_{CC} exceeds 16.5V and limits most of the chip's circuitry to 15V. When it is on the chip functions normally with one exception: if the charge pump is on, the GATE voltage is usually near ground but this is not guaranteed. Use the OV pin to ensure that GATE is grounded. The pull-up voltage on the RESET and FAULT pins follows V_{CC} until the shunt regulator turns on. When the regulator is on the pull-up voltage is 14.4V.

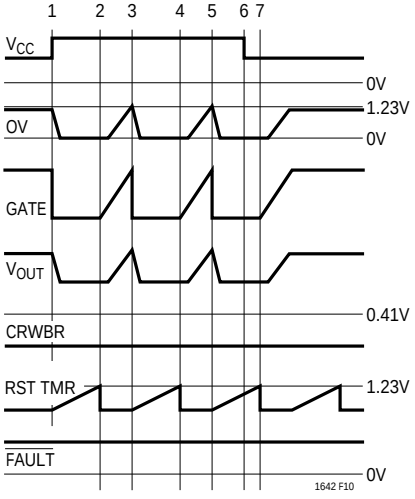


Figure 10. Overvoltage Timing (Low Side)

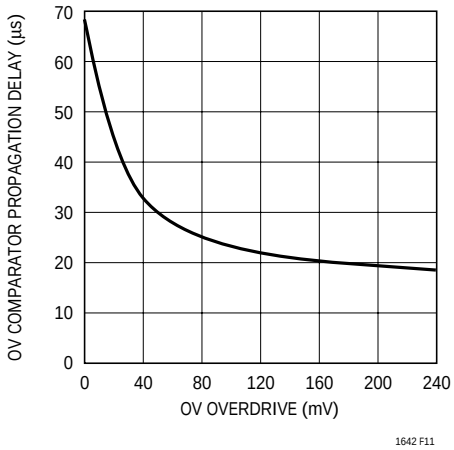


Figure 11. OV Comparator Propagation Delay vs Overdrive Voltage

APPLICATIONS INFORMATION

Undervoltage Monitor

The LTC1642 will assert $\overline{\text{RESET}}$ if a monitored voltage falls below a programmable minimum. When the monitored voltage has exceeded its minimum for at least one system timing cycle, $\overline{\text{RESET}}$ goes high. The monitoring circuitry comprises an internal 1.23V bandgap reference, an internal precision voltage comparator and an external resistive divider to monitor the output supply voltage. The circuit is shown in Figure 12, and typical waveforms in Figure 13. When the voltage at the FB pin rises above its reset threshold (1.23V), the comparator output goes low and a timing cycle starts (times 1 and 5). Following the cycle $\overline{\text{RESET}}$ is pulled high.

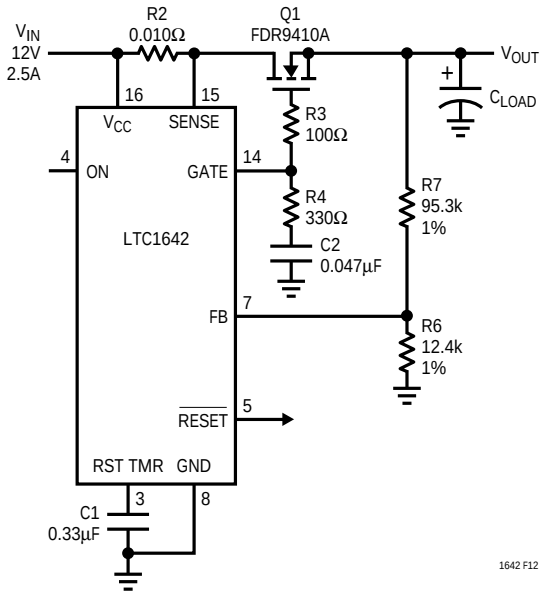
At time 2 the voltage at FB drops below the comparator's threshold and $\overline{\text{RESET}}$ is pulled low. If the FB pin rises above the reset threshold for less than a timing cycle the $\overline{\text{RESET}}$ output will remain low (time 3 to time 4). The 15µA pull-up current source to V_{CC} on $\overline{\text{RESET}}$ has a series diode so the pin can be pulled above V_{CC} by an external pull-up resistor without forcing current back into the supply.

Reference

The LTC1642's internal voltage reference is buffered and brought out to the REF pin. The buffer amplifier should be compensated with a capacitor connected between REF and ground. If no DC current is drawn from REF, 0.1µF ensures an adequate phase margin, but the minimum compensation increases if REF sources a substantial DC current, as shown in Figure 14.

Uncommitted Comparator

The uncommitted comparator has an open drain output. The comparator has 3mV of hysteresis: the output goes high when the differential input voltage exceeds 1.5mV and goes low when the differential input is less than –1.5mV.



ALL RESISTORS ±5% UNLESS NOTED.
FB COMPARATOR TRIPS AT V_{OUT} = 10.7V

Figure 12. Undervoltage Monitoring Circuitry

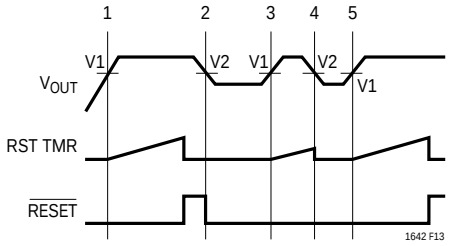


Figure 13. Supply Monitor Waveforms

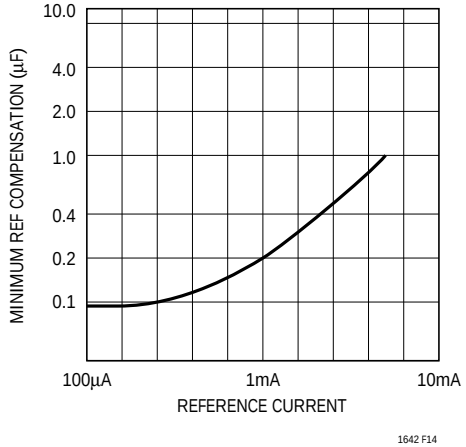
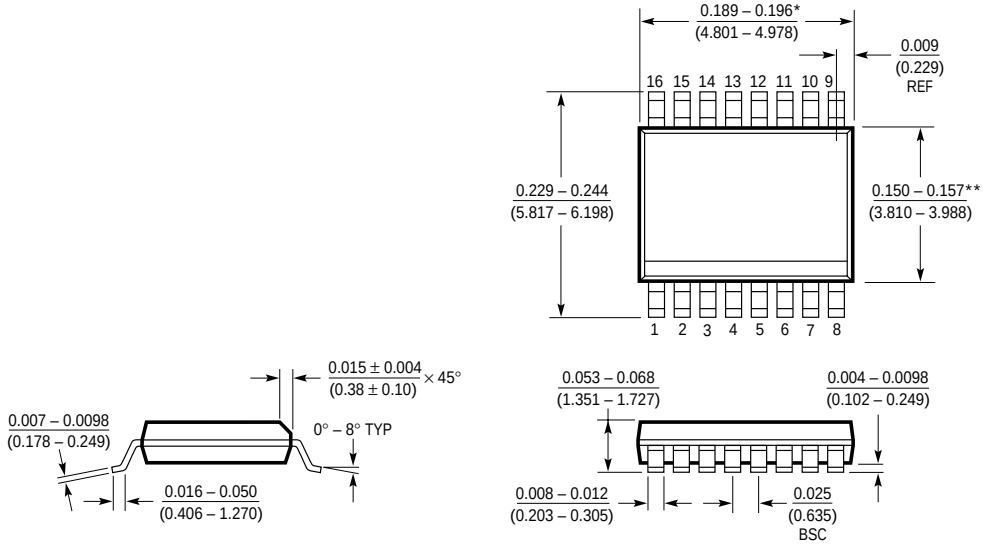


Figure 14. Minimum REF Compensation vs REF Current

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

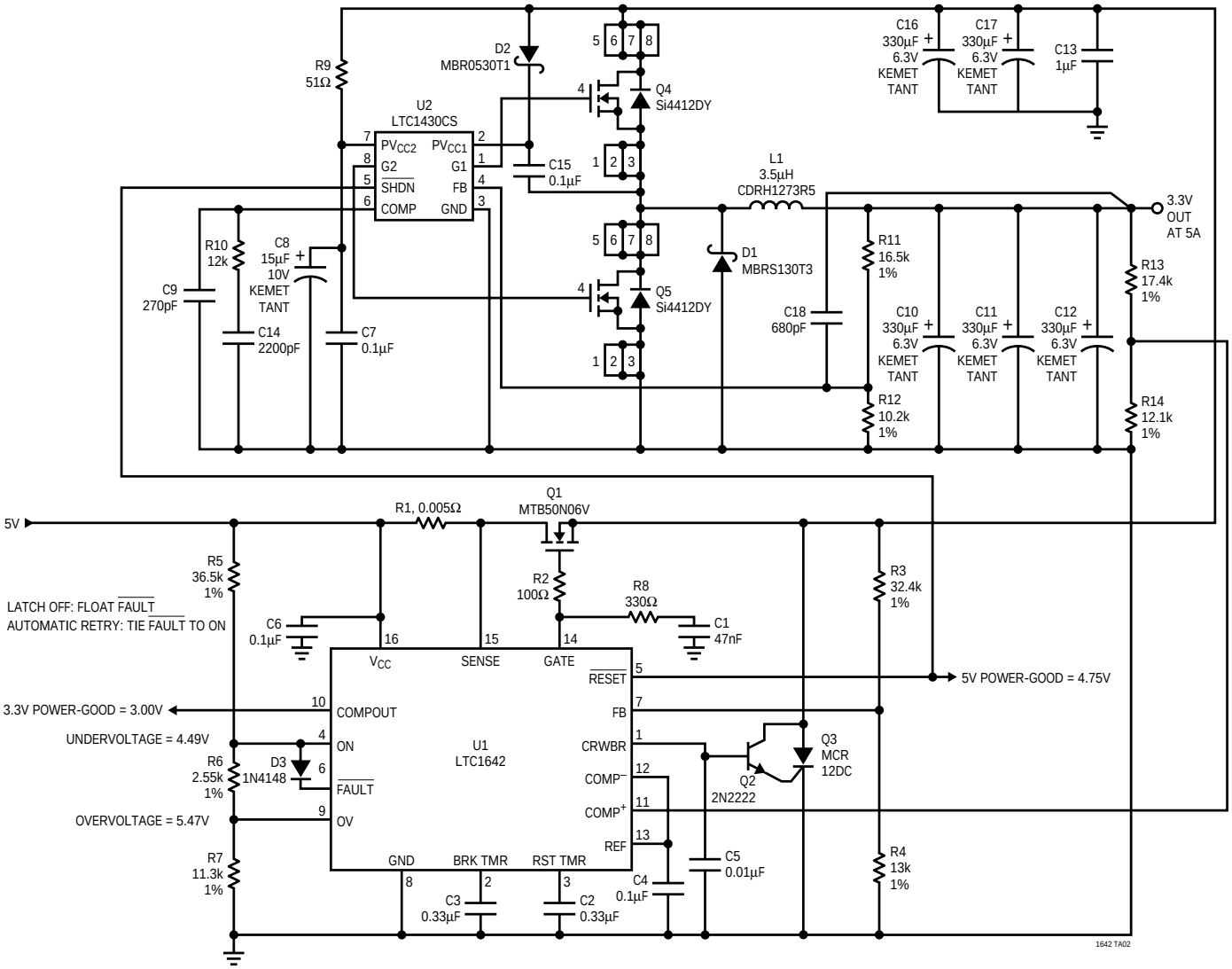


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

5V To 3.3V Hot Swap Supply Using the LTC1430



ALL RESISTORS 5% UNLESS OTHERWISE NOTED
RESET TIME = 200ms
CURRENT LIMIT TIME =20ms
CROWBAR TIME = 90µs

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Multiple Supplies
LTC1422	Hot Swap Controller	Single Supply in SO-8
LT1640	Negative Voltage Hot Swap Controller	Negative High Voltage Supplies
LTC1643	PCI-Bus Hot Swap Controller	3.3V, 5V, 12V, –12V Supplies for PCI Bus

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1642is, sn1642 LT/TP 0599 4K • PRINTED IN USA